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Intrinsic Fermi Level and Charged Intrinsic Defects Density in Doped Semiconductors from the Band offsets of MIS Device Interfaces

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Abstract: *Intrinsic Fermi level and charged intrinsic defect density in doped semiconductors has been calculated by a new method proposed earlier, that utilizes the conduction band offset in a semiconductor/insulator interface of an MIS device. This paper generates new and improved data to corroborate the new method. The method is now found to be applicable to all semiconductors, provided the band offsets are determined correctly. Very high and very low values of defect densities can be obtained by this new method that is not possible by the existing experimental techniques like DLTS, EPR, and others. The article also gives a new equation of the intrinsic Fermi level in semiconductors with an added term due to the density of charged intrinsic defects.*

Keywords: *Charge Neutrality Level, Intrinsic Fermi level, Intrinsic Defects, MIS devices, Diamond*

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I. Introduction

Point defects are zero-dimensional defects in semiconductor crystals. They can physically be a vacancy (Schottky defect), an interstitial, a vacancy-interstitial pair (Frenkel), extrinsic point defect as an impurity atom, or a split interstitial defect. In a compound semiconductor such as GaAs, the presence of two types of atoms opens the possibility of having a Ga atom in place of an As atom. This type of defect is called a Ga antisite defect. There could also be complexes of this defect with other native or extrinsic point defects such as a antisite-vacancy complex. Point defects are electrically active defects as they can be in more than one charge state as a donor or acceptor defect. As a donor, the defect is neutral when occupied by the electron and is positive after donating an electron. In the same way, the acceptor is negative when occupied by electron and becomes neutral when empty. Thus, the point defects can be classified as shallow level defects with their energy levels close to the CB or VB, or deep level defects with their energy levels away from the CB or VB edges. An understanding of point defect physics can be gained by combining theory and experiment [1]. Just like point defects, there are line defects such as dislocations, surface defects such as grain boundaries and volume defects such as precipitates and clusters. All these crystallographic defects in a semiconductor sample produce energy levels in the band gap and affect the device characteristics through generation and recombination currents. The trap close to the intrinsic Fermi level is the most effective generation-recombination centre. In a p^+n-junction and a metal-semiconductor Schottky diode, generation current via defects dominate in the reverse bias and the recombination current via defects dominate the diode current-voltage characteristics in forward bias. Defects can be good for the diode as a switch because the generation-recombination current reduces the carrier lifetime and thus turns on and off the switch faster. Defects can be bad for the diode as a detector, because the generation-recombination current increases the leakage current in the diode and the change in current due to radiation is reduced.

In this article, the density of charged intrinsic defects, N_{id}, is determined by identifying the position of the intrinsic Fermi level in a semiconductor having all types of crystallographic defects from the band offset measurements of a Metal-Insulator-Semiconductor (MIS) device. The intrinsic defects are charged deep level defects in a doped semiconductor. The method presented utilizes the physics of charge neutrality in a semiconductor leading to formulating the intrinsic Fermi level with an additional term due to N_{id}. Defect density calculations have been performed on Si, SiC and Diamond semiconductors in one group and in other compound semiconductors in another group. The method is particularly able to determine very low defect density in Diamond and very high defect density in 3C-SiC, which otherwise is not possible by the existing techniques such as Deep Level Transient Spectroscopy (DLTS), Electron Paramagnetic Resonance (EPR) and others [1].

II. Theory

The theory has been presented again to make the article independent and provide immediate reference at hand. In general, the charge neutrality equation for a semiconductor material can be written as:

$$n - p + N_A^- - N_D^+ + N_{id} = 0; \quad (1)$$

where, n is the density of conduction electrons, p is the density of valence holes, N_A^- is the density of shallow acceptors, N_D^+ is the density of shallow donors, and N_{id} is the intrinsic defects density of charged acceptor/donor deep traps that compensate the shallow donors/acceptors in a semiconductor. For an n-doped semiconductor, the equation will reduce to:

$$n - p - N_D^+ + N_{id} = 0 ; \quad (2)$$

and further if the semiconductor is made intrinsic by removing N_D^+, then the equation will reduce to:

$$n - p + N_{id} = 0 ; \quad (3)$$

This gives the equation:

$$n + N_{id} = p. \quad (4)$$

Solving the equation further,

$$\ln (1+ N_{id}/n) = \ln (p/n). \quad (5)$$

The hole concentration p in a semiconductor is given as:

$$p = N_V \exp(-\tfrac{E_F - E_V}{kT}) , \quad (6)$$

and the electron concentration n is given as:

$$n = N_C \exp\left(-\tfrac{E_C - E_F}{kT}\right). \quad (7)$$

In equations (6) and (7), N_C is the density of states in the conduction band, N_V is the density of states in the valence band, E_C is the bottom of the conduction band, E_V is the top of the valence band, E_F is the Fermi level in a semiconductor, k is the Boltzmann constant, and T is the temperature in Kelvin. Substituting equations (6) and (7) for p and n in equation (5) gives:

$$\ln\left(1 + \tfrac{N_{id}}{n}\right) = \ln\left(\tfrac{N_V}{N_C}\right) + \tfrac{-E_F + E_V + E_C - E_F}{kT} \quad (8)$$

Since this is an intrinsic material, therefore $n = n_i$ and E_F is E_i. So the intrinsic Fermi level equation is given by:

$$E_i = \tfrac{kT}{2}\ln\left(\tfrac{N_V}{N_C}\right) + \tfrac{E_V + E_C}{2} - \tfrac{kT}{2}\ln(1 + \tfrac{N_{id}}{n_i}). \quad (9)$$

Usually, $N_V \cong N_C$, giving zero for the first term in equation (9). However, it can produce a change of minus 0.01 eV in E_i of Silicon and plus 0.035 eV in E_i of GaAs. The second term is $\frac{E_V + E_C}{2}$ is the middle of the bandgap for a semiconductor. Therefore, E_i can be written as:

$$E_i = \tfrac{E_g}{2} - \tfrac{kT}{2}\ln(1 + \tfrac{N_{id}}{n_i}). \quad (10)$$

Equation (9) is the equation for the intrinsic Fermi level in a doped semiconductor having charged defects. The second term on the right hand side of equation (10) is the additional term due to the density N_{id} of charged deep donor or acceptor traps in a doped semiconductor. The negative sign indicates that the energy due to N_{id} is above the midgap. It can be observed from this equation, that if the position of the intrinsic Fermi level in a semiconductor having defects is identified, then with the known bandgap of the semiconductor, the density of charged deep bulk defects in a doped semiconductor, N_{id} can be determined. These bulk defects will also show up on the surface of the semiconductor sample, such that, if N_{id} is high, then the surface density of defects will also be high, leading to pinning of the Fermi level at the interface with an insulator or metal as the case may be. Fermi level pinning would mean that the charge density at the interface cannot be changed by the application of bias.

III. Results And Discussion

The identification of E_i from semiconductor/insulator band offsets and calculation results of charged defect density is discussed first. MIS characterization has been performed on n^+ polysilicon gated n-channel silicon MOSFETs giving the Si/SiO_2 CBO and VBO as 3.2 eV and 4.6 eV respectively. The bandgap of SiO_2 is determined to be 8.9 eV and the electron and hole conductivity effective masses in SiO_2 are found to be 0.42m and 0.58m, where m is the free electron mass [2]. For an effective electron mass of 0.42m, the Si/SiO_2 band offset from the intrinsic Fermi level is given as$8.9\ x\ 0.421 \cong 3.75\ eV$. The CBO of 3.2 eV added to 0.55 eV gives 3.75 eV. This 0.55 eV addition brings the CBO relative to the intrinsic Fermi level in silicon. This is also 0.01 eV less than midgap value for Si, meaning that the CBO of the Si/SiO_2 interface relative to intrinsic Fermi level of silicon, which is nearly at midgap, is 3.75 eV. The band offset for all the semiconductor/SiO_2 interfaces of 3.75 eV will thus identify the intrinsic Fermi level position in any semiconductor. TABLE I below gives the band offsets at the interfaces of Si, SiC and Diamond with SiO_2 CB in columns 4 and 5. ΔE_c in column 4 is determined by subtracting E_g from Φ_e, and Φ_e is determined by the internal photoemission of electrons from the

semiconductor valence band to the oxide conduction band. ΔEc subtracted from 3.75 eV gives E_c-E_i in column 6, which is the position of the intrinsic Fermi level in that semiconductor. The 3.75 eV level from the bottom of the SiO_2 CB is the Charge Neutrality Level (CNL) in thermal SiO_2 and the intrinsic Fermi level position in the semiconductor is the CNL in that semiconductor. The CNL in SiO_2 of 3.75 eV obtained by using the semiconductor/SiO_2 system [2], from the bottom of SiO_2 CB matches closely to the value of 5.04 eV from the top of the SiO_2 VB determined experimentally by Yeo et al using a metal-dielectric system [3].

Table I. The semiconductor bandgap (E_g), the photoemission barrier (Φ_e), the CBO and VBO, the position of intrinsic Fermi level (E_i), the energy due to N_{id}, intrinsic carrier concentration (n_i) and the intrinsic defect density (N_{id}) for Si, SiC and Diamond/SiO_2 interfaces, SiO_2 (E_g=8.9 eV).

sc	E_g(300K)	Φ_e	ΔE_c	ΔE_v	E_c - E_i	E_c-E_g/2	E_i-E_g/2	n_i (cm^{-3})	N_{id}(cm^{-3})
Si	1.12	4.3	3.2	4.6	0.55	0.56	-0.01	1.5E10	1.7E10
4H-SiC	3.26	6.0	2.78	2.9	0.97	1.63	-0.66	1.0E-08	1.1E14
6H-SiC	3.02	6.0	2.95	2.9	0.80	1.51	-0.71	1.0E-6	5.2E17
15R-SiC	2.96	6.0	3.0	2.9	0.75	1.48	-0.73	2.0E-6	4.8E18
3C-SiC	2.38	6.0	3.6	2.9	0.15	1.19	-1.04	1.5E-1	1.8E33
Diamond	5.5	6.9	1.4	2.0	2.35	2.75	-0.4	1.0E-26	2.3E-13

Thus, column 6 provides the position of the intrinsic Fermi level below the conduction band of the semiconductors Si, SiC, and Diamond. From equation (10) it can be seen that the energy due to N_{id} relative to E_i is given in column 8. Given the n_i values in column 9, the N_{id} concentrations in the semiconductors are calculated using equation (10) and presented in column 10. It can be observed that the key to finding the N_{id} volume density is identifying the intrinsic Fermi level position in a doped semiconductor/insulator interface. Here, Si and SiC samples are doped n-type and the Diamond sample is doped p-type. The energy for E_i relative to midgap is negative in column 8 indicating that it lies in the upper half of the bandgap.

A literature survey of charged defect density calculations provides N_{id} data for three of the six semiconductors in TABLE I: Si [4], 4H-SiC [5-7], and 6H-SiC [8]. These data match very well to the calculations in the TABLE and hence the author has the confidence in the theory and method of calculating N_{id} presented in this article. Comparing the N_{id} values for Si, SiC, and Diamond, it can be observed that N_{id} in SiC is at least 10^4 times more than in Si and very small in Diamond. Since the bulk defect density will be reflected at the interface also, therefore it can be inferred that SiC/SiO_2 interface will have more defect states than Si and Diamond. This is also established by the MOS device study of Si, SiC and Diamond. Si MOS study gives interface trap density (D_{it}) in the low 10^{11} order near conduction band (CB) [9], SiC MOS study gives D_{it} in the 10^{13} order near CB [10], and Diamond MOS has D_{it} in the low 10^{10} order near CB [11], and these values are all without any kind of interface passivation. It needs to be mentioned here that near conduction band means physically near the semiconductor/oxide interface on the semiconductor side. SiC is thus more defective than Si and Diamond, although research efforts are underway to reduce D_{it} in SiC MOS device to the level of Si MOS device [10]. It can be observed that Boron doped p-type-(100) oriented type IIb natural Diamond substrate[11] has the best interface with the SiO_2 having the least N_{id}. The observation of the N_{id} data in TABLE I for various polytypes of SiC reveals that the 3C-SiC with a bandgap of 2.4 eV has the highest N_{id} of 1.8E33/cm^3. The N_{id} values progressively decrease with the increasing bandgap of SiC polytypes. This observation is related to the sp^2-bonded carbon clusters at the SiC/SiO_2 interface. The interface states are predominantly donor type up to 2.25 eV bandgap of 3C-SiC. The interface states above 2.25 eV become predominantly acceptor type up to 3.26 eV bandgap of 4H-SiC which compensate the donor states and reduce the total N_{id} in 4H-SiC [12]. The energy position of the neutrality level is 3.75 eV instead of the estimated 3.5 eV in the reference [12]. This 3.75 eV below the bottom of the SiO_2 CB gives the position of the intrinsic Fermi level in all semiconductor/SiO_2 interface systems. If the Fermi level in the semiconductor is above 3.75 eV, then the interface traps will capture and emit electrons with the CB and are called acceptor-like traps or electron traps. If the Fermi level in the semiconductor is below 3.75 eV, then the interface traps will capture and emit holes with the VB and are called donor-like traps or hole traps. Similarly, if a deep intrinsic defect in a semiconductor is above the intrinsic Fermi level, then it is an acceptor defect, and if the deep intrinsic defect is below the intrinsic Fermi level in the semiconductor, then it is a donor defect. Considering SiO_2 alone, the deep defects in SiO_2 from CB to 3.75 eV will be acceptor type and deep defects from 3.75 eV to VB of SiO_2 will be donor type with 3.75 eV as the CNL in SiO_2. It is known that the trap centre close to the intrinsic Fermi level in a semiconductor will affect the minority carrier lifetime by reducing it the most. An example for this observation is found in the study of Klein et al [6] where the group has shown that the Z1/Z2 trap centre at 0.65 eV level from the CB in 4H-SiC acts as a lifetime killer alone in 4H-SiC. This centre is the closest to the intrinsic Fermi level of 0.97 eV calculated and presented in TABLE I above. Thus, the calculated intrinsic Fermi levels in semiconductors can assist in

identifying the minority carrier lifetime reducing trap in a semiconductor or at what level to introduce a trap centre intentionally to reduce minority carrier lifetime.

In a charged semiconductor/SiO_2 interface, band offset measurements by photoemission techniques could be in error. This problem and its solution is discussed next. Thermal SiO_2 grown on Si has small D_{it} of 10^{10} cm^{-2} eV^{-1} after H_2 passivation, and fixed positive charge density near the interface in the oxide of $10^{10}/cm^2$. These values of densities are small and the defect charges do not affect the internal photoemission measurements, even for ultrathin oxide of 2-4 nm [13]. Thin oxides with large charge density can cause band bending in the semiconductor of the semiconductor/oxide interfaces. The charges trapped at the interface states and fixed positive charge can cause band bending downwards so as to cause accumulation in n-semiconductor and the VBO will be less than actual and the CBO will be more than actual. Negative charges at the interface and in the oxide will cause depletion in the n-semiconductor and the CB will bend upwards giving less than actual CBO and more than actual VBO. A similar analysis can be performed for the p-type semiconductor, where the fixed positive charge will cause depletion in the p-semiconductor and the fixed negative charge will cause accumulation in the p-semiconductor. A good review on internal photoemission explains this problem [14]. The remedy for this is to have a thick oxide of 20 nm or more such that the voltage required at the gate of the MIS device to compensate the charges fall more across the oxide due to its higher resistance and less across the semiconductor, thus causing almost no band bending at the semiconductor surface. The literature provides support for this method on SiC/SiO_2 interfaces, where oxide thickness greater than 20 nm [15] and 40 nm [16] were taken in the samples. In other words, flatband voltage correction must be made in an MIS device [16].

The new method to calculate N_{id} values in a semiconductor is presented above again and was proposed in the author's earlier article [17]. N_{id} obtained by this new method is matched with intrinsic defect densities obtained by Photothermal Deflection Spectroscopy (PDS), Deep Level Transient Spectroscopy (DLTS) and Positron Annihilation Spectroscopy (PAS) in separate experiments by research groups, thus corroborating the new method. Some compound semiconductor/Al_2O_3 interface systems have been studied by Afanasev by internal photoemission technique [18]. The author has utilized the photoemission barrier and conduction band offset data generated by Afanasev on compound semiconductor/Al_2O_3 interface systems to confirm and support the new method in the form of TABLE II in the article on the proposed new method [17]. The experimental Φ_e data of Afanasev has now been found to be erroneous in terms of their absolute values. They have been corrected by many research groups by performing experiments on MOS devices fabricated after surface treatments of semiconductor samples and annealing of the devices [19-24]. The purpose of this article is to replace the values of photoemission barrier, Φ_e, and the conduction band offset data of Afanasev in TABLE I of his review article [18], and update the TABLE II of the author's previous article that proposed the new method [17]. GaN/SiO_2 CB offset and calculated N_{id} values are an addition to this TABLE I [25]. The values of N_{id} inTABLE IIof the present article are now different than before and corroborates the new method more convincingly, thereby validating the applicability of the new method to all semiconductors.

The review article by Afanasev reports a trend in Φ_e values, in a semiconductor/Al_2O_3 interface systems, having semiconductors such as GaAs, InGaAs, InAs, InP, GaP, GaSb, InSb etc [18]. The photoemission barrier, Φ_e, from the semiconductor VB to the oxide CB, for all the Arsenic containing semiconductors as the group V anion and having an interface with Al_2O_3, is the same 3.45 eV, which is presented in Fig. 29 of reference [18]. However, there is an interlayer dielectric due to the oxidation of the semiconductor surface that changes the electron photoemission yield. A clean and passivated semiconductor surface with Sulphur changes the photoemission barrier to 3.0 eV for GaAs and 2.95 eV for InGaAs [19, 20]. Following the trend of group V anion (As) containing semiconductor, all the semiconductor/Al_2O_3 interfaces having As anion have a photoemission barrier from the semiconductor valence band to the oxide conduction band as 3.0 eV instead of 3.45 eV. Similarly, the photoemission barrier for the phosphide and antimonide containing semiconductor/Al_2O_3 interfaces are corrected after surface passivation or annealing. The references that correct these Φ_e values are mentioned in the box brackets of the TABLE I below. The review article by Afanasev also points out that the VB of semiconductor retains its energy position with respect to the reference level of amorphous Al_2O_3 CB bottom for all same Group V anion containing semiconductors, and that the energy of the oxide CB bottom is marginally sensitive to the composition of the oxide. This is important because the bandgap of amorphous Al_2O_3 has been found to vary from 6.1 eV for the amorphous phase to 7.83 eV for the crystalline cubic phase depending on its composition, and so the changes in bandgap of Al_2O_3 mainly affects the VB offset, although, the CB offset is also affected to some extent. It is for this compositional difference in Al_2O_3, that the semiconductor/SiO_2 interface systems are a better choice for the purpose of N_{id} determination from the band offsets.

DLTS is an experimental method of determining the deep level trap concentration in a semiconductor when the trap concentration is much much smaller than the doping concentration in the semiconductor. DLTS has been performed on many semiconductors. One sample reference is given for GaAs [26], InGaAs [27], GaP [28], InP [29], GaSb [30] and GaN [31] semiconductors. The trap concentrations obtained by PDS, DLTS and

PAS techniques, matched those calculated by the new method from the MIS band offsets [16], thus corroborating the new method. It is to be reminded that the intrinsic Fermi level is identified by subtracting ΔE_c from 3.75 eV for the semiconductor/SiO_2 interface system and by subtracting ΔE_c from 2.65 eV for the semiconductor/a-Al_2O_3 interface system. The value of 2.65 eV is obtained as a control band offset for Si/a-Al_2O_3 from the intrinsic Fermi level of Si, given that the CB offset for Si/a-Al_2O_3 is 2.1 eV as given in TABLE II below. The (E_i-E_g/2) values are presented in column 7 in the TABLE II below. The negative sign indicates that the intrinsic Fermi level, E_i, is in the upper half of the bandgap of a semiconductor, and the positive sign indicates that E_i is in the bottom half of the bandgap of a semiconductor.

A revised opinion of the author on the limitation of the new method due to carrier dependent Fermi level pinning is, that the intrinsic Fermi level is purely based on the band offsets of semiconductor/insulator interface systems and Fermi level pinning due to dopants does not pose a restriction on determining N_{id} by the new method for any semiconductor, provided the band offsets are correct. Charges trapped at the surface states of the semiconductor or in the insulator causes band bending at zero bias and needs to be accounted for in the conduction band offset determination. A good example of this effect is in determining the CBO of the GaN/SiO_2 interface system, where the correction for the band bending gives the average CBO of 2.8 eV from four offsets of 2.6, 2.7, 2.8, and 3.0 eV [25], presented in Fig.12 of the reference. The CB and VB bending at zero bias if not included in the offsets will result in incorrect CBO and the VBO values, although the bandgap of the insulator will be correct because both the CB and VB bending due to charges is in the same direction and bends by the same amount [25].

Table II. The semiconductor bandgap (E_g), the photoemission barrier (Φ_e), the CBO (ΔE_c), the position of intrinsic Fermi level (E_i), the energy due to N_{id} in column 7, intrinsic carrier concentration (n_i) and the intrinsic defect density (N_{id}) for several compound semiconductor interfaces with a-Al_2O_3 (E_g=6.1 eV).

sc	E_g (300K)	Φ_e (eV)	ΔE_c	E_c-E_i	E_c-E_g/2	E_i-E_g/2	n_i (/cc)	N_{id} (/cc)	Ref.
Si	1.12	3.25--[18]	2.1	0.55	0.56	-0.01	1.5E10	1.7E10	
Ge	0.67	2.85--[18]	2.18	0.47	0.335	0.135	2.0E13	6.7E17	
GaAs	1.42	3.0--[18, 19]	1.58	1.07	0.71	0.36	2.1E06	2.5E18	[26]
$In_{0.53}Ga_{0.47}As$	0.74	2.95--[18, 20]	2.21	0.44	0.37	0.07	6.3E11	6.5E14	[27]
InAs	0.35	2.95--[18, 21]	2.60	0.05	0.175	-0.125	1.0E15	1.5E19	
GaP	2.24	3.5--[18, 22]	1.26	1.39	1.12	0.27	2.7E06	3.1E15	[28]
InP	1.35	3.5--[18, 22]	2.15	0.50	0.675	-0.175	1.3E07	9.6E12	[29]
GaSb	0.73	3.13--[18, 23]	2.4	0.25	0.365	-0.115	1.5E12	1.1E16	[30]
InSb	0.17	2.90--[18, 24]	2.73	-0.08	0.085	-0.165	2.0E16	6.8E21	
GaN/SiO_2	3.4	6.2---[25]	2.80	0.95	1.7	-0.75	1.9E-10	2.7E15	[31]

A discussion on the correlated band offset and N_{id} is made here. The band offset for the GaAs/a-Al_2O_3 interface system determined by Nguyen et al [19] equals 1.58 eV. This translates to an N_{id} value of 2.5E18/cm^3 as presented in the TABLE. Huang et al [32] has determined the same band offset as 1.68 eV, but the sample did not undergo Sulphur passivation of the GaAs surface. This band offset translates to a N_{id} value of 1.1E15/cm^3. It can be observed that for a 0.1 eV change in energy value of the intrinsic Fermi Level, there is three orders of magnitude change in N_{id} value. It can be further calculated that for a 0.03 eV change in energy of E_i-E_g/2, there is one order change in N_{id} value. It shows that the band offset values have to be determined very accurately to the second decimal place to pin-point N_{id} values. It is difficult to measure the band offset accurately to two decimal places. Different measurement techniques yield vastly different band offsets as can be observed in the TABLES of the article by Bersch et al [13]. The resolution of the photoemission techniques of finding band offsets is ±0.1 eV, which has to be kept in mind and is found insufficient for the purpose of N_{id} determination. Ideally, it should be 0.01 eV, that is, the second decimal place for band offset is important, which can be obtained by using the BOEMDET technique of MIS characterization [33]. Since Nguyen's value matched with the N_{id} in GaAs determined by the PDS technique [26], therefore 1.58 eV band offset was considered to be correct assuming a state of the art GaAs growth method is used to make the sample. The XPS data in Huang's work is not corrected for charges at the surface states of GaAs/a-Al_2O_3 interface and charges in the oxide, which are probably high and can affect the determination of Core Level (CL) and Valence Band Maximum (VBM) values [16, 34].

IV. Conclusion

The present article again presents the new method of calculating the density of charged intrinsic defects in doped semiconductors by identifying the intrinsic Fermi level in any semiconductor from the band offset measurements of MIS devices. Very low and high defect densities can be obtained by this method such as in Diamond and 3C-SiC, that are not possible by other existing experimental techniques like DLTS, EPR etc. The article also gives a new equation of the intrinsic Fermi level in semiconductors with an added term due to the density of charged intrinsic defects. The new method is a generalized method applicable to all semiconductors,

provided the conduction band offsets are determined correctly. Band bending due to charges trapped at the surface states and charges in the dielectric near the interface should be accounted for in determining the CB and VB offsets. The carrier dependent Fermi Level pinning does not pose a restriction in determining N_{id} by the new method. The calculated intrinsic Fermi levels in semiconductors can assist in identifying the minority carrier lifetime reducing trap in a semiconductor. The semiconductor/SiO_2 interface systems are a better choice for the MIS devices utilized in this method.

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