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A new F-shaped XOR gate and its implementations as novel adder circuits based Quantum-dot cellular Automata (QCA)

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Abstract: *Quantum-dot cellular automata (QCA) is a novel nanotechnology that promises smaller size, lower power consumption, with faster speed and is considered as a solution to the scaling problems in complementary metal oxide semiconductor technology. We propose a novel QCA F-shaped XOR gate. The proposed gate is simple in structure and powerful in terms of implementing digital circuits. We implement novel adder circuits like half adders and half subtractors by introducing the proposed XOR gate. The proposed adder circuits are simple in design and occupy a fraction of area, as compared to previous designs. These circuits are suitable for optimizing the complex structures. Simulation results demonstrate that the new structures have achieved significant improvements in terms of circuit complexity. The functionality of proposed structures have been checked by QCADesigner tool.*

Key words: *Nanotechnology, Quantum Dot Cellular Automata (QCA), F-shaped XOR gate, Half-adder, Half-subtractor*

I. Introduction

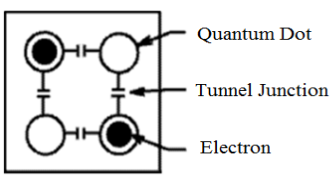
A number of research efforts have been focused on new devices that might replace CMOS technology [1]. The CMOS technology in nano scale has some fundamental problems because of increase in amounts of variation in every aspect of nanometer design. One conventional way to enhance the performance of logic system is to use parallelism [2]. Utilizing the QCA technology for implementing logic circuits is one of the approaches, QCA can be used to implement combinational circuits by properly arranging cells in series. Recently several studies have been reported about combinational circuit design, such as QCA full adder [3, 4], [7-9]. Multiplexer [5] and Programmable Logic Array [6], etc. In this paper, we have proposed a novel F-shaped XOR gate with proper arrangement of cells and clocks, which consists of less area, circuit complexity as compared to previous structures [10].The objective of this paper is to introduce a new detailed design, QCA layout and simulation results of combinational circuits based on F-shaped XOR gate. We have proposed an optimal design of adder circuits like half adder, half subtractor, based on F-shaped XOR gate, which consists of less area and circuit complexity as compared to previous structures [16].

II. Quantum-dot cellular automata

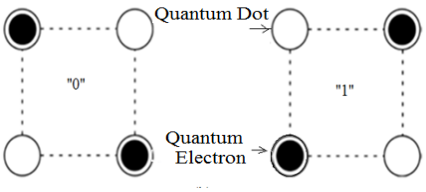
The fundamental unit of QCA device is QCA cell, created with four quantum-dots positioned at the vertices of a square [12, 13] coupled by tunneling barriers as shown in Fig. 1(a). These quantum dots are sites in which electrons are able to tunnel between them but cannot leave the cell. The electrons will tend to occupy diagonally opposite into the quantum dots due to electrostatic force of interaction. The electrons are quantum mechanical particles and they are able to tunnel between the dots in a cell.

Quantum-dots are small semi-conductor or metal islands with a diameter that is small enough to make their charging energy greater than k_bT (where k_b is Boltzmann's constant and T is the operating temperature). In the future, they will shrink to regions within specially designed molecules. If this is the case, they will trap into the charge barriers [14, 21].

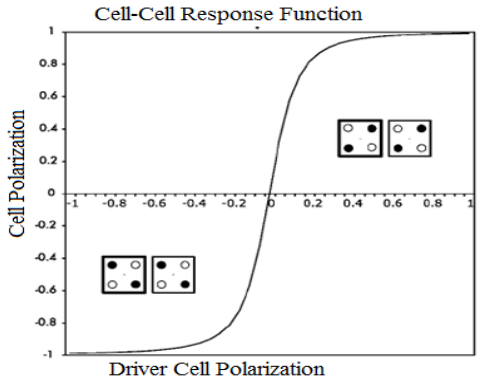
Exactly two mobile electrons are loaded in the cell and can move to different quantum dots in the QCA cell by means of electron tunneling. Tunneling paths can be represented by the lines connected the quantum-dots in Fig. 1(b). The electrons in the cell that are placed adjacent to each other will interact; as a result, the polarization of one cell will be directly affected by the polarization of its neighboring cells.



(a)



(b)



(c)

Fig. 1: (a) Basic QCA Cell; (b) Basic four-dot QCA cell showing the possible ground-state polarizations (c) Non-linear interaction between QCA cells.

If the barriers between cells are sufficiently high, the electrons will be well localized on individual dots. The Coulomb repulsion between the electrons will tend to make them occupy antipodal sites in the square as shown in Fig. 1(b). For an isolated cell there are two energetically equivalent arrangements of the extra electrons which we denote as a cell polarization P = +1 and P = -1. The cell polarization is used to encode binary information, thus, P = +1represents a binary 1 and P = -1 represents a binary 0. The two polarization states of the cell will not be energetically equivalent if other cells are nearby. Consider two cells close to one another as shown in the inset of Fig. 1(c)

Fig. 1(c) inset illustrates the case when cell 2 has a polarization of +1. It is clear that in that case the ground-state configuration of cell 1 is also a +1 polarization. Similarly if cell 2 is in the P = −1 state, the ground state of cell 1 will match it. This shows the nonlinear response of the cell–cell interaction to which plays the role of voltage gain in conventional devices restoring signal levels at each stage.

2.1 QCA logic circuits

Some basic elements for QCA logic implementation are wire, inverter, and majority voter [15] shown in Fig. 2(a, b, c & d). The QCA wire is formed by an array of QCA cells shown in Fig. 2(a), which provides a medium for data propagation based on coulomb interactions. The simplest inverter is built by placing QCA cells in a diagonal structure shown in Fig. 2(b); the common inverter is built by seven cells shown in Fig. 2(c). The polarization of the output QCA cell 'out' or 'output' is the opposite of the polarization of input QCA cell 'in' or 'input'. QCA majority voter (MV) and its logic symbol are shown in Fig. 2(d). Here the MV, is equivalent to a logic function F (A, B, C) =AB+AC+BC and can be implemented by five QCA cells arranged in a cross. Cells A, B, and C are input cells, and cell D is the output cell that is polarized according to the polarization of majority of the input cells. Logical AND and OR functions can be implemented from majority voter by presetting one input immutably to binary values 0 and 1, respectively.

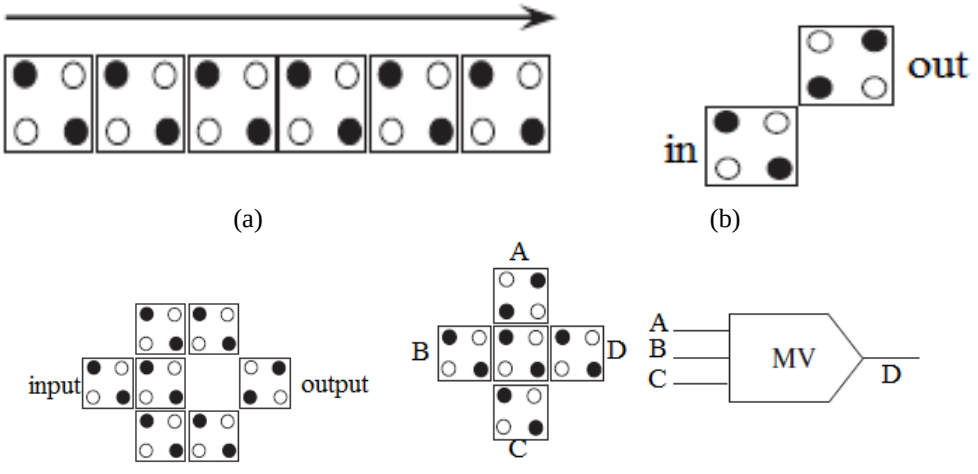
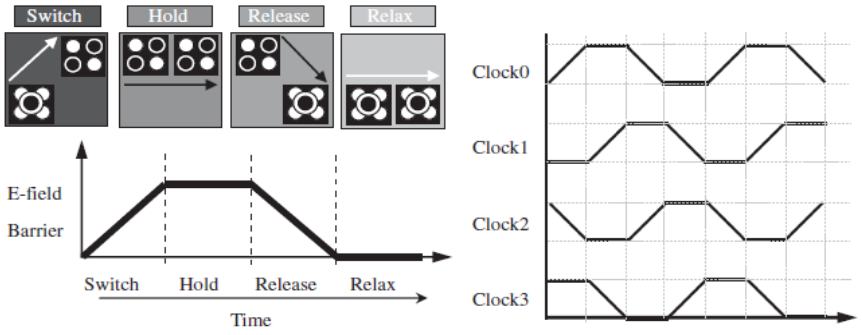


Fig. 2: Basic QCA logic devices: (a) Wire (b) and (c) Inverter (d) Majority vote.

2.2 QCA clock

A QCA cell has four clock zones and clock zone has four phases; Switch, Hold, Release and Relax [16]. Fig. 3(a) shows its operation process. During the switch phase, QCA cells begin unpolarized and their inter-dot potential barriers are low. The barriers are then raised during this phase and the QCA cells become polarized according to the state of their driver (i.e. their input cell). It is in this clock phase that the actual computation (or switching) occurs. By the end of this clock phase, barriers are high enough to suppress any electron tunneling and cell states are fixed. During the hold phase, barriers are held high so the outputs of the sub array can be used as inputs to the next stage. In the release phase, barriers are lowered and cells are allowed to relax to an unpolarized state. Finally, during the fourth clock phase, the relax phase, cell barriers remain lowered and cells remain in an unpolarized state [12-16]. Fig. 3(b) shows each clock zone signal and demonstrates pipeline mechanism. All cells in a certain zone are controlled by the same QCA clock signal. Cells in each zone perform a specific calculation; the state of a zone is then fixed so that it can serve as input signals to the next zone. Information transfers in a pipelined fashion.



(a) (b)

Fig. 3: (a) Four phases of QCA clock (b) Clock zones signal.

III. QCA Implementations

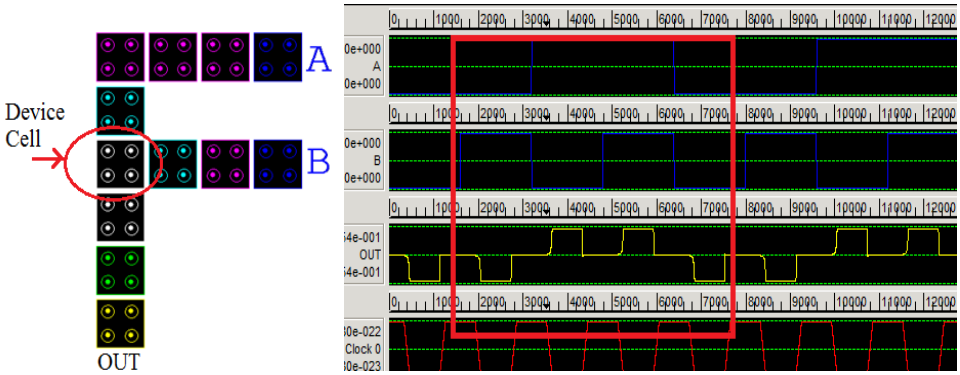
3.1 The proposed XOR gate

In addition to AND, OR, NOT, NAND and NOR gates, exclusive-OR (XOR) and exclusive-NOR (XNOR) gates are also used in the design of digital circuits. These have special functions and applications. These gates are particularly useful in arithmetic operations as well as error detection and correction circuits. XOR and XNOR gates are usually found as 2-input gates. No multiple-input XOR/XNOR gates are available since they are complex to fabricate with hardware. Different authors have proposed either the QCA implementation and simulation results for conventional layout [18-20] .The design have complexity of cells and coplanar crossovers or multiple layers to implement.

XOR gate is a logical operation of two operands that results in a logical value of true if and only if one of the operands, but not both, has a value of true. This forms a fundamental logic gate in many operations. The exclusive-OR (XOR) performs the following logic operation:

$$A \oplus B = A'B + AB'$$

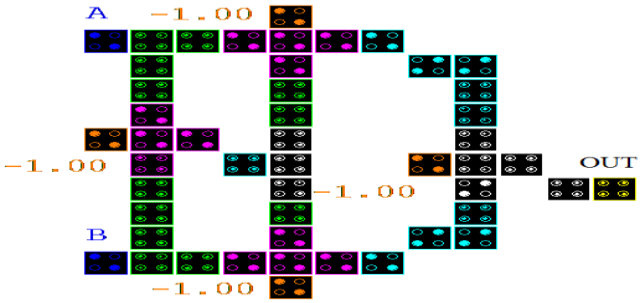
It is possible to implement all combinational and sequential logic functions by properly arranging cells so that the polarization of one cell sets the polarization of a nearby cell [22]. According to previous studies, several logic gates and computing devices has implemented with QCA [23]. We have propose a novel F-shaped XOR gates with simple arrangement of basic cells and consist of very less area 0.01um^2, of 12-cells with proper arrangement of 1-clock delay as compared to previous designs [10], [11]. The proposed QCA layout consists of single layer of basic cell arrangements and is in the shape of ‘F’ named as F-shaped XOR gate shown in Fig. 4(a) and its simulation results is shown in Fig. 4(b), have been verified using QCADesigner. The dotted line shown in Fig. 4(a) is called “device cell”, can be used for computations. The proposed design is a solution for implementations of QCA based circuits using minimum number of QCA cells, lesser clock delays and reduced area.



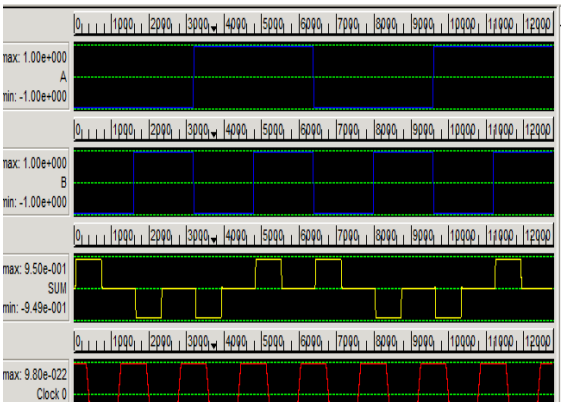
(a) (b)

Fig. 4: (a) QCA layout of F-shaped XOR gate (b) Simulation results

Fig. 4(c) is another efficient proposed XOR gate using universal NAND realizations. The simulations results of proposed design have been checked using QCADesigner tool shown in Fig. 4(d). The proposed layouts can be easily used to design complex circuits based on XOR operation like adder circuits, shift registers etc.



(c)



(d)

Fig. 4: (c)QCA layout of XOR gate with NAND gates (d) Simulation results

3.2 The proposed half adders

Digital computers perform various arithmetic operations. The most basic operation is the addition. The addition operation is achieved by majority logic that can reduce the overall number of gates required to create the adder circuits.

Researcher [17] has proposed the QCA implementation of half adder. The design needs either needs either coplanar crossovers or multiple layers to implement. The half adder is a combinational circuit that performs addition of two bits. It is designed conventionally by XOR and AND gates. When two inputs A and B are added, the Sum and Carry outputs are produced.

Truth table of half adder is shown in table 1(a).

QCA majority logic for half adder can be written as:

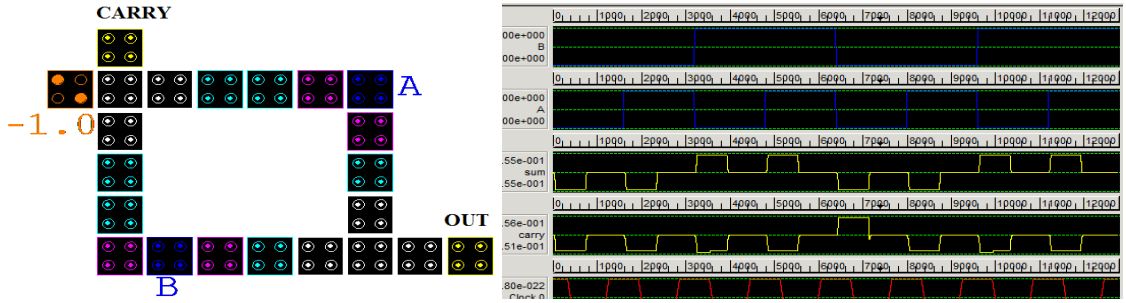
$$\text{Sum} = m\,(m\,(A', B, 0), 1)$$

$$\text{Carry} = m\,(m\,(A, B, 0)$$

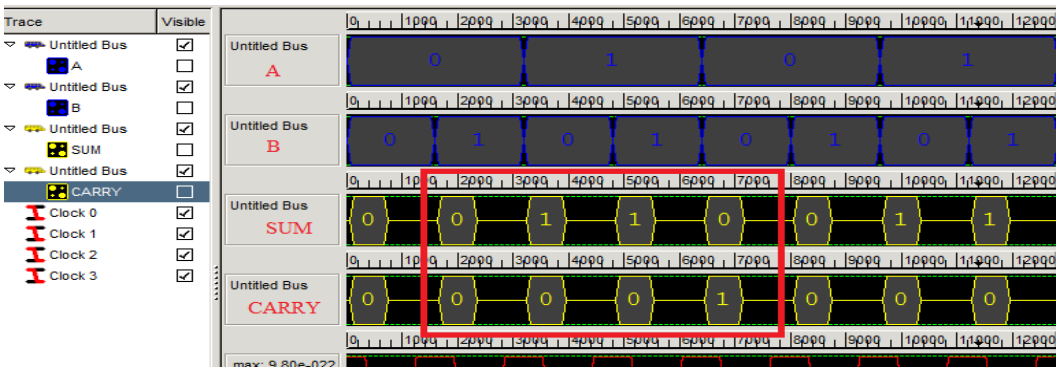
Table.1 (a): Truth table of half adder

A	B	SUM	CARRY
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

We have proposed a novel QCA half adder using F-shaped XOR gate as shown in Fig. 5(a). Simulation results of proposed designs shown in Fig. 5(b) & Fig. 5(c) have been checked using QCADesigner tool. Simplicity of the proposed half adder is using only one, AND gate. A proposed half adder consists of simple arrangement of QCA cells with proper clocking organization. The circuit area of half adder is 0.03um^2, latency 1, and circuit complexity is 22-cells.



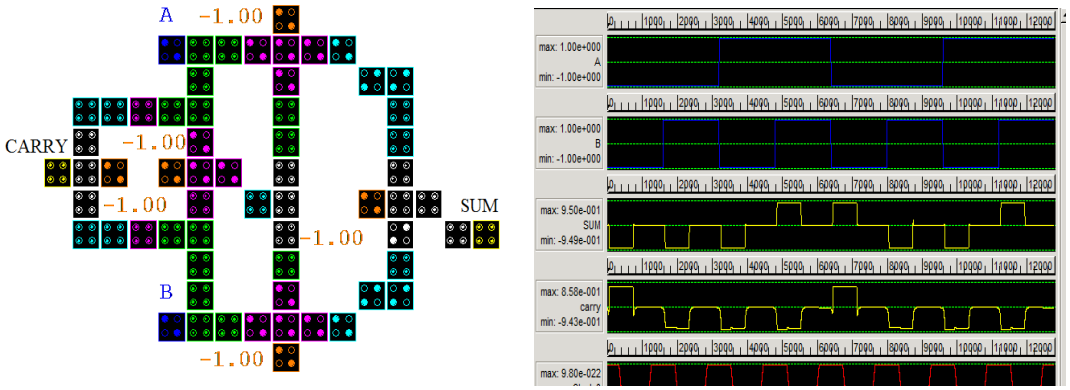
(a) (b)



(c)

Fig. 5: (a) QCA layout half adder (b) & (c) Simulation results

QCA layout of other half adder is shown in Fig. 5(d). The simulation result of half adder is shown in Fig. 5(e). Logically, the half adder operation can also be implemented using majority gates. The circuit area of half adder is 0.08um^2, with complexity of 62-cells



(d) (e)

Fig.5: (d) QCA based half adder (e) Simulation results

3.3. The proposed half subtractors

The half subtractor is a combinational circuit that is used to perform subtraction of two bits. It has two inputs, A (minuend) and B (subtrahend) and two outputs D (difference) and B (borrow), the truth table of half subtractor is shown in table 2(a).

The majority logic function for half subtractor can be written as:

Borrow = m (m (A', B, 0), 1)
Difference = m (m (A', B, 0)

Table 2 (a): Truth table of half subtractor

A	B	DIFFERENCE	BORROW
0	0	0	0
0	1	1	1
1	0	1	0
1	1	0	0

QCA layout of novel half subtractor using F-shaped XOR gate is shown in Fig. 6(a). The simulation results of half subtractor are shown in Fig. 6(b) & (c). We have using simple way to design half subtractor with proper clocking origination and consist of less area 0.03um^2. Dotted line in the Fig. 6(a) shows using two-cell inverter.

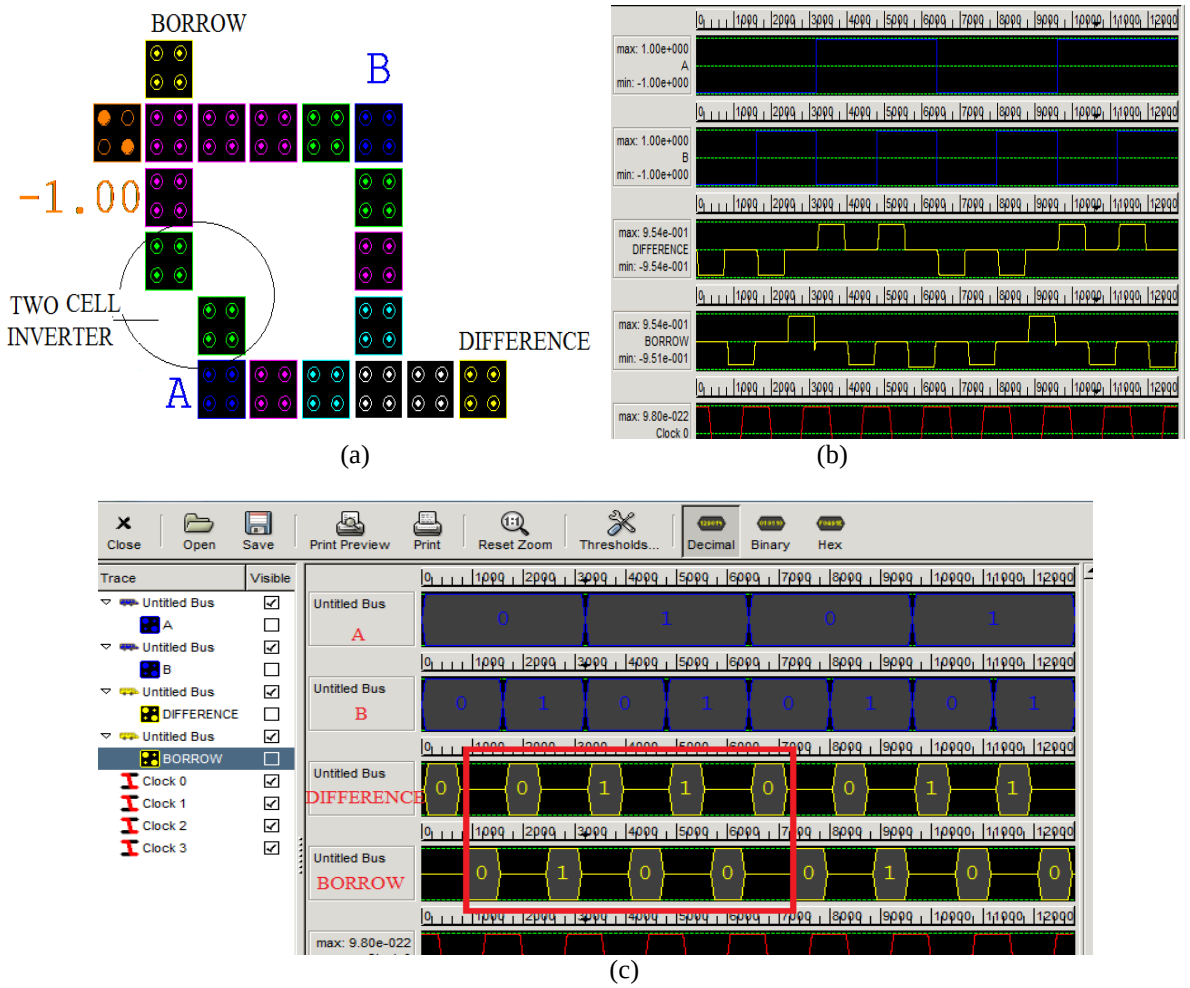
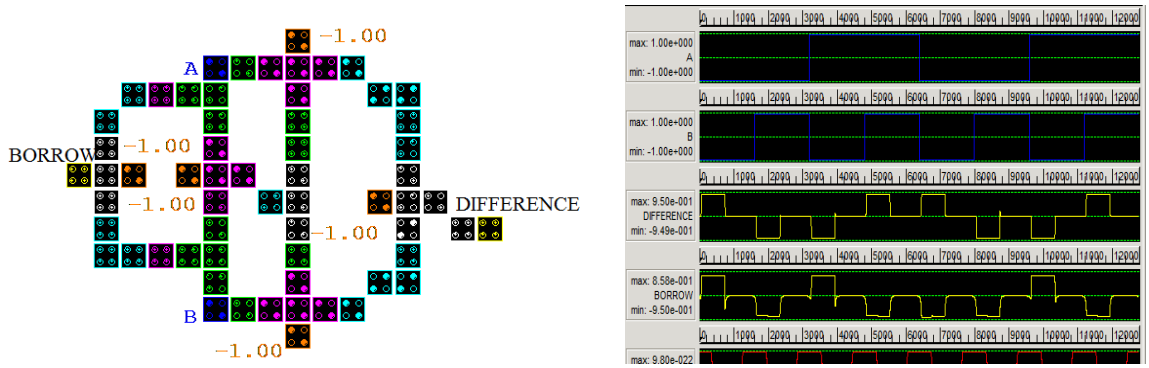


Fig. 6: (a) QCA layout half subtractor, (b) & (c) Simulation results.

The proposed QCA layout of half subtractor using basic majority gates is shown in Fig. 6(d). Simulation result of proposed design is shown in Fig. 6(e). The layouts have been designed to provide the more efficient configurations in terms of circuit complexity. Logically, the half subtractor operations have been implemented by using majority gates. The circuit area of proposed half subtractor is 0.08um^2 and circuit complexity is 62-cells.



(d) (e)

Fig. 6: (d) QCA based half subtractor (e) Simulation results.

IV. Performance Table of Logic Structures

The comparative study of proposed structures is shown in performance table 3(a). It is evident from table 3(a) the proposed designs are efficient in terms of cell count, area and circuit complexity.

Table 3 (a): Comparative study

	Previous Structures				Proposed Structures		
QCA Structures	Complexity	Area	Latency		Complexity	Area	Latency
XOR gate [9]	34 cells	0.06 um^2	1	Fig. 4(a)	12 cells	0.01um^2	1
[11]	35 cells	0.04 um^2	0.4	Fig. 4(b)	49 cells	0.07 um^2	2
Half adder [16]	77 cells	297x280 nm^2	1	Fig. 5(a)	62 cells	0.08 um^2	2
				Fig. 5(d)	22 cells	0.03 um^2	1
Half subtractor	Not applicable			Fig. 6(a)	62 cells	0.08 um^2	2
				Fig. 6(d)	19 cells	0.03 um^2	1

V. Conclusion

The proposed designs are a solution for implementations of QCA based circuits using minimum number of QCA cells, lesser clock delays and reduced area. This paper has demonstrated the design of improved QCA F-shaped XOR gate and its implementations as novel half adder and half subtractor circuit structures, which will be useful as an efficient building block for larger arithmetic units. The proposed designs are a solution for minimum number of QCA cells. The simulation results are compared with existing methods and are tabulated. The proposed layouts, occupies less area, and enjoys superior performance. Simulation results have been checked using QCADesigner tool. This research work is an attempt to find an optimal, way of realizing combinational circuits designed from a simple QCA based F-shaped XOR gate.

References

[1] R.Compano, L.Molenkamp, D.J.Paul, Technology roadmap for nano electronics. in: Proceeding of the European Commission IST Programme, Future and Emerging Technologies, Conference 1999.
[2] S. Timarchi, K. Navi, IEEE Trans. On Instrumentation and Measurement, Vol. 58 Issue: 9, PP-2959-2968 2009.
[3] W. Wang, K. Walus, G.A. Jullien, Quantum-Dot Cellular Automata Adders, Proceedings of third IEEE Conference Nanotechnology. 461–464, 2003.
[4] Sen. Wang, Li. Cai, Novel exclusive-OR gate and full adder implementation using quantum cellular automata, Solid-state phenomenon. 565–569, 2007.
[5] V. Vankamamidi, M. Ottavi, F. Lombardi, Two-dimensional schemes for clocking/timing of QCA circuits, IEEE Transactions on Computer-aided Design of Integrated Circuits and Systems 27 (1), 34–44, 2008.
[6] S.Hu, M. Crocker, M. Niemier, M. Yan, G. Bernstein, "PLAs in quantum-dot cellular automata", Proceeding International Symposim VLSI. 242–247, 2006.
[7] P.D. Tougaw and C. S. Lent, "Logical devices implemented using quantum cellular automata," J. Appl. Phys., American Institute of Physics, vol. 75, pp. 1818-1824, 1994.
[8] A. Vetteth, K. Walus, V. S. Dimitrov, and G. A. Jullien, "Quantum-dot cellular automata carry-look-ahead adder and barrel shifter," in Proc. IEEE Emerging Telecommunications Technologies Conference, Dallas, TX, Sept. 2002.
[9] Fijany, N. Toomarian, K. Modarress, and M. Spotnitz, "Bit-serial adder based on quantum dots," NASA technical report, Jan. 2003.

[10] Mohammad Rafiq Beigh, Mohammad Mustafa, Firdous Ahmad, "Performance Evaluation of Efficient XOR Structures in Quantum-Dot Cellular Automata (QCA)", Circuits and Systems, 4, 147-156, 2013.
[11] Wani Shah Jahan, Peer Zahoor Ahmad, Peer M A3, Khan K A, " Circuit Nanotechnology: QCA Adder Gate Layout Designs, "IOSR Journal of Computer Engineering (IOSR-JCE), vol 16, PP 70-78, 2014
[12] K.Walus, Wei Wang and Julliaen et al, "Quantum Cellular Automata adders" in Proc IEEE Nanotechnology conf, vol 3 page461-463December 2004.
[13] K.Walus, Schulaf and Julliaen et al, "High level Exploration of Quantum Dot Automata" in Proc IEEE Nanotechnology conf, vol 2,page 30- 33 2004.
[14] C. G Smith, "Computational without current", science, 284:274, 1999.
[15] I. Amlani, A.O. Orlov, G. Toth, G.H. Bernstein, C.S. Lent, G.L. Snider, "Digital 7logic gate using quantum-dot cellular automata", Science 284 (5412), 289–291. 1999.
[16] C.S. Lent, P.D. Tougaw, "A device architecture for computing with quantum dots", Proceedings of the IEEE 85 (4), 541–557, 1997.
[17] S. Karthigai Lakshmi and G. Athisha, "Design and Analysis of Adders using Nanotechnology Based Quantum dot Cellular Automata," Journal of Computer Science 7 (7): 1072-1079, 2011.
[18] S.Karthigai lakshmi, G.Athisha, "Efficient Design of Logical Structures and Functions using Nanotechnology Based Quantum Dot Cellular Automata Design," International Journal of Computer Applications (0975 – 8887) Volume 3 – No.5, June 2010.
[19] P.D Tougaw and C.S Lent, "logical devices implementation using quantum dot cellular automata,"journal of applied physics, 75:1818, 1999.
[20] Vishnu Teja Ch, Satish Polisetti and K. Santhosh, " QCA based multiplexing of 16 arithmetic & logical subsystem-a paradigm for nano computing" ,3rd Annual IEEE- International conference on Nano/Micro Engineering Molecular System, Hainan Island, China, January 2008.
[21] P. Tougaw and C. Lent, "Logical devices implemented using quantum cellular automata," J. Appl. Phys., vol. 75, No. 3, pp. 1818–1825, 1994.
[22] My. Choi and Mi. Choi, "Scalability of globally asynchronous QCA (quantum-dot cellular automata) adder design," Journal of Electronic Testing, vol. 24, pp. 313–320, 2008.
[23] I.Hanninen and J.,Taka, "Arithmetic design on quantum-dot cellular automata nanotechnology," Workshop on Embedded Computer Systems Architectures, Modeling, and Simulation SAMOS, Samos, Greece, pp. 43–52, 2008.