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Empirical Study of 2-bit Fast Adder using Simon 2.0

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Abstract : *The present context of post CMOS era demands highly sophisticated low power consuming high speed novel integrated chips in nanometer region. SET (Single Electron Transistor) is eventually the highest priority indexed device that are to be incorporated largely in replacing today's CMOS transistors. Several attempts have been made so far in mobilizing SET in designing future electronic circuits. One such attempt is being reported here in the present work. The target is to model an SET digital 2-bit fast adder to augment the speed of the super computers or large processing systems. Authors, here, have emphasized in deliberately integrating SET logics to design the 2-bit fast adder. A comparative study is annexed to advocate the incorporation of SET in near future.*

I. Introduction

'Mesophysics', has been studied since long as it signifies vast scope of research in device physics as well as in numerical computations. Off late a shift has been envisaged in the field of electronic endeavors so that the use of empirical research in future models is maximized. In this regard 'ITRS roadmap' of 2003 [1] portrays the end of CMOS technology by the end of 2015. The possible elements of such catastrophic demolition of CMOS are-(1) What would be the minimum allowable channel length (2) What would be the minimum allowable gate oxide thickness (3) What would be the possible depletion depth. Besides, empirical study revealed that the leakage power increases up to 20% when the CMOS is scaled down below 100 nanometers. Last, but not the least, is the maximum heat generation that moves up to the temperature nearly equal to the surface of the sun. This is why the end of CMOS was inevitable.

Once the fear embraced in the mind of Researchers; Scientists from MIT came up with the idea of quantum electronics that possess numerous advantages. But, technological limitation, material limitation and other process related limitations shadowed the popularization of quantum electronics. Further technological shift was envisioned in the embryonic field of SET. SET is considered to be the most promising candidate of future electronics owing to its excellent merit of transferring one bit of information using one single electron or a very few electrons. On the other hand, SET possess the virtue of simplicity, robustness, non-volatility, non-vulnerable and high speed. Likharev [2] categorically demonstrated single electron box in the late 90s. This research attracted scientists worldwide although till 2005 no such highly recognizable research was reported. Then after researchers form USA, UK and USSR almost concurrently initiated SET based research. Japanese researchers moved one step further in obtaining logical synthesis of SET. By the end of 2008 several scientists started experimental application of SET logic devices. Indian scientists laid this research into a new horizon by incorporating SETs in replacing CMOS based VLSI, ULSI circuits [3-11].

Here, the authors have limited themselves in modeling SET based 2-bit fast adder or Ripple Carry Adder by integrating SETs into several subsections. The modus operandi of such adder has been equated with conventional 2-bit fast adder. Following section describes SET implementation along with its circuit diagram for nano IC modeling. SIMON 2.0 has been used as test bench to satisfy the logical reasoning of the circuit. Here the authors render to the earlier publications of Dr. J. Gope [12-22].

II. Implementation of SET 2-Bit Fast Adder Using SIMON

Fig.1 is the simple nano IC structure of SET 2-bit fast adder having inputs A_1,B_1,A_0,B_0, initial carry C_1, output S_0,S_1 and output carry C_1.

III. The Operational Maneuver

As depicted a ripple carry adder mimics the pencil and paper method of operation. The rightmost least significant digit position is the starting point. The two corresponding digits are further added to obtain the result. Possibly, a carry may be generated of any specific digit position. Accordingly, all digit positions except the rightmost holds the possibility of having an extra 1 i.e. adding an extra 1. This carry is nothing but is generated from the just next position to the right. It means that no digit position will have fixed absolute final value until it has been confirmed that a carry is coming or not from the right. To exemplify, the authors take up pencil and paper method as stated herein. 9+5=4 and carry 1. The sum without a carry is 9 in pencil and paper method or 1 in binary, it is somehow impossible to signify whether or not a given digit position is ready to pass on a carry to

the position on its left. Carry look ahead further depends upon calculating on each digit position-whether that digit position is supposed to propagate a carry from the right. Supposing that a group of four digits are chosen. Then sequentially the following steps take place:

The 1 bit adders calculate their results and simultaneously the look ahead units perform their own calculations. If a carry appears at a particular group within 5 gate delays, that carry will appear at the left hand end of the group and will start propagating through the group to its left. If that carry also propagates to the next group, the look ahead unit will control it. Similarly, when the particular carry emerges from the next group, the look ahead unit will convey the same to the next group that it will receive a carry and such propagates till the end.

IV. Comparative Study

As the Researchers tend to shrink the transistor size below 100 nanometers, the possible heuristic approach is integrating SET for logical synthesis. The three decisive factors that are primarily considered are power consumption, speed and size.

As the size is beneath 100nms, thus undoubtedly this size matter falls out of context when compared with existing CMOS technology. Empirical results revealed after simulating the model using SIMON 2.0 that the power consumption is less than 1/10th and the speed rises to 200 times faster when compared to conventional CMOS counterpart. The power dissipation is also low thereby heat generation is significantly avoided. The speed of IC as stated rises very high thereby the robustness of the model increases manifolds. Other factors like electron transport phenomenon substantiate the limitations of the conventional CMOS topology. Moreover, the cost of the device is anticipated to lessen down considerably during mass production. Henceforth, the author appraise the use of 2-Bit fast adder in future next generation high speed super computers large processing systems.

V. Conclusion

The circuit eventually attributes all the 'Figure of Merits' of nano-technology and the same has been withstand with great confidence by the authors. SIMON2.0 is an excellent platform to model and test the durability of the proposed designed specification. Convincingly the designed nano 2-bit is hereby designated as a super work horse for future VLSI/ULSI BASED supercomputers or large processing systems. Authors would like to tender this short communication as an alternative of the fragilities and limitations of CONVENTIONAL CMOS technologies only to sustain the gigantic growth of electronics industry keeping in view the MOORE'S LAW in past CMOS era.

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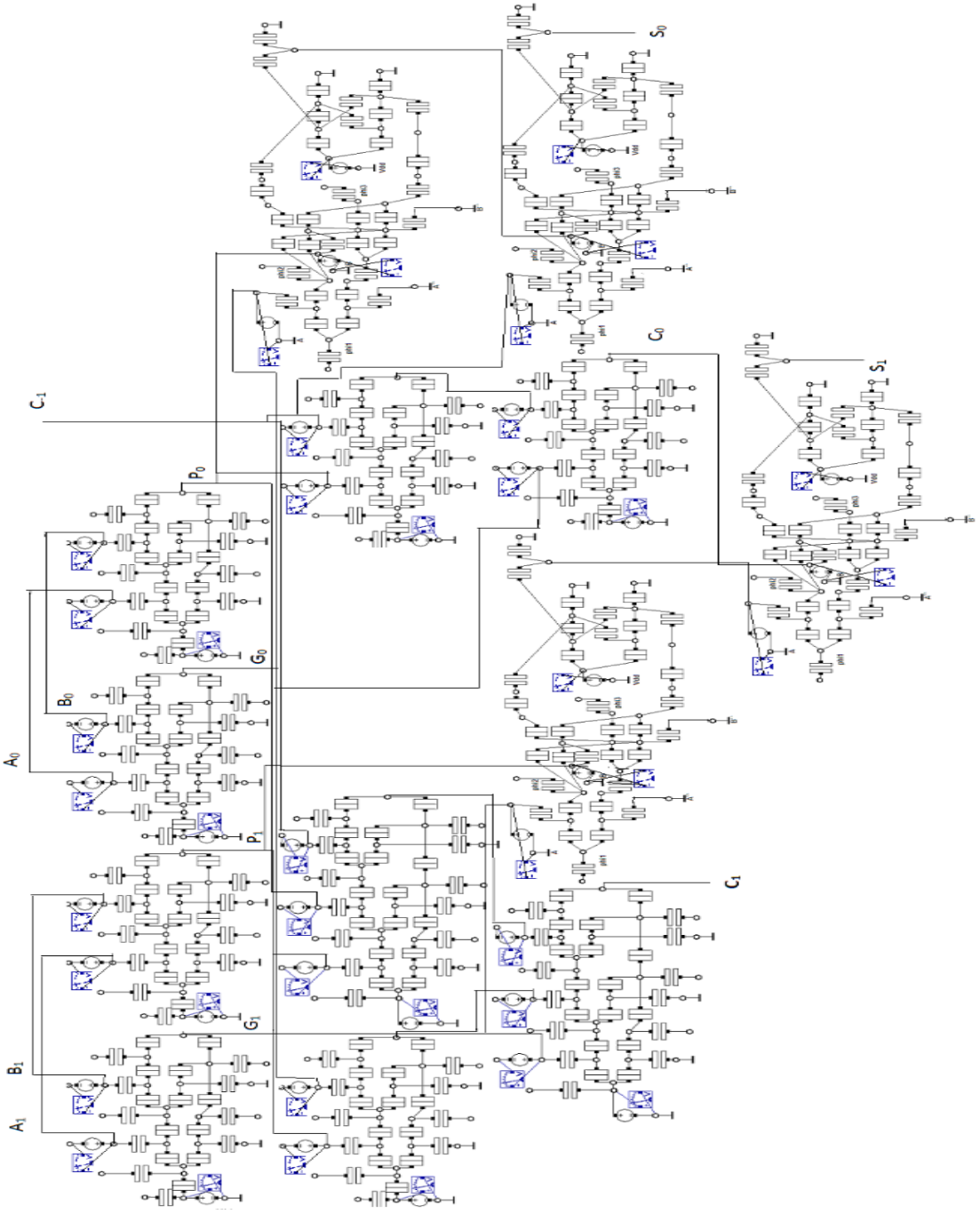

Fig.1: SIMON2.0 made SET 2-bit fast adder nano IC