

Real Time Zetta Bytes -Universal Memory ASIC SOC IP Core Design Implementation using VHDL and Verilog HDL for High Capacity Data Computing Processors like Cloud/Cluster/Super VLIW Parallel Distributing Pipelined Array Computing Processors

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Abstract: The main intention is RTL Design Architecture and HDL Design Implementation of Zetta Bytes Memory ASIC SOC IP Core for Advanced Parallel Array Distributed Pipelined Array Computing /Cloud Computing / Super VLIW Computing/Cluster Computing Processors/very High Big Data Control Stations /Servers , Arrays of Data Servers, Interfacing for All Advanced Real Time Smart Computing Products-wireless , telecom , consumer, advanced processor and controller IP cores, Aerospace/Avionics ,Automotive , Industrial Automation ,Hi-Fi applications. Design Coding Implementation Done by Verilog HDL and VHDL , Simulation and Synthesizing , FPGA Front End Design Flow Implementation Done By Xilinx ISE 9.2i Software. Programming & Debugging Done through Xilinx Virtex /Kintex-7 FPGA Development Board/Kit.

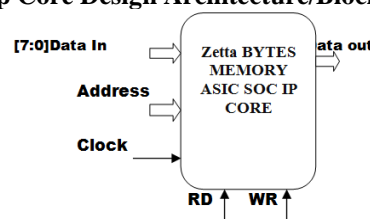
Keywords: Application Specific Integrated Circuit, FPGA – Field Programmable Gate Array, HDL – Hardware Description Language , ISE – Integrated Software Environment.

I. Introduction

In Modern electronics Memory Plays vital role in all advanced real time smart Embedded computing products and applications for keeping large storage of data of Big Big Data Centric Storage and controlling Applications like Stations and Servers, Cloud, cluster , Parallel Distributed Pipelined Array Processors Computing and large data Storage Servers and Racks and Network Array Processors Computing, Graphics and Large Data Image Processors Computing. Now I Designed Universal Memory IP ASIC SOC IP Core of Different Data bytes capacity- Zetta bytes capacity Memory IP Cores. The Memory SOC IP Core Store Large secure Big Data of Big MNC's/ Large Defense Sectors/Entire Major network and storage stations /cities etc. This memory IP Core is very suit for all Advanced ASIC.FPGA Development Boards . This memory IP Core is virtual type . This memory is very suit for future advanced applications and 6th Sense Products . This Memory ASIC Contain RTL Blocks of Zetta Bytes Memory Design Blocks. This Memory acts as a Universal IP Core for Both RAM and ROM Array Designs. This Memory Contains Chip Select CS Signal, Read and / Write Control Signal and Zetta Bytes Data. For **Zetta Memory -2⁷⁰** Data Bytes Storage Locations for advanced HIFI Real Time Smart-Computing-Industrial-Software-Applications /Products. These memories are purely clock dependent storage. This Memory Contains 8/16/32/64/128 Data Bit Storage Width for that I 'am using Registers for keeping temporary/Permanent storage of Data. The Main Intention of Designing the Universal memory SOC ASIC Soft IP Core is for At a time computing and running the functionality of multiple large big Data by based Control Stations/Servers /MNC's Servers by Partitioning Big Memory spaces using Parallel Array Distributed Computing Array Technique and Cloud/ Cluster Computing Technique using Single System on Chip Solution. This-Memory-suit-for-Interfacing-with Advanced Processor Boards of Mega /Giga /Tera /Peta /Exa /Zetta /Yotta /Xona /Weka/Vendica Bytes Capacity and Same Frequency Rate Baud rate Generators for Out rich Electronic Design Cards/SOC's .

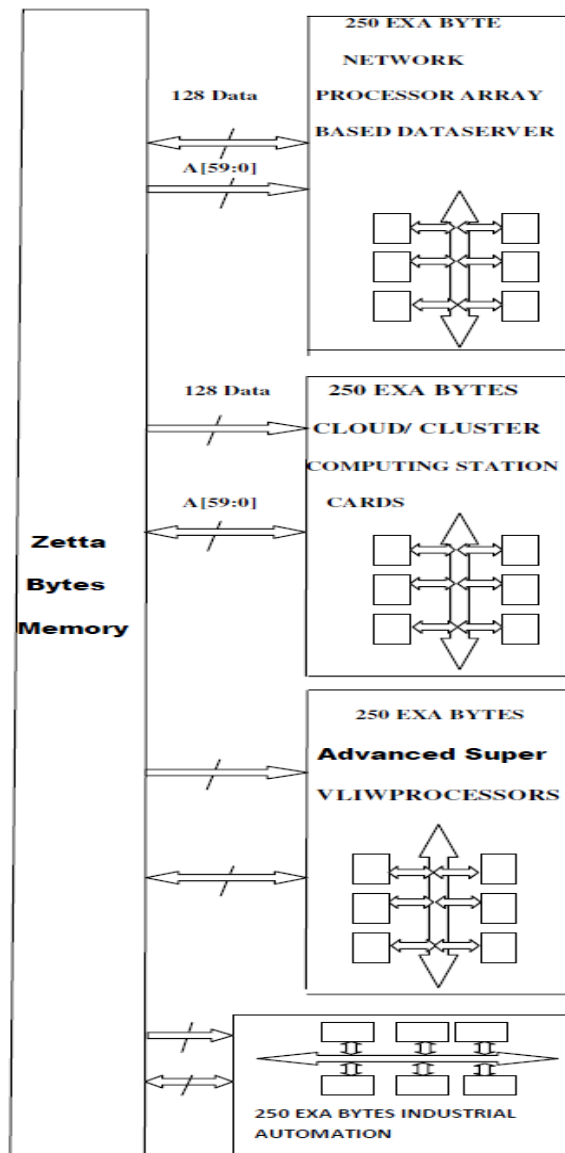
II. Zetta Bytes Memory Design Architectures

1.1 Zetta Bytes Memory Asic Soc Ip Core Design Architecture/Block Diagram



Fig(1). Zetta Bytes Block Architecture

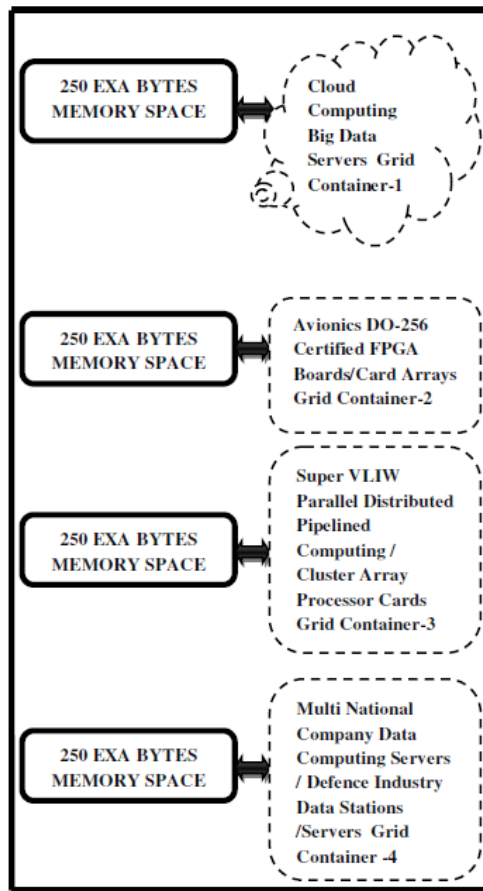
2.2 Zetta Bytes Memory Detailed Architecture



Fig(2). Detailed Memory Interface Partition Soft IP Core Architecture

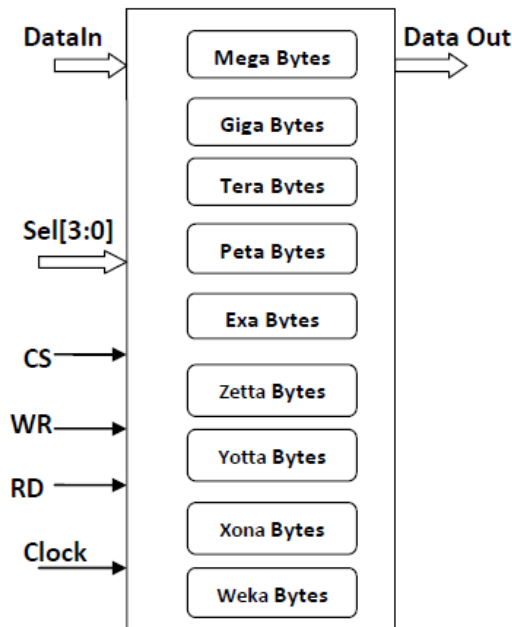
2.3 Description. Zetta Bytes Memory Partitioned Into four 250 Exa Bytes Memory. Each having 128 Bit DataBus and 60 bit Address bus and Each Exa byte Memory Allocated for Network Processor Array Based Data Servers Card , Cloud/Cluster Computing Station, Advanced Super VLIW Processor Array Cards, Industrial Automation Products / Application Cards. Each Share Data and Address through Data Bus and Address Bus. This is mainly Designed for Processing, Controlling, Maintaining Big/Large Secured Data . Splitting the Data in to Sub Data for Different Card Array Based Busses. And This Memory Running Large Data and Applications through Advanced VLIW Processor Instructions through Advanced Network Data Servers , Cloud/Cluster Computing Stations, Advanced Super VLIW Processor Array Cards for Running Long Instruction Words through Parallel Pipe Line Array Distributed Computing Array Technique like Fetch, Decode, Execute the Data Functionality in the Memory Partitioned Space. Simply These Are Executed through Pipelined Processors Cloud/Cluster Array Cards. Data Rate In terms of Zetta Bits Per Second through Zetta Hertz Clock. This Clock Synchronizes all Big Data Frames/Packets d Processing and Controlling. Data Processing in terms of Bytes, Frames, Super Frames, Super Very Long Word Frames for Highly Reliable Data Computing in these Memories. And Also other remaining 250 Exa Bytes Memory Space for Running the Applications / Products Industrial Automation Applications Real Time Smart Computing Applications like wireless and telecom protocols, Transceivers, Highly Reliable Consumer Electronic Smart Computing Products ,Image and Medical Diagnostic Products /Applications, Image and Graphics Processing and Computing w.r.t Clock Synchronization. This is simply Single System on Chip Card Solution.

2.4 zetta Bytes Memory System-Asic Soc Partitioned Interface Architecture



Fig(3). Zetta Memory System Partitioned Software IP Core Architecture

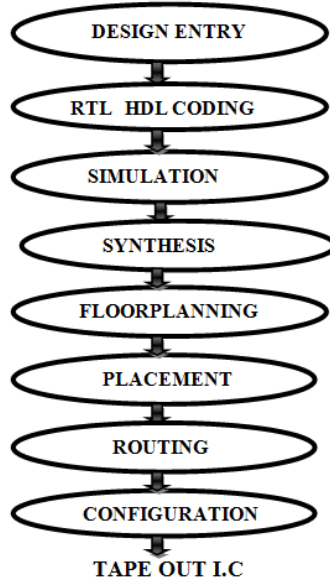
2.5 Universal Memory Asic Soc Ip Core Detailed Architecture/Block Diagram



Fig(4).Detailed Architecture Universal Memor Asic Soc

2.5.1Description. This Soft IP Core Universal Memory Chip Contains Different Data Byte Memorieslike Mega,Giga,Tera,Peta,Exa,Zetta,Yotta,Xona,Weka,Vendica Bytes Capacity for Processing, Storage, Controlling, Distributed Large Computed Big Data Applications/Products

III. Software – V.L.S.I I.C Design Flow

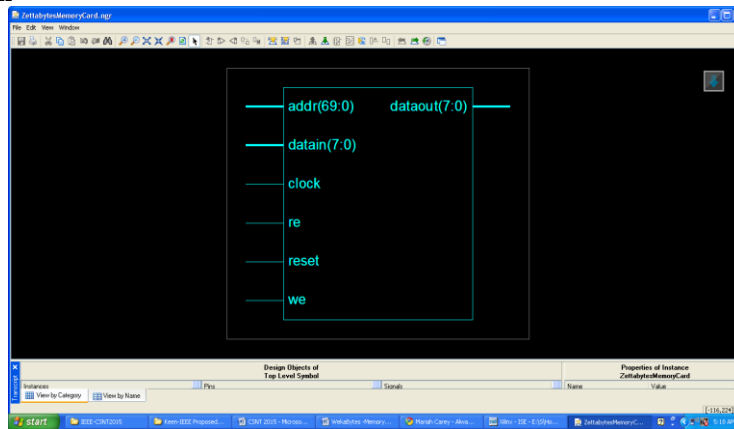


Fig(5).VLSI Design Flow Chart $2e^{23}$ -1 E.b.p.s P.R.B.S A.S.I.C I.P CORE

Description. The Design Process and Implementation Done by the above V.L.S.I Software Design Flow Chart Phases. It Consists Design Entry Specifications , R.T.L H.D.L Coding (V.H.D.L and Verilog H.D.L) and R.T.L Logic Simulation and R.T.L Synthesis and Floor planning, Placement and Routing of $2e^{23}$ -1 E.b.p.s P.R.B.S A.S.I.C I.P CORE Implementation Done by Xilinx FPGA Synthesis Software (X.S.T)

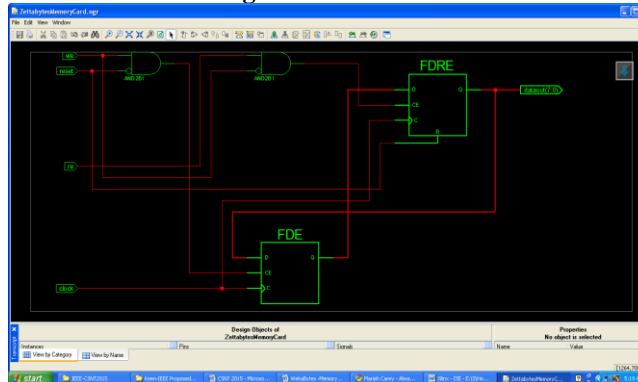
IV. Fpga Design Flow Reports

4.1 Rtl Design Block



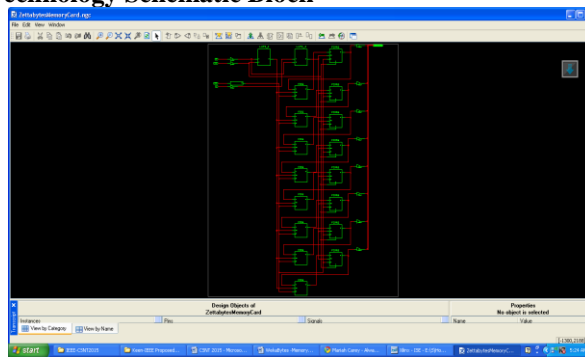
Fig(6). Zetta Bytes Memory RTL Design

4.2 Zetta Bytes Memory RTL Schematic Design Block



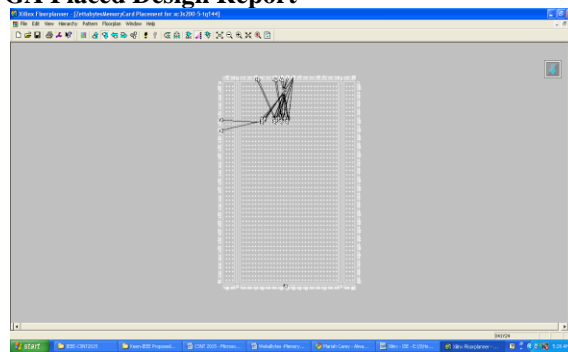
Fig(7).Zetta Bytes Memory RTL Schematic

4.3 Zetta Bytes Memory Technology Schematic Block



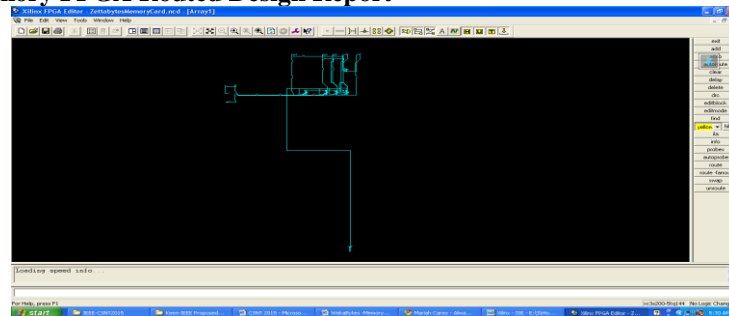
Fig(8). Zetta Bytes Memory Technology Schematic

4.4 Zetta Bytes Memory FPGA Placed Design Report



Fig(9). Zetta Bytes Memory FPGA Placed Design Report

4.5 Zetta Bytes Memory FPGA Routed Design Report



Fig(10). Zetta Bytes Memory FPGA Routed Design Report

IV. Hdl Synthesis Report

Macro Statistics

# Registers	: 2
8-bit register	: 2

Final Register Report

Macro Statistics

# Registers	: 16
Flip-Flops	: 16

Final Report

Number of Slices: 9 out of 1920 0%
 Number of Slice Flip Flops: 16 out of 3840 0%
 Number of 4 input LUTs: 2 out of 3840 0%
 Number of IOs: 90
 Number of bonded IOBs: 12 out of 97 12%
 Number of GCLKs: 1 out of 8 12%

TIMING REPORT

RTL Top Level Output File Name :

ZettabytesMemoryCard.ngr

Output Format : NGC

Optimization Goal : Speed

Keep Hierarchy : NO

Design Statistics

IOs : 90

Cell Usage :

BELS : 2

LUT2 : 2

Flip-flops/Latches : 16

FDE : 8

FDRE : 8

Clock Buffers : 1

BUFGP : 1

IO Buffers : 11

IBUF : 3

OBUF : 8

Device utilization summary: Selected Device : 3s200tq144-5

Number of Slices: 9 out of 1920 0%
 Number of Slice Flip Flops: 16 out of 3840 0%
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TIMING REPORT

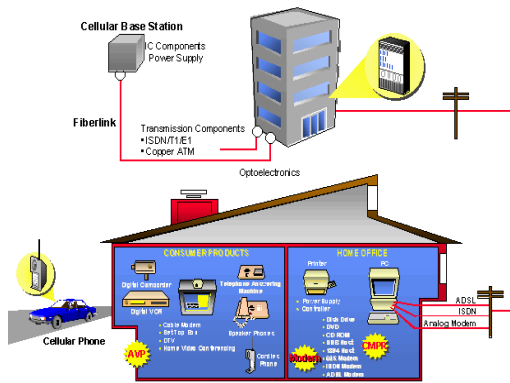
Timing Summary:

 Speed Grade: -5
 Minimum period: 1.547ns
 (Maximum Frequency: 646.224MHz)
 Minimum input arrival time before clock: 3.889ns
 Maximum output required time after clock: 6.280ns
 Timing constraint: Default period analysis for Clock 'clock' Clock period: 1.547ns (frequency:
 646.224MHz)
 Total number of paths / destination ports: 16 / 16
 Total memory usage is 143912 kilobytes
 Reconfiguration/ FPGA Programming Window



V. Real Time Live Applications

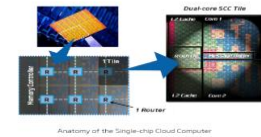
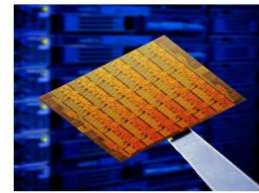
PC-Multimedia Applications



Single-chip Cloud Computer



Intel Labs has created an experimental "Single-chip Cloud Computer" (SCC) a research microprocessor containing the most Intel Architecture cores ever integrated on a silicon CPU chip - 48 cores. It incorporates technologies intended to scale multi-core processors to 100 cores and beyond, such as an on-chip network, advanced power management technologies and support for "message-passing". Architecturally, the chip resembles a cloud of computers integrated into silicon. The novel many-core architecture includes innovations for scalability in terms of energy-efficiency including improved core-core communication and techniques that enable software to dynamically configure voltage and frequency to attain power consumptions from 1.25W to as low as 25W.

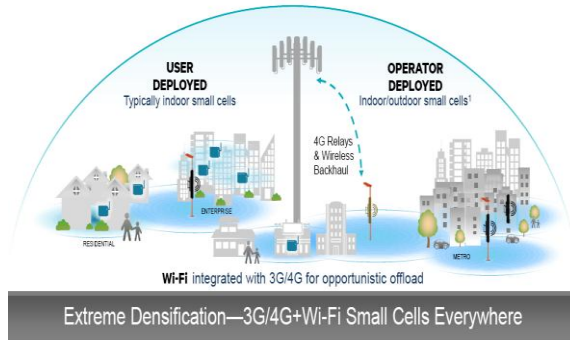


Inside the Single-chip Cloud Computer

The name "Single-chip Cloud Computer" reflects the fact that the architecture resembles a scalable cluster of computers such as you would find in a cloud, integrated into silicon.

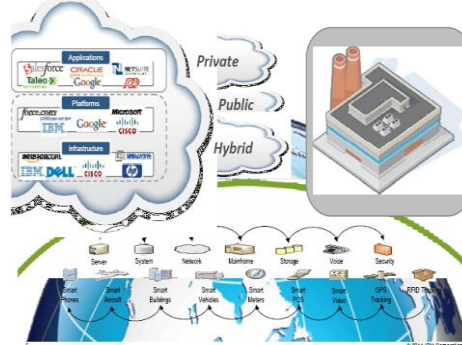
- The research chip features:
- 24 "tiles" with two IA cores per tile
 - A 24-router mesh network with 256 GB/s bisection bandwidth
 - 4 integrated DDR3 memory controllers
 - Hardware support for message-passing

Bringing the network closer to the user is key to 1000x



Deployment Choices

It's an interconnected world...and includes more than just applications



Enabling a superior **video** experience
Driving 4K video with mobile

Four times more detail than Full HD 1080p

Expanded color gamut for accurate colors

Crisp text and graphics

Phone, tablet and TV share content

iCloud

SD Full HD 4K UHD

Highly Integrated Consumer Products

VI. Conclusion

Zetta Bytes Memory Designed for Large Computing Data Stations like Servers/Cloud Computing, Advanced VLIW Parallel Distributed Computing Processors, High Speed Industrial Data Automation Systems.

Bibliography

M.S(E.C.E)(A.U),M.Tech(E.C.E), (PhD)-ECE(JNTUH), PG Dip. VLSI(I.S.O.U.K ,B'lore)

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