IOSR Journal of Computer Engineering (IOSR-JCE)
e-ISSN: 2278-0661,p-ISSN: 2278-8727, Volume 21, Issue 2, Ser. II (Mar - Apr 2019), PP 11-22
www.iosrjournals.org

Design and simulation of a Tristate Buffer circuit in Quantum Dot Cellular Automata

Ratna Chakrabarty[1], Niranjan Kumar Mandal[2]
[1] *Department of Electronics Engineering, Institute of Engineering & Management, Salt Lake, Sector-V, Kolkata, India*
[2] *Department of Electrical Engineering, University of Engineering & Management, India*
Corresponding author: [*] Ratna Chakrabarty

Abstract
Quantum dot Cellular Automata (QCA) is an emerging technology that offers a radical change in the design era at nano-level. QCA based design is advantageous over macro level for its extremely low power requirement, high packaging density and high speed of operation. QCA is a suitable replacement of semiconductor based transistor and CMOS technology. This paper proposes a new approach towards QCA based nanotechnology design with an input controlled Tri state buffer circuit of Fan out of three logic gates. The paper comprises the explanation about power dissipation of a QCA cell and energy calculations for the designed circuit. Robustness of the buffer circuit is verified by displacement of an important cell known as device cell. In majority voter device cell transfers the input information to the output. All the simulations and design has been done using QCADesigner tool.
Keywords: *QCA, Majority Voter, NAND gate, NOR gate, Fan out, Robustness.*

Date of Submission: 26-02-2019 Date of acceptance: 12-03-2019

I. Introduction

Semiconductor CMOS technology is useful when it is used as a current switch to send the digital information in electrical form. To send the binary information by just switching on and off the current switch is a novel one, but it has some serious drawback when the size of the device is reduced as then the quantization of charge in both the doping level and in channel level become very significant one according to [1]. Physical limits of using the CMOS devices have been successfully overcome in nanoscale level from the concept proposed in [2-4] which offers a solution at nanoscale level with a new method of computation and transformation of information. Authors showed transfer of the charge potential without the electron motion within a quantum cell. Metal dot and semiconductor dot QCA cell arrangement and the fabrication is explained in the papers [5-7]. QCA cell is composed of four metal dots with tunnel junctions and capacitors where switching of a single electron in a cell can control the position of the next cell electron by basic law of Coulomb repulsion. Logical behaviour of this kind is described in [8]. It has been explained that room temperature operation is possible if QCA cells are fabricated in 5 nm or less in size. Authors in [9, 10, 11] proposed such concept in molecular QCA. It describes the progress toward making QCA molecules at a tiny level to operate at room temperature.

In this paper an input controlled Tri state buffer circuit is developed using Quantum dot Cellular Automata. The circuit is verified with Fan out of three other logic gates. The designed circuit operates correctly up to temperature variation of 13 degree Kelvin for semiconductor QCA. Robustness of the circuit is tested by varying its device cell of majority gate which is the basic design of any QCA based logic design.

The paper is organized as follows, basic introduction is given in section 1, section 2 describes the principles of operation of quantum Dot based cell, section 3 describes the Tri state buffer in digital circuits and section 4 describes the previous design of universal logic gate in QCA. Section 5 describes Tri state buffer using QCA, its design and simulation. Section 6 shows the effect of Kink Energy and energy dissipation of the QCA based circuits. Section 7 checked robustness of the circuit by misplacement of device cell. Section 8 concludes the paper.

II. Logical devices in Quantum Dot Cellular Automata

A QCA cell consists of four metallic dots positioned in four corners of a square quantum cell. Each cell has two mobile electrons, which carry the charge information from one cell to another according to the position of electrons in the dots due to mutual Columbic repulsion. The information in QCA flows without the electron movement from one cell to another cell with lowest energy state as explained in [12]. Fig. 1 shows the

polarization of quantum cell according to the electron position in the quantum dots of that particular cell. Polarization is given by the following equation.

$$P = \frac{(P1+P3)-(P2+P4)}{P1+P2+P3+P4}$$

When P=+ 1 it indicates 1 and 3 position has extra electrons and when P= -1 it mean occupancy of electron in 2 and 4 position. The mutual coulomb repulsion between the electrons thus results in bi-stability between the P = +1 and P = -1 states.

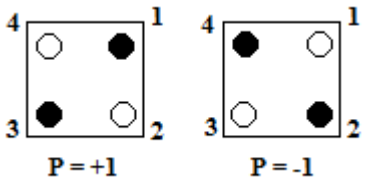


Fig. 1 Quantum cells with four dots and polarization of P= +1 and P= -1.

2.1 Majority Gate in QCA

Three input majority voter device is the basic of QCA based logic circuit as shown in Fig. 2. The majority gate [13] is used to build the fundamental logic AND gate and logic OR gate. Majority input changes the orientation of the device cell to its lowest energy state.

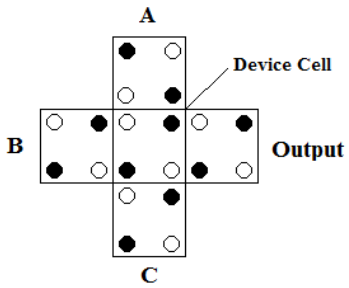


Fig. 2 Majority Gate in QCA

In a majority voter circuit let A, B and C are the three inputs and Y the output, the logical function for the majority voter gate circuit is given by –

$$Y = AB + BC + AC \qquad (1)$$

One input among A, B, C in logic 0 gives the AND function. Similarly, the OR function can be set by giving logic 1 to the one input among A, B, or C in equation 1. Thus the results of operations are as below the equations:

$$\text{AND} \rightarrow AB + B\,(0) + A\,(0) = AB$$
$$\text{OR} \rightarrow AB + B\,(1) + A\,(1) = A + B$$

Here input C is taken as zero input for AND operation and if it is taken as one input it will work for OR operation. This is done in QCADesigner tool with the cell function operation by changing its fixed polarization. With this property i.e. the ability to generate the AND and OR functions, any logical circuit can be generated with QCA devices. Fig. 3 shows the majority OR and AND gates.

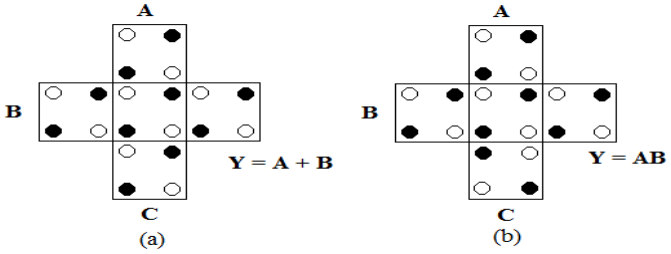


Fig. 3 (a) Majority OR gate with P=+1 in C input. (b) Majority AND gate with P= -1 in C input

2.2 QCA Wire

QCA wire [14-15] is framed by arranging the cells in a length as shown in Fig. 4. Charge transfer occurs from left-to-right in the following wire because of the Columbic interactions between the cells.

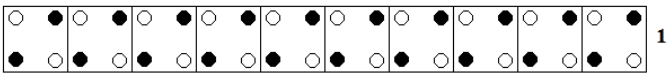


Fig. 4 Binary wire in QCA

2.3 QCA Inverter

In logic circuits, an inverter means which sense the logic signal and gives the output in opposite manner. A low signal input through an inverter results in a high output and vice versa. By arranging array of cells, as shown in Fig. 5, an inverter in QCA can be constructed.

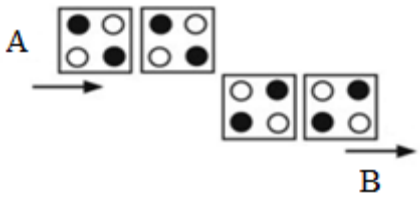


Fig. 5 An Inverter circuit in QCA

2.4 QCA Clocking Phenonmenon

Basic feed of QCA based circuit is the clock signal [16-18]. Information propagated through the circuits by the use of proper implementation of the four phased clock signals. QCA does not need any extra power to operate other than the clock signal as shown in Fig 6. An electric field is created by CMOS or carbon nanotube which is buried under the QCA circuitry. The field operates here for raising or lowering the tunneling barrier of a QCA cell. When the barrier is high cell does not allowed changing the state, it is then polarized. Adiabatic switching is achieved by lowering the barrier. It then transfers the input information to the next cell by erasing the previously stored information. It is a non polarized state. Switch, hold, release and relax states are defined as four clocking zones of a clock signal is shown in the following figure. In switch phase inter dot potential barriers are low and QCA cell become polarized according to the state of its input driver. In the second phase named as hold phase of clocking where barriers are still high and does not allow the electron tunneling and output of this state is used as the inputs to the next. Potential barrier is lowered in the release phase and electron positions are configured according to the original state. The cells are relaxed or unpolarized in the fourth clocking phase.

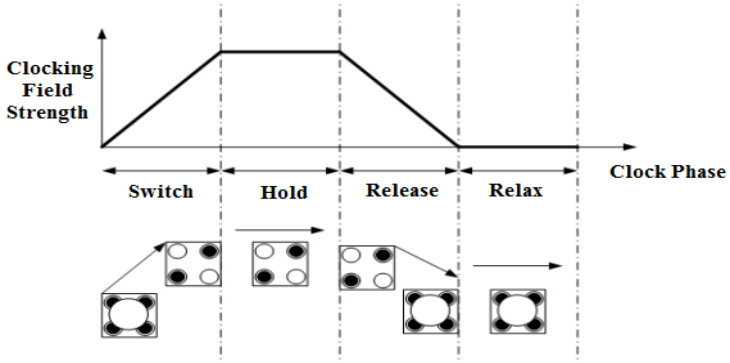


Fig. 6 Four clocks phases in the QCA cell.

III. Tristate Buffer In Digital Circuits

Tri state buffer is a type of circuit whose output can be controlled by controlling the input. The gate is known as 3 State Buffer or a Tri-state Buffer for its three possible output states. Tristate mean logic "0" or a logic "1" output and third state allowing its output in high impedance state.

A Tri-state buffer needs two inputs. One is the data input and the other the control input. The Fan out phenomenon in digital circuit is the output driving capability.
In a logic circuit design output of a logic gate depends on the inputs of other gates so the additional gate connections add to the load of the gate. Fan out is defined the number of parallel gates or loads that can be driven simultaneously by one digital circuit. If a digital buffer has a high fan out rating it must have high fan in rating as well which causes propagation delay of the output. This deteriorates the performance of circuit so fan in of less than 4 gates are usually preferred.
A Tri state Buffer or tri state output driver can be used where the applications need to decouple the gates from each other. Common digital logic buffer circuit is shown in Fig. 7.

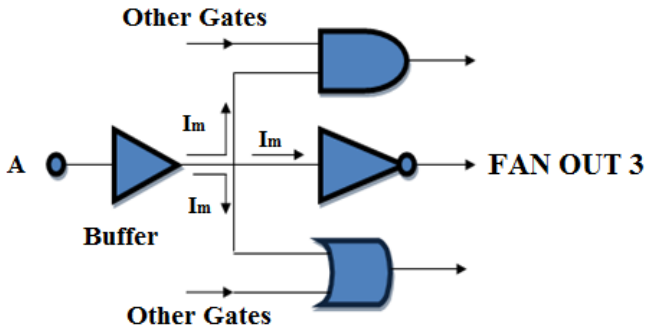


Fig.7 Digital Buffer with Fan out 3

IV. Universal Logic Gate Using Qcadesigner

NAND and NOR gates are known as universal logic gates which are commonly used for designing various sequential and combinational circuit design in digital electronics. Using layering approach the design idea of universal logic gates in Quantum Dot Cellular Automata was developed in [19] earlier and used in various circuits afterwards in QCA domain. In this paper these gates are used for the circuit design. Fig. 8 shows the NAND and NOR gate design in QCA using two layers considering the radius of effect between the cells used in layers.

NAND Logic = UG (A, B, +1);
NOR Logic = UG (A, B, -1); Where UG = Universal Gate, +1 or -1 are polarization in the new layer cell.

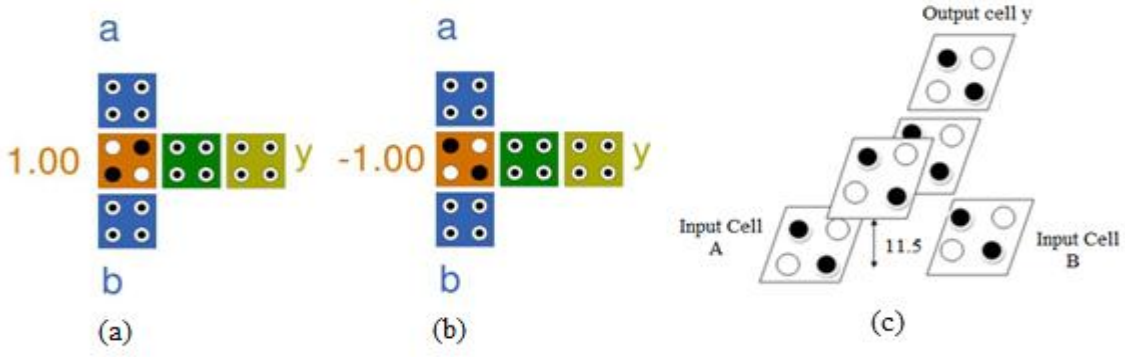
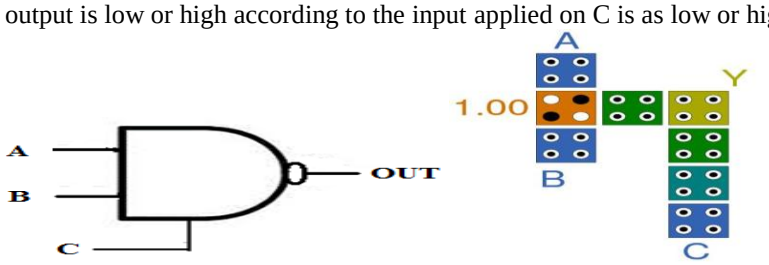


Fig. 8 (a) NAND Gate. (b) NOR Gate. (c) Layer configuration for the construction of the gates

V. Tristate Buffer in quantum DOT cellular automata

In QCA the design of Tri State buffer is similar to digital electronics. Fig. 9 shows the basic design of a Tristate buffer in QCA using NAND gate. Fig. 10 shows the corresponding simulated output. Fig. 11 shows the output when high impedance state of the circuit is taken. In the design QCA cells named as A and B are taken as the inputs and the cell C is taken as the control input. The circuit works as follows, when Control input C is in clock 2 and rest cells are in clock 0 or in active state the device works as NAND gate when input C is in logic 0. When input cell C is given an input as logic 1, output stays in high state. From Table 1 it shows that the buffer circuit designed in QCA domain is fully controlled by the clock signal implemented on control input C. When cell C is in clock zero output is low or high according to the input applied on C is as low or high.



(a) (b)

Fig. 9 (a) Tristate buffer using NAND gate symbol in digital electronics (b) Tri state buffer using QCADesigner tool.

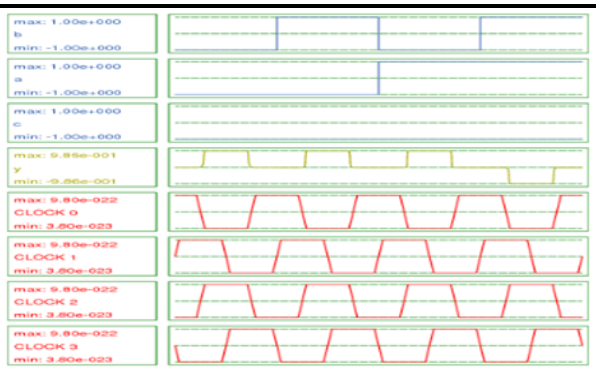


Fig. 10 Simulated output of Tri state buffer using NAND gate

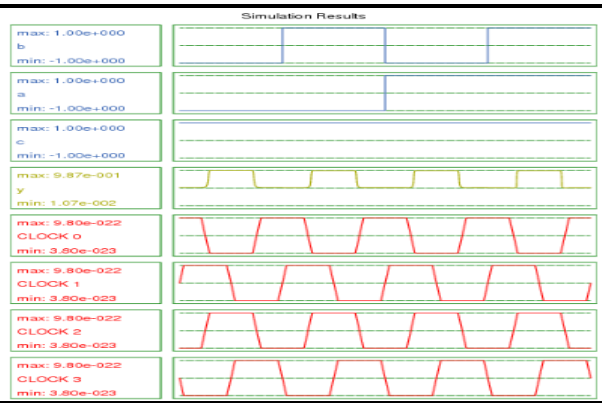


Fig. 11 Simulated output of Tri state buffer with high output state

Table 1 Low & High outputs from Tristate buffer circuit when C is in clock2 & clock0 respectively

	INPUTS			OUTPUT	INPUTS			OUTPUT
Input C is in Clock 2	**A**	**B**	**C**	**Y**	**A**	**B**	**C**	**Y**
	0	0	0	1	0	0	1	1
	0	1	0	1	0	1	1	1
	1	0	0	1	1	0	1	1
	1	1	0	0	1	1	1	1
	NAND gate output from Tristate buffer circuit with logic inputs when input cell C is taken as 0 in clock 2.				High output from Tristate buffer circuit when input cell C is taken as 1 in clock 2.			
Input C is in Clock 0	**A**	**B**	**C**	**Y**	**A**	**B**	**C**	**Y**
	0	0	0	0	0	0	1	1
	0	1	0	0	0	1	1	1
	1	0	0	0	1	0	1	1
	1	1	0	0	1	1	1	1
	Low output from Tristate buffer circuit when C is in clock zero with low input.				High output from Tristate buffer circuit when C is taken as 1 in clock zero.			

Fig. 12 shows a NAND gate circuit used as load is connected to the output of the buffer circuit. Y is the buffer circuit output and X is the output of cascaded with NAND gate. If the control input is in clock 2 it gives correct output for NAND operation if C is taken as low input. Fig. 13 shows the corresponding simulated output. Fig. 14 shows the design of Tri state buffer circuit with three other output connections as NAND, NOR and Inverter gate. The output ports named as X, W and Z are for NAND, Inverter and NOR gate output. Fig. 15 shows the simulated output of the designed circuit. The device works here as Fan out of 3 logic gate devices with 28 cells and consumption of area is 0.04μm^2. Table 2a and Table 2b show the output of the designed circuit of Fig. 14.

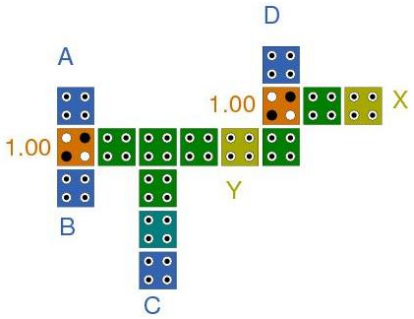


Fig. 12 Tristate buffer connected with NAND gate as one of its load.

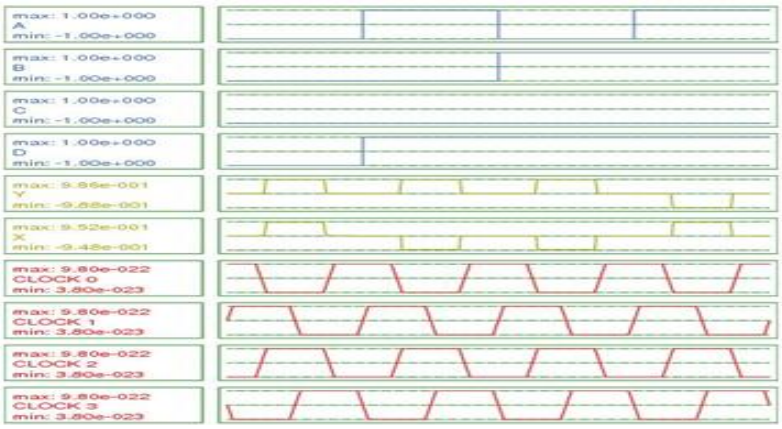


Fig. 13 Simulated output with NAND gate as one of its load.

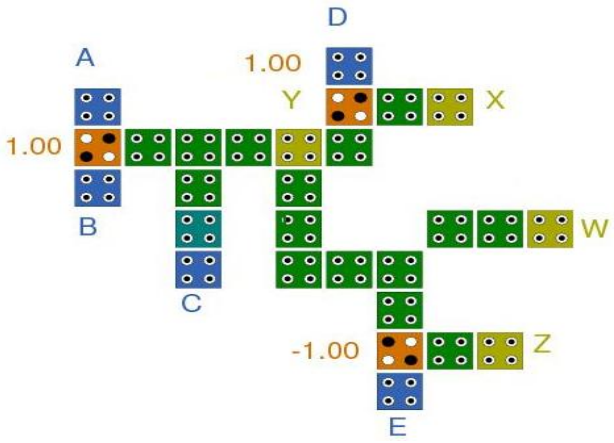


Fig. 14 Tristate buffer connected with NAND and NOR and Inverter gate as its load

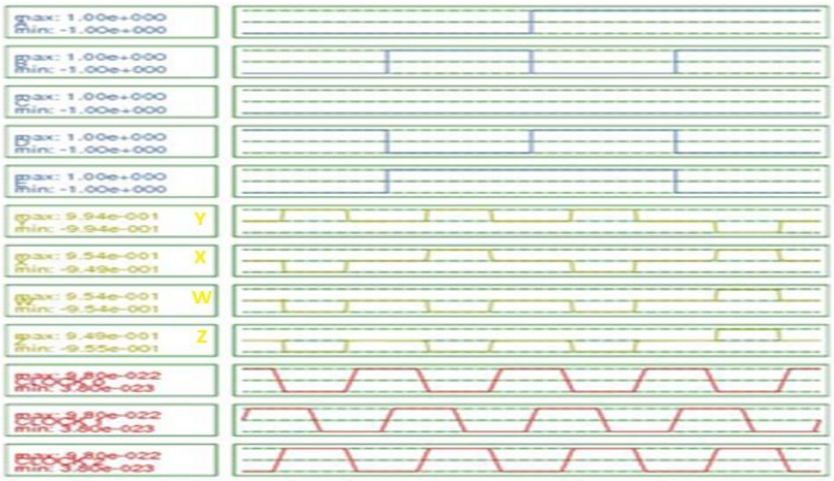


Fig. 15 Simulated output of Tristate buffer connected with NAND, NOR and Inverter gate as its load

Table 2a: NAND gate output from Fig. 14

A	B	Y (NAND output)	D	X (NAND gate output)
0	0	1	1	0
0	1	1	0	1
1	0	1	1	0
1	1	0	0	1

Here A and B are the inputs and C is the control input of the Tristate buffer circuit. Y the NAND gate output works as one input for the output connected as NAND gate. Here Y and D are the inputs for output X. Inputs E and Y are used for the NOR gate design and W the inverter output for Y as shown in table 2b.

Table 2b NOR gate and Inverter output from Fig. 14

Y	E	Z (NOR output)	$W = \overline{Y}$
1	0	0	0
1	1	0	0
1	1	0	0
0	0	1	1

VI. Effect of kink energy and energy dissipation in the designed circuit

In QCA error may occur in a cell due to clocking failure and it may affect then the neighboring cells output performance. Two polarized states in a QCA cell is determine as P=+1 and P= -1. Kink energy is defined as the energy cost of two neighboring cells having opposite polarization. This depends upon the cell spacing and cell diameter in the domain and not on the temperature acting upon it. Electrostatic interaction between two neighboring cell is defined as –

$$E^m = \frac{1}{4\pi\epsilon_0\epsilon_r}\sum_{i=1}^{4}\sum_{j=1}^{4}\frac{q\, i^m q j^k}{|\, ri^m - rj^k\,|}$$

Kink energy is calculated using the following calculation.

$$E_{kink} = E_{opp.polarization} - E_{samepolarization}$$

Kink energy is defined as follows for calculation

$$U = \frac{k\, q_1 q_2}{r}$$

U is the summation of kink energy as defined in [20]. All Circuit designs and simulations is done using QCADesigner tool [21].

The energy dissipation due to change in polarization can easily be computed from the equation as below [22]

$$E_{diss} \leq \left[\frac{2\gamma_{new}}{E_k}\left(\frac{p_0}{\bar{P}_{old}}\gamma_{old} - \frac{p_n}{\bar{P}_{new}}\gamma_{new}\right) + \frac{E_k \bar{P}_{new}}{2}(p_0 - p_n)\right]$$

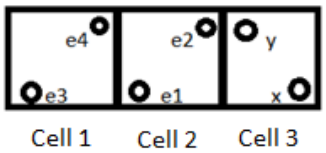


Fig. 16 (a) Three quantum dot cell and change in polarization is from 1 → 1 & 1 → 0

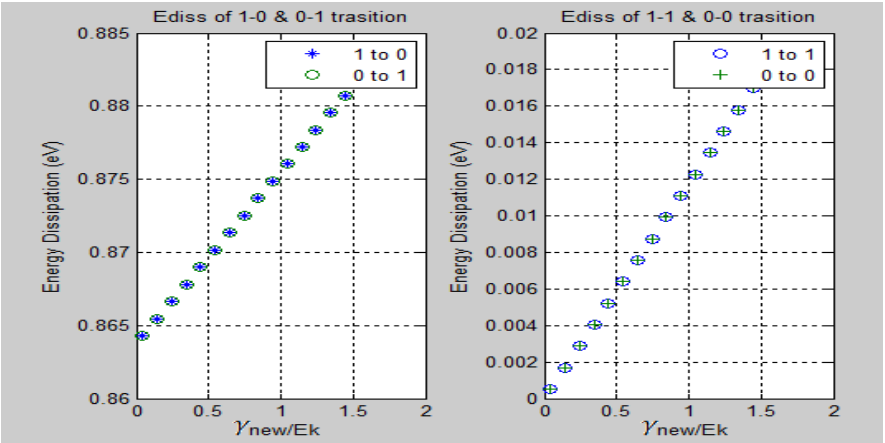


Fig. 16 (b) Energy dissipation between the two neighboring cells for different transition of polarizations from - (i) 1→0 (ii) 0→1 (iii) 1→1(iv) 0→0

Fig. 16(a) shows three quantum dot cell and it is considered the energy dissipation due to the transition of polarization from cell 2 to cell 3 i.e. polarization 1 → 0. If it is found E_{diss} with the given known parameters P_n =+1, P_o = -1, P_{old} = +1 and P_{new} = -1, the clock energy during switching event γ_{new} & γ_{old} are same, then E_{diss} will be equal to the kink energy between the three cells.

The total energy dissipation between the cells changes when the clock energy supplied to the cell is increased from 0.05E to 2E for different state transitions from 1 to 0, 0 to 1, 1 to 1 and 0 to 0 as given in the equation. When transition of polarization is different (i.e. from 1 to 0 & 0 to 1) then E_{diss} is summation of the total kink energy which is contributed by the two cells and due to clock energy during switching.

$$E_{diss}\,|_{1\ to\ 0\ \&\ 0\ to\ 1} = \left[\frac{2\gamma_{new}}{E_k}\left(\frac{p_0}{\bar{P}_{old}}\gamma_{old} - \frac{p_n}{\bar{P}_{new}}\gamma_{new}\right) + \frac{E_k\bar{P}_{new}}{2}(p_0 - p_n)\right]$$

In the case of same polarization transition (i.e. from 1 to 1 & 0 to 0), the E_k value will be canceled and only dissipated energy which is caused by clock energy during switching, will be taking part. Therefore, energy is dissipated even if the polarization of a cell does not change to the next cell and this dissipated energy is equal to –

$$E_{diss}\,|_{1\ to\ 1\ \&\ 0\ to\ 0} = \frac{2\gamma_{new}}{E_k}\left(\frac{p_0}{\bar{P}_{old}}\gamma_{old} - \frac{p_n}{\bar{P}_{new}}\gamma_{new}\right)$$

It is noted that all the points of E_{diss} vs $\frac{\gamma_{new}}{E_k}$ curve in Figure 16 is same for 1 to 0 and 0 to 1 transition as well as for 1 to 1 and 0 to 0.

6.1 Kink energy calculation of the designed circuits

Kink energy calculation is done in the output cell considering the radius of effect of the neighboring cells. It is observed that to get low error probability kink energy and power dissipation from the circuit increases. So calculation of kink energy will give some idea about the maximum power dissipation of the designed circuit. So it can be concluded that energy dissipation from the circuit designed in QCA is proportional to the calculation of kink energy and it is obvious that it should be minimum.

Kink energy calculation for the design shown in Fig. 14 is given below where there are three gates connected as a load in the output section. For the calculation of kink energy output section X, W and Z of the designed circuit are taken simultaneously. All output connections along with the polarization is shown in Fig. 17.

Calculation for output x (Output of NAND gate)

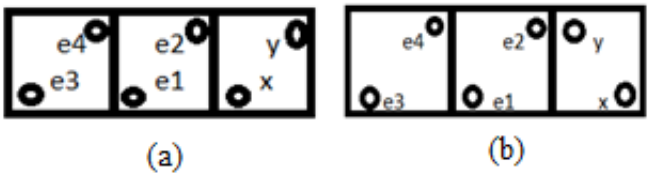


Fig. 17 (a) Tristate buffer (output section polarization +1), (b) Tristate buffer (output section polarization -1)

Table 3 (a) Kink energy calculation for output X

Output X	Polarization taken as +1	kink energies at the positions from x	kink energy calculation (10^{-20} J)	kink energies at the positions from y	kink energy calculation (10^{-20} J)
		U_1	1.152	U_1	0.548
		U_2	1.272	U_2	1.152
		U_3	0.576	U_3	0.379
		U_4	0.810	U_4	0.576
		Total, U_x	3.81	Total, U_y	2.655
		U_{Total_1} = U_x + U_y = 6.4654 x 10^{-20} (J)			
	Polarization	kink energies at the positions from x	kink energy calculation (10^{-20} J)	kink energies at the positions from y	kink energy calculation

					(10^{-20} J)
		U_1	0.8565	U_1	0.6063
		U_2	11.52	U_2	0.8565
		U_3	0.525	U_3	0.3972
		U_4	1.0472	U_4	0.525
		Total, U_x	13.9487	Total, U_y	2.367
		U_{Total_2} = U_x + U_y = 16.3157 x 10^{-20} (J)			
$U = U_{Total\_2} - U_{Total\_1}$ = 9.8503 x 10^{-20} (J)					

Table 3 (b) Kink energy calculations for output W

Output W	Polarization taken as +1	kink energies at the positions from x	kink energy calculation (10^{-20} J)	kink energies at the positions from y	kink energy calculation (10^{-20} J)
		U_1	1.152	U_1	0.548
		U_2	1.272	U_2	1.152
		U_3	0.576	U_3	0.379
		U_4	0.810	U_4	0.576
		Total, U_x	3.81	Total, U_y	2.655
		U_{Total_1} = U_x + U_y = 6.4654 x 10^{-20} (J)			
	Polarization taken as -1	kink energies at the positions from x	kink energy calculation (10^{-20} J)	kink energies at the positions from y	kink energy calculation (10^{-20} J
		U_1	0.8565	U_1	0.6063
		U_2	11.52	U_2	0.8565
		U_3	0.525	U_3	0.3972
		U_4	1.0472	U_4	0.525
		Total, U_x	13.9487	Total, U_y	2.367
		U_{Total_2} = U_x + U_y = 16.3157 x 10^{-20} (J)			
$U = U_{Total\_2} - U_{Total\_1}$ = 9.8503 x 10^{-20} (J)					

Table 3 (c) Kink energy calculation for output Z

Output Z	Polarization taken as +1	kink energies at the positions from x	kink energy calculation (10^{-20} J)	kink energies at the positions from y	kink energy calculation (10^{-20} J
		U_1	1.152	U_1	0.548
		U_2	1.272	U_2	1.152
		U_3	0.576	U_3	0.379
		U_4	0.810	U_4	0.576
		Total, U_x	3.81	Total, U_y	2.655
		U_{Total_1} = U_x + U_y = 6.4654 x 10^{-20} (J)			
	Polarization taken as -1	kink energies at the positions from x	kink energy calculation (10^{-20} J)	kink energies at the positions from y	kink energy calculation (10^{-20} J
		U_1	0.8565	U_1	0.6063
		U_2	11.52	U_2	0.8565
		U_3	0.525	U_3	0.3972
		U_4	1.0472	U_4	0.525
		Total, U_x	13.9487	Total, U_y	2.367
		U_{Total_2} = U_x + U_y = 16.3157 x 10^{-20} (J)			

$$U = U_{Total\_2} - U_{Total\_1} = 9.8503 \times 10^{-20} \text{ (J)}$$

From table 3(a) to 3(c) it is observed that the above calculations of kink energy remain same in each sections of output connected in the designed circuit. So the all the outputs remain in a steady state.

VII. Robust ness of the circuit

Proposed circuit is designed using layered NAND and NOR gates. So it is very important to check the robustness of the circuit. During fabrication several errors may occur like cell misplacement, cell omission or angle displacement from right cell alignment. In this work it is shown that the device cell is misplaced from its original position from both the output of the designed buffer circuit. The reason for taking device cell is that it is placed in a separate layer for the NAND and NOR gate configuration. It is observed that output at X is obtained correctly if its device cell is shifted up to 28nm. Similarly shifting of 17 nm for the Z port device cell is perfect and it measures the correct output. Fig. 18 shows the circuit design where device cells are misplaced from the original design which is shown in Fig. 14. Simulated output is shown in Fig. 19 and it is the same as observed in Fig. 15 which is the simulated output of original circuit as shown in Fig. 14.

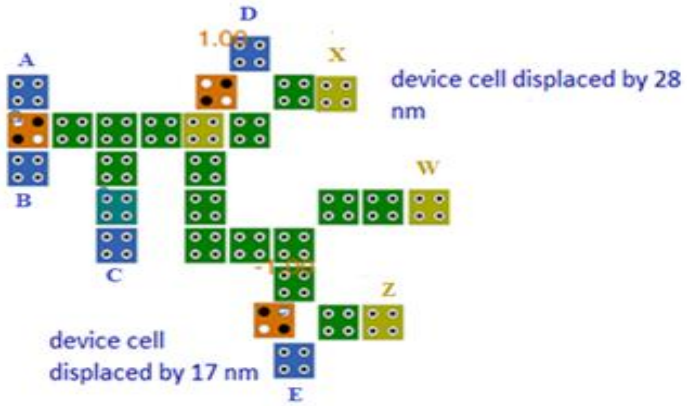


Fig. 18 Tristate buffer with device cell displacement

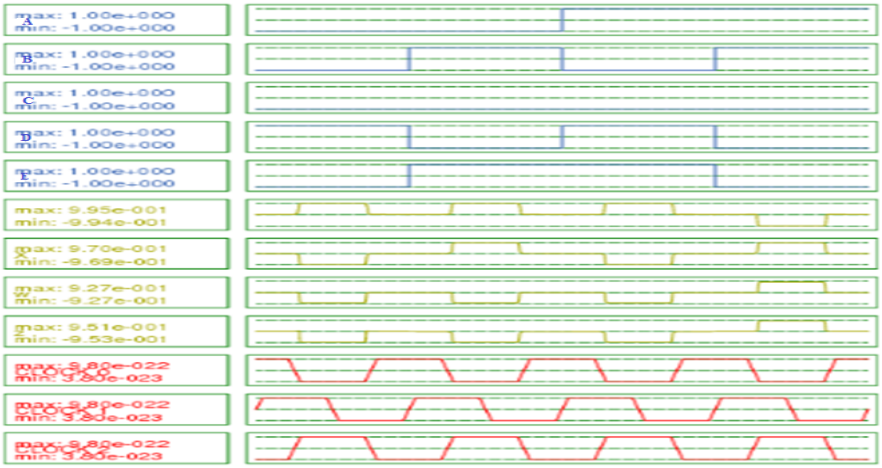


Fig. 19 Simulated output after displacement

VIII. Conclusion

The paper explained the detail design of a Tristate buffer circuit used in digital domain which is a new concept in Quantum Dot Cellular Automata. The design is analyzed with the calculation of energy which shows that output obtained from the various gates attached in the output section of the circuit is a stable one. Detail discussion about the energy dissipation and effect of clock energy on it also discussed in the paper. Energy dissipated from the buffer circuit remains same and it proves the statement that Fan out with three logic gates is possible for the proposed design. Circuit robustness is checked by displacement of device cell from two gates such as NAND and NOR gate attached with it. Output controlled by controlling the input of a Tristate buffer circuit is a new concept in QCA based design. In this paper three outputs are controlled by controlling one cell

in the input section. In future it is aimed to design the buffer circuit in quantum dot cellular automata connected with more logic gates which can be used in different applications in nano lavel.

References

[1]. Craig S Lent, P. Douglas Tougaw, 1997 , A Device Architecture for Computing with Quantum Dots. 84(4).
[2]. Lent C S, Liu M and Lu Y, 2006, *Nanotechnology*. 17: 4240.
[3]. S. Srivastava, S. Sarkar and S. Bhanja, 2009 Power Dissipation Bounds and Models for Quantum-dot Cellular Automata Circuits. *IEEE Transactions on Nanotechnology*. 8(1): 116-127.
[4]. R. Compano, L. Molenkamp, and D.J. Paul 2000.Technology Roadmap for Nanoelectronics. *European Commission IS Programme Future and Emerging Technologies*.
[5]. A.O. Orlov, I. Amlani, G.H. Bernstein, C.S. Lent, and G.L. Snider, 1997, Realization of a Functional Cell for Quantum-Dot Cellular Automata, *Science*, 277:928-930.
[6]. A. Orlov, R. Kummamuru, R. Ramasubramaniam, C. Lent, G. Bernstein, and G. Snider, 2003, Clocked quantum-dot cellular automata shift register, *Surface Science*, 532: 1193–1198.
[7]. R. Kummamuru, A. Orlov, R. Ramasubramaniam, C. Lent, G. Bernstein, and G. Snider, 2003, Operation of a quantum-dot cellular automata (qca) shift register and analysis of errors, *IEEE Transactions on Applied Physics*, 50:1906–1913.
[8]. I. Amlani, A.O. Orlov, G. Toth, C.S. Lent, G.H. Bernstein, and G.L.Snider, 1999, Digital Logic Gate Using Quantum-Dot Cellular Automata, *Science*, 284(5412):289-291.
[9]. M. Lieberman, S. Chellamma, B. Varughese, Y. Wang, C.S. Lent, G.H. Bernstein, G. Snider, and F. Peiris, 2002, Quantum-Dot Cellular Automata at a Molecular Scale, *Annals of the New York Academy of Sciences*, 960: 225-239.
[10]. C.S. Lent, B. Isaksen, and M. Lieberman,2006, Molecular quantum-dot cellular automata, *Journal of American Chemical Society*, 125: 1056-1063.
[11]. W. Hu, K. Sarveswaran, M. Lieberman, and G. H. Bernstein, 2005, High-resolution electron beam lithography and DNA nano-patterning for molecular qca, *IEEE Transactions on Nanotechnology*, 4: 312-316.
[12]. Craig S Lent, P Douglas Tougaw, Wolfgang Porod and Gary H Bernste, 1992, Quantum Transport, Department of Electrical Engineering, University of Notre Dame.
[13]. Tougaw, P. D. & Lent, C. S, 1994, Logical Devices Implemented Using Quantum Cellular Automata. *Journal of Applied Physics*, 75(3): 1818-1825.
[14]. Michael Thaddeus Niemier, B.S, 2004, Department of Computer Science and Engineering, Notre Dame, Indiana.
[15]. P.D. Tougaw and C.S. Lent, 1994, Logical devices implemented using quantum cellular automata, Journal *of Applied Physics*, 75: 1818.
[16]. Hennessy, K. & Lent, C. S, 2001, Clocking of Molecular Quantum-dot Cellular Automata. *Journal of Vacuum Science and Technology B* 19 (5): 1752-1755.
[17]. Amiri, M. A. Mahdavi, M. & Mirzakuchaki, S. 2008, QCA Implementation of a Mux-Based FPGA CLB, *Proceedings of International Conference On Nanoscience and Nanotechnology*, 141-144.
[18]. Vankamamidi, V, Ottavi, M. & Lombardi, F. 2008,. Two-Dimensional Schemes for Clocking/Timing of QCA Circuits. *IEEE Transaction on Computer Aided Design of Integrated Circuits and Systems*, 27(1): 34-44.
[19]. Ratna Chakrabarty et al, 2015, Layered T Full Adder in Quantum-dot Cellular Automata: Paradigm based on Semiconductor Approach, *IEEE Conecct* , 1-6.
[20]. R Farazkish, 2015, A new quantum-dot cellular automata fault-tolerant full-adder: Journal of Computational Electronics, 14(2),506–514
[21]. http://www.qcaddesign.ca
[22]. Saket Srivastava, Sudeep Sarkar and Sanjukta Bhanja, 2006, Power Dissipation Bounds and Models for Quantum-dot Cellular Automata Circuits, *IEEE NANO*.