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Verilog Implementation of 32 Point FFT Using Radix-2 Algorithm on FPGA Technology

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Abstract: *Here the transformation related to the fast Fourier strategy mainly used in the field oriented well effective operations of the strategy elated to the scenario of the design oriented fashion in its implementation related to the well efficient strategy of the processing of the signal in the digital domain plays a crucial role in its analysis point of view in well oriented fashion respectively. It can also be applicable for the processing of the images and there is a crucial in its analysis in terms of the pixel wise process takes place in the system in well effective manner respectively. There is a vast number of the applications oriented strategy takes place in the system in w ell effective manner in the system based implementation followed by the well efficient analysis point of view in well stipulated fashion of the transformation related to the fast Fourier strategy plays a crucial role and some of them includes analysis of the signal, Filtering of the sound and also the compression of the data equations of the partial differential strategy plays a major role and the responsibility in its implementation scenario in a well oriented fashion respectively. There is a huge amount of the efficient analysis of the system related to the strategy of the transformation of the fast Fourier environment plays a crucial role and the responsibility for the effective implementation of the DFT in well respective fashion. Here in the present system oriented strategy DFT implementation takes place in a well explicit manner followed by the well effective analysis of the system where domain related to the time based strategy of the decimation plays a crucial role in its implementation aspect in well effective fashion respectively. Experiments have been conducted on the present method where there is a lot of analysis takes place on the large number of the huge datasets in a well oriented fashion with respect to the different environmental strategy and there is an implementation of the system in a well effective manner in terms of the improvement in the performance followed by the outcome of the entire system in well oriented fashion respectively.*
Keywords: *FFT, DIT, DIF, DFT, Radix-2, 4, 8, VHDL, FPGA.*

I. Introduction

There is a huge proposal takes place in the system in the design oriented strategy in well explicit manner takes place in the system of the design oriented phenomena of the 32 point FFT of the block based on the processing playas crucial role in terms of the analysis in a well effective manner respectively [1][2]. There is an efficient analysis takes place in the system in terms of the focusing of the project based on the aspect of the design based strategy in well effective manner of the kit based on the FPGA plays a crucial role respectively [3].

Block Diagram

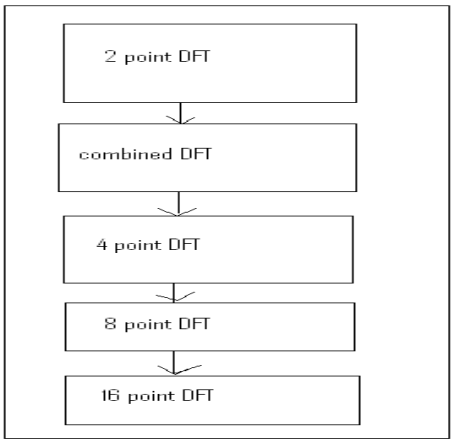


Fig 1: Shows the block diagram of the present method respectively

II. Methodology

In this paper a method is designed with a well effective strategy oriented framework in a well effective manner used for the implementation of the system in terms of the performance based strategy followed by the accurate analysis with respect to the system respectively [4][5]. Here the present designed method is shown in the below figure in the form of the block diagram and explains in the elaborative fashion respectively. Here the present method completely overcomes the drawbacks of the several previous methods in a well efficient manner that is in terms of the performance followed by the accurate analysis respectively [6][7][9]. There is a huge challenge for the present method where it is implemented by the effective analysis and there is an accurate analysis of the system in a well effective manner followed by the performance based evaluation in a well oriented aspect respectively [8]00.

III. Radix-2 Dit Fft Algorithm

The radix-2 algorithms are the simplest FFT algorithms. The decimation-in-time (DIT) radix-2 FFT recursively partitions a DFT into two half-length DFTs [13] of the even-indexed and odd-indexed time samples. The outputs of these shorter FFTs are reused to compute many outputs, thus greatly reducing the total computational cost. The radix-2 decimation-in-time and decimation-in-frequency fast Fourier transforms (FFTs) are the simplest FFT algorithms. Like all FFTs, they gain their speed by reusing the results of smaller, intermediate computations to compute multiple DFT frequency outputs.The radix-2 decimation-in-time algorithm rearranges the discrete Fourier transform (DFT) equation into two parts: a sum over the even-numbered discrete-time indices n=[0,2,4,…,N_2] and a sum over the odd-numbered indices n=[1,3,5,…,N_1] .

$$\begin{aligned} X(k) &= \sum_{n=0}^{N-1} x(n) e^{-\left(i\frac{2\pi nk}{N}\right)} \\ &= \sum_{n=0}^{\frac{N}{2}-1} x(2n) e^{-\left(i\frac{2\pi\times(2n)k}{N}\right)} + \sum_{n=0}^{\frac{N}{2}-1} x(2n+1) e^{-\left(i\frac{2\pi(2n+1)k}{N}\right)} \\ &= \sum_{n=0}^{\frac{N}{2}-1} x(2n) e^{-\left(i\frac{2\pi nk}{\frac{N}{2}}\right)} + e^{-\left(i\frac{2\pi k}{N}\right)} \sum_{n=0}^{\frac{N}{2}-1} x(2n+1) e^{-\left(i\frac{2\pi nk}{\frac{N}{2}}\right)} \\ &= \mathrm{DFT}_{\frac{N}{2}}[[x(0),x(2),\ldots,x(N-2)]] + W_N^k \mathrm{DFT}_{\frac{N}{2}}[[x(1),x(3),\ldots,x(N-1)]] \end{aligned}$$

This is called decimation in time because the time samples are rearranged in alternating groups and a radix-2[5] algorithm because there are two groups. A basic butterfly [13] operation is shown in Figure 2, which requires only N2 twiddle-factor multiplies per stage.

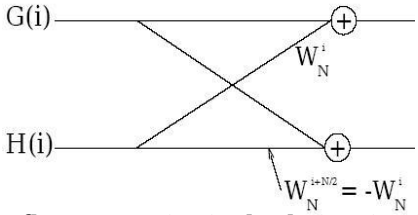


Fig 2: Basic butterfly computation in the decimation-in-time FFT algorithm.

The same radix-2 decimation in time can be applied recursively to the two length N2 DFTs to save computation. When successively applied until the shorter and shorter DFTs reach length-2, the result is the radix-2 DIT FFT algorithm.

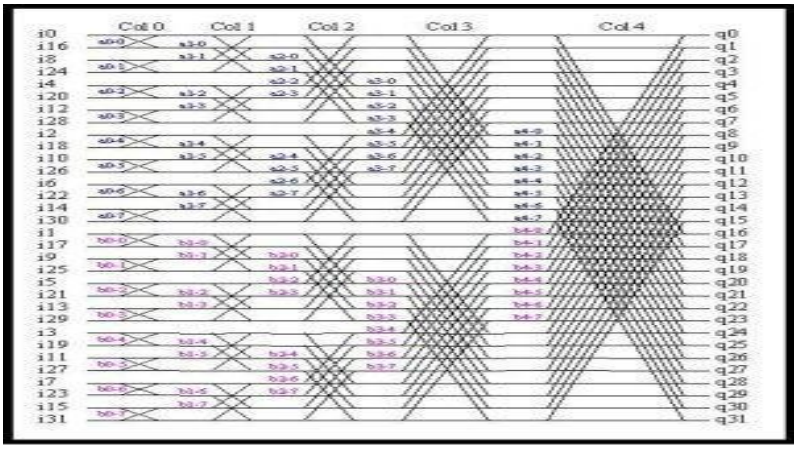


Fig 3: Radix-2 Decimation-in-Time FFT algorithm for a length-32 signal

IV. Software Simulation And Results

A lot of analysis is made in the present method and a huge number of the computations have been applied on the large number of the data sets in a well oriented fashion respectively. A comparative analysis is made between the present method to that of the several previous methods in a well effective fashion and is shown in the below figure in the form of the graphical representation and explains in an elaborative fashion respectively. There is a huge challenge for the present method where it is supposed to overcome the drawbacks of the several previous methods followed by the accurate analysis of the system in a well oriented fashion respectively.

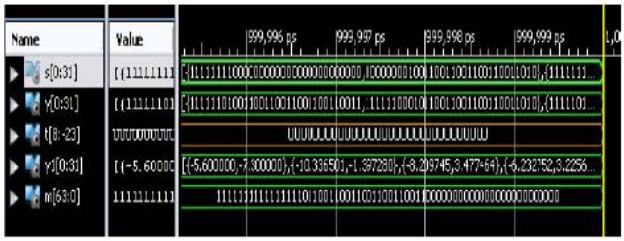
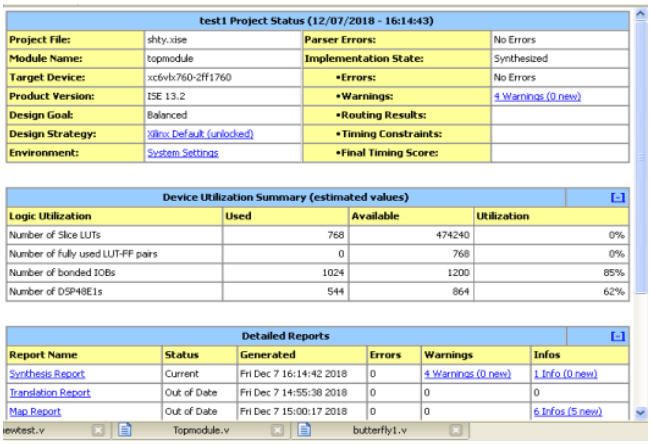


Fig 4: Shows the simulations of the present method respectively

Synthesis Report

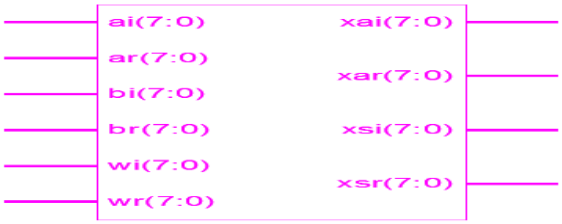


test1 Project Status (12/07/2018 - 16:14:43)			
Project File:	shty.xise	Parser Errors:	No Errors
Module Name:	topmodule	Implementation State:	Synthesized
Target Device:	xc6vlx760-2ff1760	•Errors:	No Errors
Product Version:	ISE 13.2	•Warnings:	4 Warnings (0 new)
Design Goal:	Balanced	•Routing Results:	
Design Strategy:	Xilinx Default (unlocked)	•Timing Constraints:	
Environment:	System Settings	•Final Timing Score:	

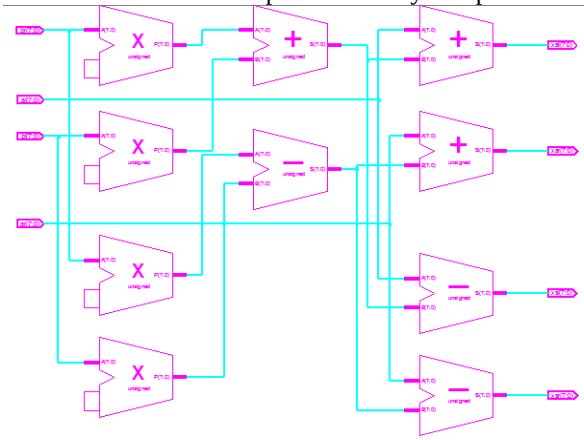
Device Utilization Summary (estimated values)			
Logic Utilization	Used	Available	Utilization
Number of Slice LUTs	768	474240	0%
Number of fully used LUT-FF pairs	0	768	0%
Number of bonded IOBs	1024	1200	85%
Number of DSP48E1s	544	864	62%

Detailed Reports					
Report Name	Status	Generated	Errors	Warnings	Infos
Synthesis Report	Current	Fri Dec 7 16:14:42 2018	0	4 Warnings (0 new)	1 Info (0 new)
Translation Report	Out of Date	Fri Dec 7 14:55:38 2018	0	0	0
Map Report	Out of Date	Fri Dec 7 15:00:17 2018	0	0	6 Infos (5 new)

Block Diagram of 2- point DFT



RTL Schematic of 2-point Butterfly computation



V. Conclusion

In the paper a method is designed with a powerful technique where there is a lot of analysis takes place in the system in which accurate analysis in terms of the improvement in the performance followed by the outcome of the entire system in a well oriented fashion respectively. Here in the present strategy there is a eel effective implementation of the system in which well oriented in terms of the design based specification of the scenario related to the well oriented aspects of the block based FFT in a well efficient manner followed by the implementation of the mechanism of the 32 length of the sigma l in a well effective manner followed by the analysis oriented strategy for the synthesis followed by the simulation in well efficient manner of the design of the XILINX plays a crucial role in its representation respectively. Here the block well oriented with respect to the strategy of the real time logic plays a crucial role in its representative phenomena takes place in the system mainly used for the process of the data in the time based domain of the decimation in well oriented fashion respectively. Here we finally conclude that the present method is effective and efficient in terms of the performance followed by the outcome of the entire system in a well oriented fashion respectively.

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