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Power Line Carrier Communication

Dorathe. V
Department of electronics and communication engineering Jeppiaar engineering college Chennai,Tamil

Abstract: *Communication is the backbone for all modes of development in this modern world. Without communication the whole world is virtually deaf and dumb. In order to minimise the cost spent on additional wires, we are using the same existing power lines as a medium of communication in this project. The data are mixed with radio frequency carrier (40-500 kHz) and then injected into high voltage power line using a suitable Coupling Capacitor.The power line has a rigid, long conductor parallel to the ground that guides the carrier waves to travel along the transmission line. This system which is economic and reliable for inter grid message transfer is mainly used for telecommunication, tele-protection and tele-monitoring between electrical substations through power lines at high voltages such as 110KV, 220KV, 440KV.*

I. INTRODUCTION

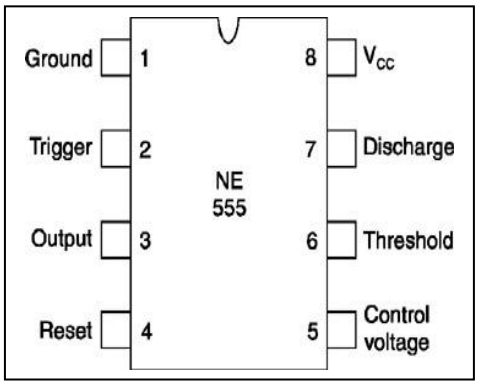
The PLCC has a transmitter block and receiver block. In the transmitter block ,we use audio signal as an input which should be amplified with a pre amplifier before getting modulated. After pre amplification the audio signal is modulated with the carrier signal by FM modulator. Before transmitting the signal, it should be amplified once again using RF amplifier. Now the modulated and amplified signal is given to the transformer in which isolates RF signal with the 230V AC supply. Finally the signal is coupled to the AC line with the help of coupling capacitor, which allows high frequency modulated signal simultaneously providing high impedance to the power frequency (50 Hz). In receiver block the signal is received from the 230V power line through the coupling capacitor. Then the received signal is given to transformer which is used for isolation purpose and then the RF signal is amplified using RF amplifier. The amplified output is given to PLL FM demodulator for the extraction of audio signal from the modulated signal. Then demodulated output is power amplified and is given to the loud speaker.

II. COMPONENTS

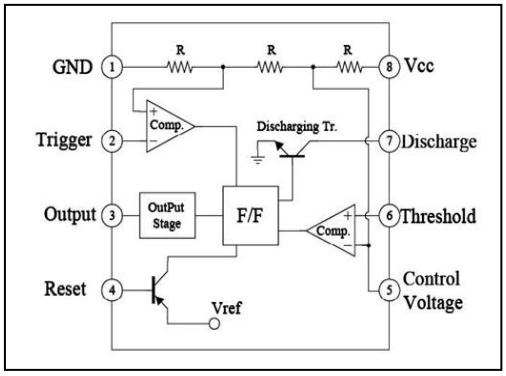
A. I.Ne 555 Timer (Modulator)

The NE555 is a highly stable controller capable of producing accurate timing pulses. It is an 8pin timer IC and has mainly two modes of operation: monostable and astable. With monostable operation, IC 555 is commonly used for generating time delays and pulses.In the time-delay or monostable mode of operation, the timed interval is controlled by a single external resistor and capacitor network. In the astable mode of operation, the frequency and duty cycle can be controlled independently with two external resistors and a single external capacitor.The threshold and trigger levels normally are two-thirds and one-third, respectively, of VCC. This IC consists of 23 transistors, 2 diodes and 16 resistors. The explanation of terminals coming out of the 555 timer IC is as follows. The pin number used in the following discussion refers to the 8-pin DIP and 8-pin metal can packages.The NE555 is characterized for operation from 0°C to 70°C

PIN DIAGRAM OF NE 555



INTERNAL BLOCK DIAGRAM



The block diagram of a **555 timer** is shown in the above. A 555 timer has two comparators, which are basically 2 op-amps, an R-S flip-flop, two transistors and a resistive network.

- Resistive network consists of three equal resistors and acts as a voltage divider.
- Comparator 1 compares threshold voltage with reference voltage 2/3 VCC volts.
- Comparator 2 compares the trigger voltage with a reference voltage + 1/3 VCC volts.

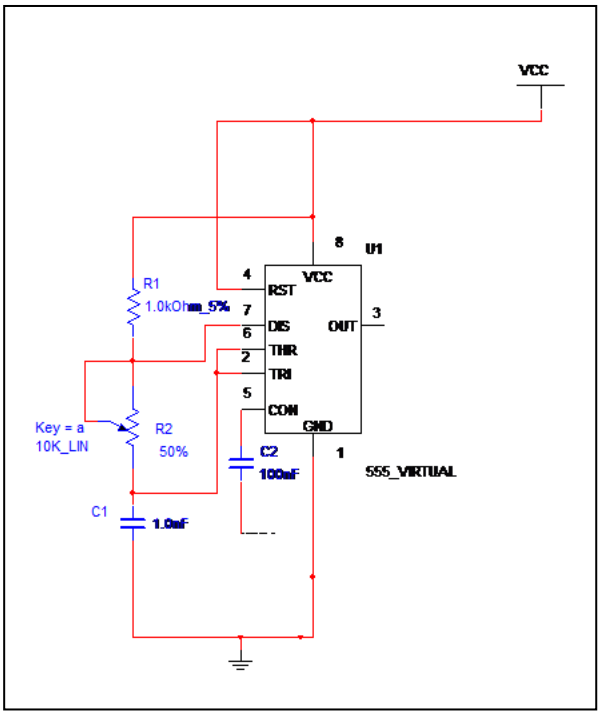
Output of both the comparators is supplied to the flip-flop. Flip-flop assumes its state according to the output of the two comparators. One of the two transistors is a discharge transistor of which collector is connected to pin 7. This transistor saturates or cuts-off according to the output state of the flip-flop. The saturated transistor provides a discharge path to a capacitor connected externally. Base of another transistor is connected to a reset terminal. A pulse applied to this terminal resets the whole timer irrespective of any input.

A. ii. FM MODULATION

Here we are using IC 555 in astable mode to make it function as an FM Modulator.

An Astable Multivibrator, often called a free-running multivibrator, is a rectangular-wave generating circuit. Unlike the monostable multivibrator, this circuit does not require any external trigger to change the state of the output, hence the name free-running.An astable multivibrator can be produced by adding resistors and a capacitor to the basic timer IC, as illustrated in figure. The timing during which the output is either high or low is determined by the externally connected two resistors and a capacitor.

FM MODULATION CIRCUIT



Pin 1 is grounded; pins 4 and 8 are shorted and then tied to supply +Vcc, output (V_{OUT}) is taken form pin 3; pin 2 and 6 are shorted and the connected to ground through capacitor C_1, pin 7 is connected to supply + V_{CC} through a resistor R_1; and between pin 6 and 7 a resistor R_2 is connected. At pin 5 a bypass capacitor of 100 nF is connected.

A.iii.DESIGN

For astable oscillator

$T_1 = 0.693(R_1+R_2)C_1$ and

$T_2 = 0.693*R_2*C_1$

Frequency $f = 1/T = 1.44/((R_1+2R_2)C_1)$

Assume $R_1 = 1\ k\Omega$, $R_2 = 10\ k\Omega$ and $C_1 = 1nF$

Substitute the values in the above formula

Frequency $(f) = 1.44/((20\ k\Omega+1\ k\Omega)*1\ nF)$

Therefore Frequency $(f) = 68.5\ kHz$

In order to achieve FM modulation we need to apply our actual message input (audio signal) is applied to control pin (pin 5) of the 555 timer through 100 nF. By varying the massage signal frequency respectively the output pulse width also varied. Hence FM modulation is achieved. The typical FM modulation circuit diagram is given above.

B.i. PHASE LOCKED LOOP (LM 565)

In an FM signal, the instantaneous frequency varies in accordance with the modulating signal. For a sinusoidal modulating signal, the frequency deviation in an FM signal is sinusoidal, and it is proportional to the modulating, amplitude. The changes in the instantaneous frequency of the carrier signal occur with respect to the previously attained value of the carrier frequency. This clearly suggests that a PLL can be used to demodulate an FM signal.

Suppose the centre frequency of the FM signal is f_0, and it lies within the hold-in range of PLL the VCO is locked to f_0, by applying a demodulated carrier at the input of the phase detector. When VCO is locked to f_0, the error signal is zero, and therefore, the control signal that changes the VCO frequency is also equal to zero. If an FM signal is applied to the phase detector, there will be a difference in the phases of the VCO output and the input FM signal. The control signal is produced in proportion to the phase difference at an instance of time. This control voltage will modify the VCO frequency, which is again compared with the incoming frequency. In this way, the current incoming frequency is compared with the previously attained value of the VCO frequency, which is previously attained frequency of the FM Signal.

The VCO tries to track the instantaneous frequency of the applied FM signal. The control signal is produced in proportion to the difference between the VCO frequency and the instantaneous frequency of FM signal. In other words, the control signal so produced is proportional to the frequency deviation in the FM signal. Since the frequency deviation is proportional to the modulating signal, the control signal appearing at the output of LPF is the modulating signal. Therefore, the FM signal is demodulated by PLL.

B.ii. INTERNAL BLOCK DIAGRAM OF IC 565

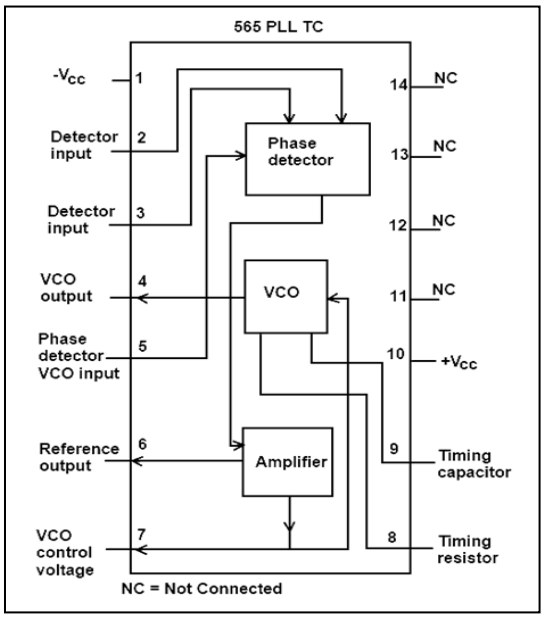
The internal block diagram shows that IC 565 PLL consists of phase detector, VCO, and amplifier. The amplifier also functions as the low pass filter. This is a 14 pin dual in line package.

In figure1.6,the PLL IC consists of two power supply pins marked ±Vcc. The positive terminal of the Vcc is connected to pin number 10, and the negative (ground) terminal of Vcc is connected to pin number 1. The output signal to the phase detector is applied to pin numbers 2 and 3. The VCO output is applied to the phase detector through pin number 5. The output of the phase detector is internally connected to the amplifier (low-pass filter).

The output or the phase detector is low-pass filtered and amplified by the amplifier stage. The Output or the amplifier is the control voltage that is applied to VCO to force it to track the incoming frequency. The control voltage is also available at pin number 7. This is the output signal. In the ease of FM demodulator, the signal at pin number 7 is the modulating signal. The amplifier also generates an output at pin number 6 for reference purposes.

The VCO gets its control voltage internally from the amplifier and its output at pin number 4. The VCO output should be given to the phase detector through pin number 5. It is customary to short pin numbers 4 and 5 so that the VCO output is applied directly to the phase detector. The external resistor and capacitor can set the free-running frequency of the VCO. The resistor and capacitor are called the timing resistor and the timing capacitor. The timing resistor is connected at pin number 8, and the timing capacitor is connected at pin number 9. Pin numbers 11, 12, 13, and 14 are not connected because they do not have any internal circuitry with them.

INTERNAL BLOCK DIAGRAM OF PLL 565

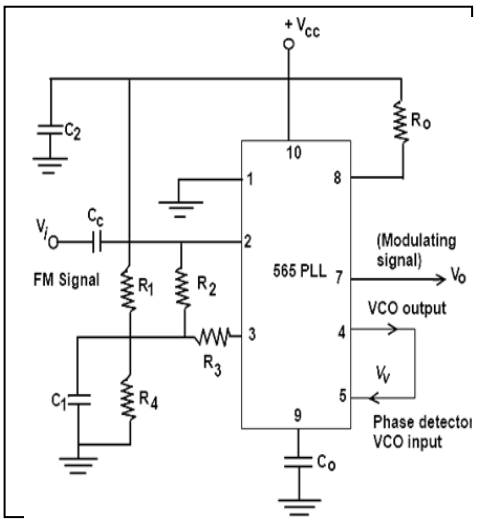


B.iii .CIRCUIT DESCRIPTION

Figure1.7 shows the circuit external to the IC 565 PLL for FM detection. The circuit shown in this figure is a general circuit. The choice of the timing components, resistor R_0 and capacitor C_0 decides the various parameters and the free-running frequency of PLL. Accordingly, the values of other components are also chosen.

The power supply V_{cc} is connected between pin numbers 10 and 1, with $+V_{cc}$ and - V_{cc} applied at pin number 10 and 1 respectively. The timing resistor R_0 is connected to pin number 8, and the timing capacitor, C_0 is connected to pin number 9. The VCO output, which is available at pin number 4 is applied to phase-detector input at pin number 5. Pin number 4 is shorted with pin number 5 as no external component is required in this case.

DEMODULATION CIRCUIT



The input FM signal, V_i, is applied to pin number 2 through the coupling capacitor C_c. A part of this signal is also applied to pin number 3 through the potential divider network, consisting of R_2, R_3, and R_4. The dc power supply is also provided to the input pins 2 and 3 through R_1 from $+V_{cc}$ supply. The capacitor C_2 is used to filter out an AC ripple, if present in the DC supply.

The demodulated FM signal is nothing but the control signal, which is available at pin number 7. Therefore, the signal available at pin number 7 is the required modulating signal.

B.iv. DESIGN

Some typical design equations for various parameters related to PLL operation are:

- The free-running frequency of VCO (f_0) can be calculated as:

$$f_0 = 0.3/R_0C_0$$

For $R_0 = 10$ KΩ, Free-running frequency (f_0) = 68.5 KHz, C_0 is calculated as:

$$C_0 = 0.3/(10 \text{ X } 10^3 * 68.5\ 10^3)$$

$$C_0 = 470 \text{ pF}$$

Thus, for the central frequency of an FM signal to be 68.5 kHz, a resistor 10 KΩ and a capacitor of 470 pF can be used as timing components.

- Hold-in range

The hold-in range may be calculated as:

$$f_h = \pm 8 f_0/V_{cc}$$

Where

f_0 = free running of VCO

V_{cc} = supply voltage

for f0 = 68.5 KHz and V_{cc} = 12 V, the hold-in range is calculated from above Equation as:

$$f_h = \pm 8 \text{ X } 68.5 \text{ X } 10^3/12$$

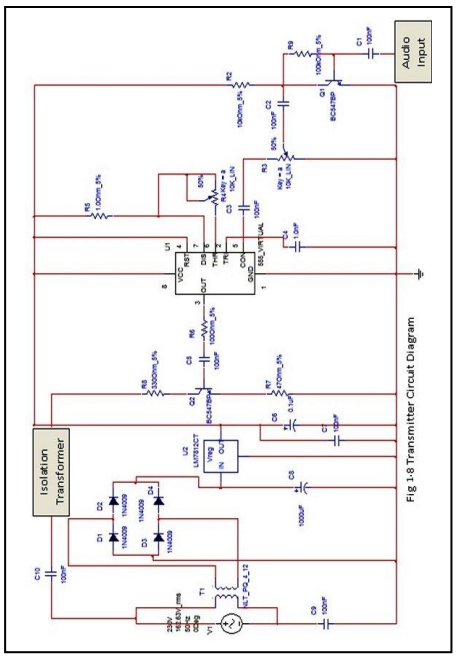
$$f_h = \pm 45.66 \text{ KHz}$$

Therefore, for the given values, the loop will remain locked over a frequency range of ±45.66 KHz after it is locked initially.

C. CIRCUIT DIAGRAM

C.i. TRANSMITTER

Transmitter circuit diagram of PLCC is shown below. Basically we need to amplify the signal before modulation process. We know that transistor amplifies the amplitude of the signal. So we use BC 5473 transistor for pre-amplification process. Here the audio signal is applied to the base of the BC 5473 transistor which amplifies the signal before modulation, called pre-amplification process. The pre amplified signal is then applied to the pin 5 of NE 555 timer through a capacitor. In 555 timerIC, as frequency of message signal varies, the output pulse width also varies. Hence FM modulation occurs. Then the output of 555 is taken from pin 3 and is given to the base of BC 5473 transistor through a coupling capacitor and a resistor for RF amplification. Then the amplified signal is given to the polyester capacitors of 1 nF rated 630 V through a step down transformer. Finally the capacitors are connected to the 230 V (50Hz) AC line. A Bridge rectifier is connected between transformer and voltage regulator (7812), for the rectification of AC signal from the transformer providing constant 12 V power supply to all the transistors and 555 timer respectively



C.ii. RECEIVER

The Receiver part is similar to transmitter part but reverse in operation. A bridge rectifier and a voltage regulator is used for constant supply from the transformer. The modulated signal is taken from the 230 V (50Hz) AC line and is given to the base of BC 5473 transistor. RF amplification is held at this point before the demodulation process. Then the amplified signal is applied to pin 2 of PLL 565, from where the required message signal is demodulated. Detected output is obtained from pin 7 of PLL 565. Now the demodulated signal is again amplified using Power amplifier which is as called Power amplification process. Now thepower amplified signal is fed to the Loud Speaker and the audio signal is received.

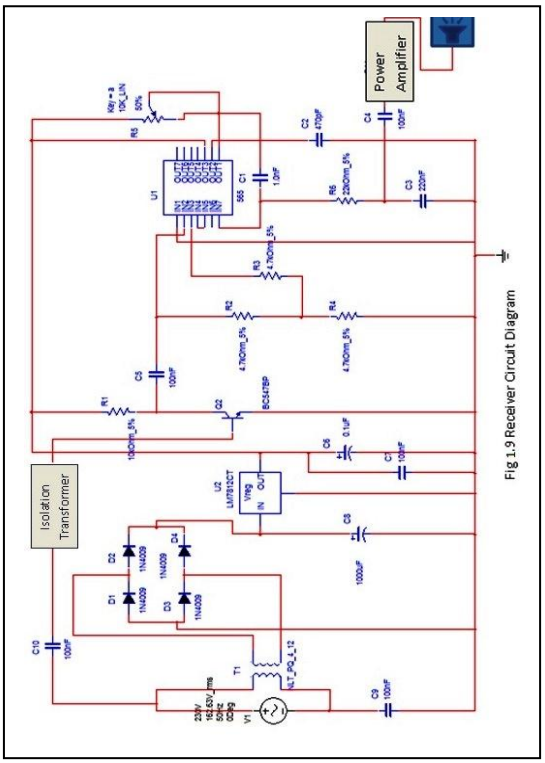


Fig 1.9 Receiver Circuit Diagram

III. ADVANTAGES AND DISADVANTAGES

i. ADVANTAGES

- No separated wires are needed for communication purposes, as the power lines on their own carry power as well as communication signal. Hence the cost of constructing separate telephone lines is saved.
- When compared with ordinary lines the power lines have appreciably higher mechanical strength. They would normally remain unaffected under the condition which might seriously damage telephone lines.

II. DISADVANTAGES

- Proper care has to be taken to guard carrier equipment and persons using them against ac voltages and currents on the lines.

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