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An Efficient Low Power Ripple Carry Adder for Ultra Applications

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Abstract: *The main goal of this paper is to provide new low power solutions for very large scale integration. Designers especially focus on the reduction of the power dissipation which shows increasing growth with the scaling down of the technologies. In this paper various technologies at the different levels of the design process have been implemented to reduce the power dissipation at the circuit, architecture and system levels. Previous technologies are summarized and compared with our new approach is presented in this paper.*

: The main objective of this project is the reduction of power dissipation by eliminating the PMOS tree and also by utilizing energy stored at the output can be retrieved by the reversing the current source direction discharging process instead of dissipation in NMOS network with DOMINO LOGIC, PASS TRANSISTOR LOGIC. It also increases the performance of circuits.

Here for this project, I am using MICROWIND TOOL. By using this tool we can develop schematic for all above techniques and also find out the power dissipation.

Key words*: Low power, CMOS,DUAL RAIL DOMINO LOGIC, PASS TRANSISTOR.*

I. Introduction:

Much of the research efforts of the past years in the area of digital electronics has been directed towards increasing the speed of digital systems. Recently, the requirement of portability and the moderate improvement in battery performance indicate that the power dissipation is one of the most critical design parameters .

The three most widely accepted metrics to measure the quality of a circuit or to compare various circuit styles are area, delay and power dissipation. Portability imposes a strict limitation on power dissipation while still demands high computational speeds. Hence, in recent VLSI systems the power-delay product becomes the most essential metric of performance. The reduction of the power dissipation and the improvement of the speed require optimizations at all levels of the design procedure. In this chapter, the proper circuit style and methodology is considered. Since, most digital
Circuitry is composed of simple and/or complex gates, we study the best way to implement adders in order to achieve low power dissipation and high speed.

Several circuit design techniques are compared in order to find their efficiency in terms of speed and power dissipation. A review of the existing CMOS circuit design styles is given, describing their advantages and their limitations. Furthermore, a four-bit ripple carry adder for use as a benchmark circuit was designed in a full-custom manner by using the different design styles, and detailed transistor-level simulations using HSPICE [2] were performed. Also, various designs and implementations of four multipliers are analysed in the terms of delay and power consumption. Two ways of power measurements are used.

In this chapter we study two different CMOS logic styles, they are

i.DUAL RAIL DOMINO LOGIC

ii. COMPLEMENTORY PASS TRANSISTOR LOGIC (CPL)

Here we are comparing the parameters like power, delay and area of the above mentioned techniques with the CONVENTIONAL CMOS technique.

II. Power And Delay In Conventional

CMOS Circuits:

Since the objective is to investigate the tradeoffs that are possible at the circuit level in order to reduce power dissipation while maintaining the overall system throughput, we must first study the parameters that affect the power dissipation and the speed of a circuit. It is well known that one of the major advantage of CMOS circuits over single polarity MOS circuits, is that the static power dissipation is very small and limited to leakage. However, in some cases such as bias circuitry and pseudo-nMOS logic, static power is dissipated.

Considering that in CMOS circuits the leakage current between the diffusion regions and the substrate is negligible, the two major sources of power dissipation are the switching and the short-circuit power dissipation

$$P = p_f \, C_L \, V_{dd}^2 \, f \quad + \quad I_{sc} \, V_{dd},$$

Where p_f f is the node transition activity factor, C_L is the load capacitance, V_{dd} is the supply voltage, f f is the switching frequency, I_{sc} is the current which arises when a direct path from power supply to ground is caused, for a short period of time during low to high or high to low node transitions . The switching component of power arises when energy is drawn from the power supply to charge parasitic capacitors. It is the dominant power component in a well designed circuit and it can be lowered by reducing one or more of pf , CL, Vdd and f, while retaining the required speed and functionality.

Even though the exact analysis of circuit delay is quite complex, a simple first-order derivation can be used in order to show its dependency of the circuit parameters

$$T_d \;\propto\; \frac{C_L \, V_{dd}}{K \; (V_{dd} - V_{th})^{\alpha}},$$

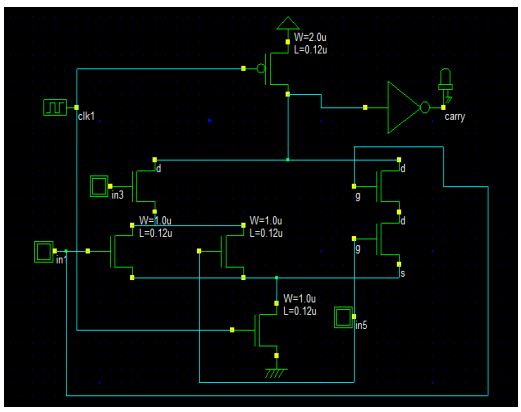
where K depends on the transistors aspect ratio (W/L) and other device parameters, V_{TH} is the transistor threshold voltage, and α is the velocity saturation index which varies between 1 and 2 (α is equal to 1.4 for the 1.5μm process

III. Dual Rail Domino Logic:

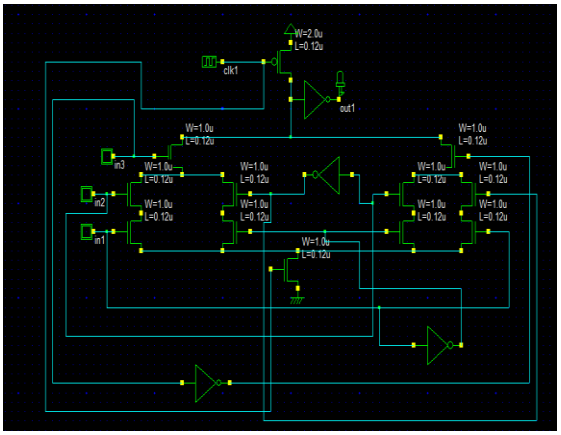
Dual-Rail Domino Logic [10,11] is a precharged circuit technique which is used to improve the speed of CMOS circuits. Figure 5.6 shows a Dual-Rail Domino full adder cell. A domino gate consists of a dynamic CMOS circuit followed by a static CMOS buffer.

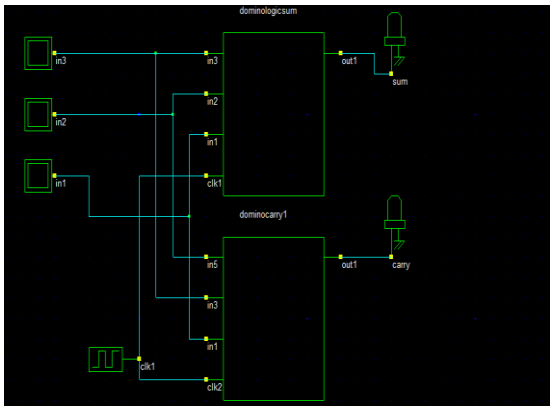
The dynamic circuit consists of a pMOSFET precharge transistor and an nMOSFET evaluation transistor with the clock signal (CLK) applied to their gate nodes, and an nMOSFET logic block which implements the required logic function. During the precharge phase (CLK = 0) the output node of the dynamic circuit is charged through
the precharged pMOSFET transistor to the supply voltage level. The output of
the static buffer is discharged to ground. During the evaluation phase (CLK= 1) the evaluation nMOSFET transistor is *ON*, and depending on the logic performed by the nMOSFET logic block, the output of the dynamic circuit is either discharged or it will stay precharged. Since in dynamic logic every
output node must be precharged every clock cycle, some nodes are precharged only to be immediately discharged again as the node is evaluated, leading to higher switching power dissipation .One major advantage of the dynamic, precharged design styles over the static styles is that they eliminate the spurious
transitions and the corresponding power dissipation. Also, dynamic logic does not suffers from short-circuit currents which flow in static circuits when a direct

DUAL RAIL DOMINO LOGIC CARRY

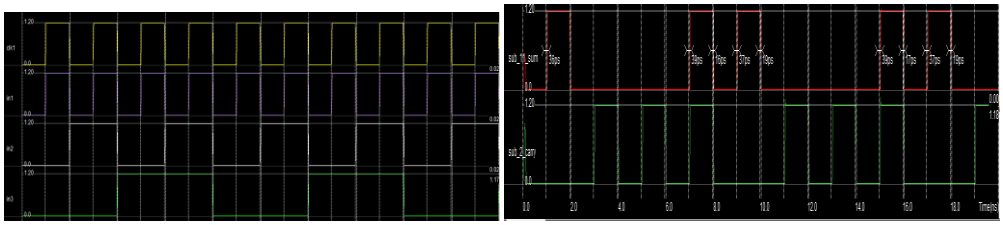


DUAL RAIL DOMINO LOGIC SUM





DUAL RAIL DOMINO LOGIC FULL ADDER

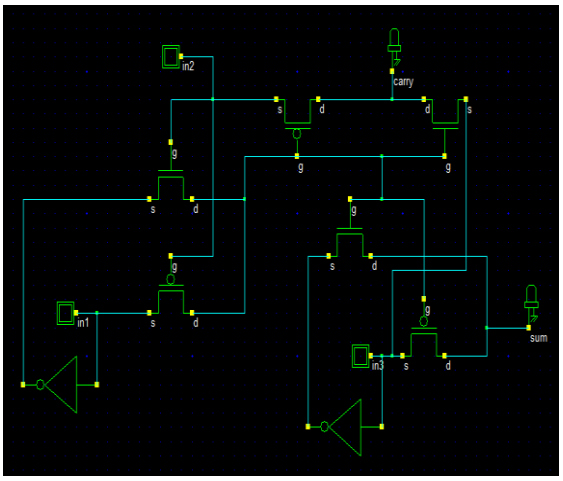


IV. Complementary Pass-Transistor Logic – CPL

The main concept behind CPL [5] is the use of only an NMOSFET network for the implementation of logic functions. This results in low input capacitance and high speed operation. Because the high voltage level of the pass-transistor outputs is lower than the supply voltage level by the threshold voltage of the pass transistors, the signals have to be amplified by using CMOS inverters at the outputs. CPL circuits consume less power than conventional static circuits because the logic swing of the pass transistor outputs is smaller than the supply voltage level. The switching power dissipated from charging or discharging the pass transistor outputs.

In the case of conventional static CMOS circuits the voltage swing at the output nodes is equal to the supply voltage, resulting in higher power dissipation. To minimize the static current due to the incomplete turn-off of the PMOSFET in the output inverters, a weak PMOSFET feedback device can also be added in the CPL circuits.

In order to pull the pass-transistor outputs to full supply voltage level. However, this will increase the output node capacitance, leading to higher switching power dissipation and higher propagation delay.



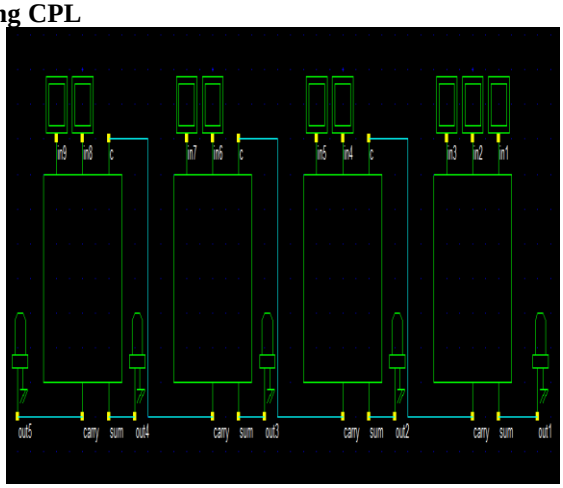
FULLADDER BY COMPLEMENTORY PASS TRANSISTOR

Comparison of technologies:

Technique	power	Area	Delay
CMOS	16.969uw	62*12um	18ps
Domino	9.02uw	34*14um	19ps
CPL	2.17uw	17*12um	16ps

From the above analysis, we came to know that CPL is the best technique. So we design ripple carry adder using the CPL technique because it consumes less power.

Ripple carry adder by using CPL



Above ripple carry adder is designed by using CPL full adder. It consists of four full adders. This ripple carry adder consumes less power as adiabatic logic technique is the efficient in consuming less power and reducing power dissipation.

V. Conclusion:

In this chapter, the most common kinds of adders have been characterized in terms of power, using either a traditional low-level design flow paradigm, which is rather tedious and incompatible with modern design flows, but provides the most accurate results, or a high-level design flow paradigm,
which is commonly used.

In this paper we compared the performance of DUAL RAIL DOMINO LOGIC and CPL adder circuits with traditional CMOS adder circuits. The analysis shows that designs based on adiabatic principle gives superior performance when compared to traditional approaches in terms of power even though their transistor count is high in some circuits so for low power and ultra low power requirements adiabatic logic is an effective alternative for traditional CMOS logic circuit design.

A four-bit ripple carry adder was designed using adiabatic logic here is used as the benchmark circuit. All the circuits have been designed in a full-custom manner.

References:

[1] A. Chandrakasan, R. Brodersen, Low Power Digital Design, Kluwer Academic Publishers, 1995.
[2] Meta-Software, HSPICE User's Manual - Version 96.1,1996.
[3] K. Yano, Y. Sasaki, K. Rikino, K. Seki, "Top-Down Pass-Transistor Logic Design". IEEE Journal of Solid-State Circuits, vol.31, pp. 792-803. 1996
[4] MIPS Technologies, "R4200 Microprocessor Product Information", MIPS Technologies Inc., 1994
[5] R K. Navi, Md.Reza Saatchi and O.Daei,(2009) "A High-Speed Hybrid Full Adder," European Journal of Scientific Research,Vol 26 No.1,pp 29-33.
[6] D. Sourdis, C. Piguet and C. Goutis,(2002) " Designing CMOS Circuits for Low Power, European Low-Power Initiative for Electronic System Design", Reading pp 71-96, Kluwer Academic Publishers.