Minimization Of Total Harmonic Distortion Using Pulse Width Modulation Technique

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Abstract: *Multilevel inversion is a power conversion strategy used to synthesize a desired AC voltage from several levels of DC voltages with reduced total harmonic distortion. These multilevel inverters are used to increase inverter operating voltage, to minimize total harmonic distortion and to reduce electromagnetic induction due to lower voltage steps. The advantages of this multilevel approach include good power quality, good electromagnetic compatibility and low switching losses. This project proposes to study various multilevel inverter topologies like diode clamped inverter, capacitor clamped inverter and cascaded multi-cell inverter operating on several modulation techniques such as single pulse width modulation, sinusoidal pulse width modulation and delta modulation. The main objective of the study is to reduce total harmonic distortion, comparison of total harmonic distortion and fundamental component for different modulation technique. The induction motor is connected as load to observe the stator current harmonics and speed-torque characteristics.*
Keywords: *CMIT, Delta Modulation, DCMIT, FCMIT, SPWM, THD*

I.   Introduction

Inversion is the process of conversion of dc power to ac power at a required output voltage, current and frequency. A static semiconductor inverter performs this electrical energy inverting transformation process. The output connection of an inverter is of two types. A voltage source inverter (VSI) is the one in which the DC input voltage remains constant and is independent of the current drawn by the load. The load voltage is specified by inverter while the drawn current shape is determined by the load. The DC power input to the inverter can be supplied by a power supply network or from a rotating alternator through a rectifier or a battery, fuel cell, PV array or by a magneto hydro generator. In recent years, industries works on mega power level. Today, it is not easy to connect a single power semiconductor switch directly to medium voltage or high voltage grids (2.3, 3.3, 4.16, or 6.9 kV). For these reasons, a new family of multilevel inverters has introduced as the solution for the problem in working with higher voltage levels. Multilevel inversion is a power conversion technique in which the output voltage of is obtained in steps. Hence the output voltage wave form becomes much closer to a sine wave and reduces the total harmonic distortion (THD).Multilevel inverters can be applied to higher power medium voltage control system. Multilevel inverters include an array of power semiconductors switches, capacitor voltage sources and dc voltage sources the output of which generate stepped output voltage waveforms. The power semiconductor switches must withstand some desired voltage level.

II.   Pulse Width Modulation Techniques

2.1: Single Pulse-Width Modulation

The primary aim of any modulation technique is to generate gating signals. In this technique it is done by comparing a rectangular reference signal of amplitude A_r with a triangular carrier wave of amplitude A_c. The frequency of reference signal determines the frequency of the output waveform. The ratio of A_r and A_c is the control variable and termed as the amplitude of modulation index (M).By varying A_r from 0 to A_c, the pulse width can be modified and the rms output voltage varies accordingly.
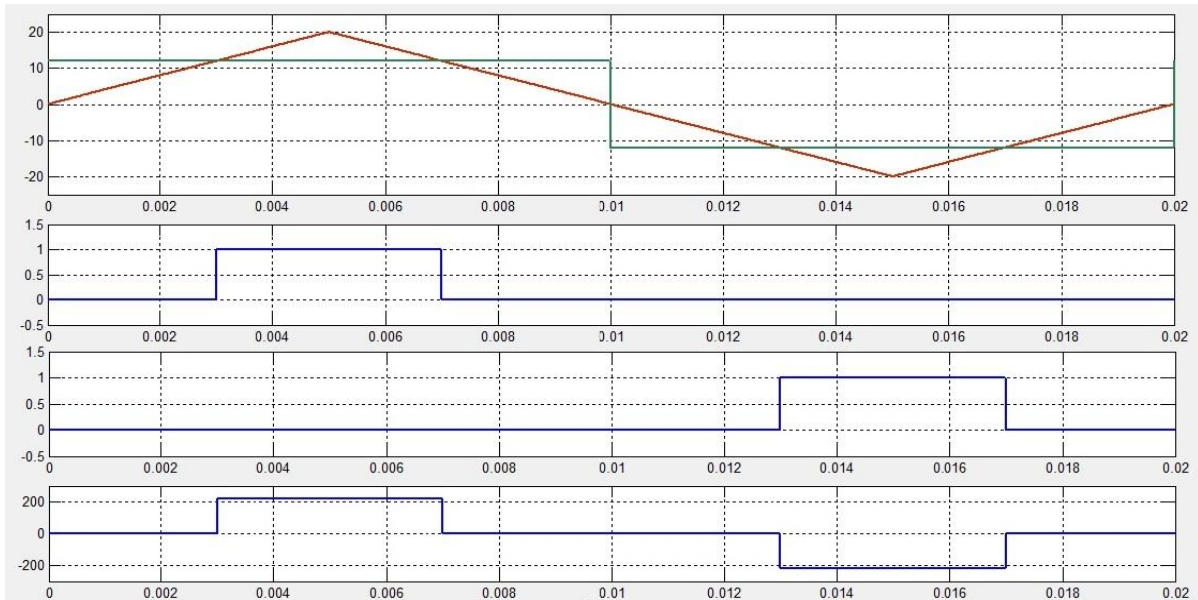
Fig. 1.1: Single pulse width modulation

2.2: Sinusoidal Pulse Width Modulation (SPWM)

Sinusoidal pulse width modulation technique is a very simple technique used for harmonic reduction. The sinusoidal pulse width modulation (SPWM) technique uses sinusoidal reference wave and triangular carrier wave to generate the gate pulses for the inverter. The operating principle of the SPWM technique for a single phase inverter can be explained with the help of figure 1.2. Sinusoidal reference wave (A_r), reference wave with 180° phase difference i.e. (-A_r) and triangular carrier wave (A_c) of higher frequency are shown in the first subplot. When the reference wave is greater than the triangular wave the gate signal is at on state otherwise it is at 0 volt. When the reference wave A_r is greater than A_c gate 1 is triggered. Similarly when -A_r is greater than A_c gate 2 is triggered.
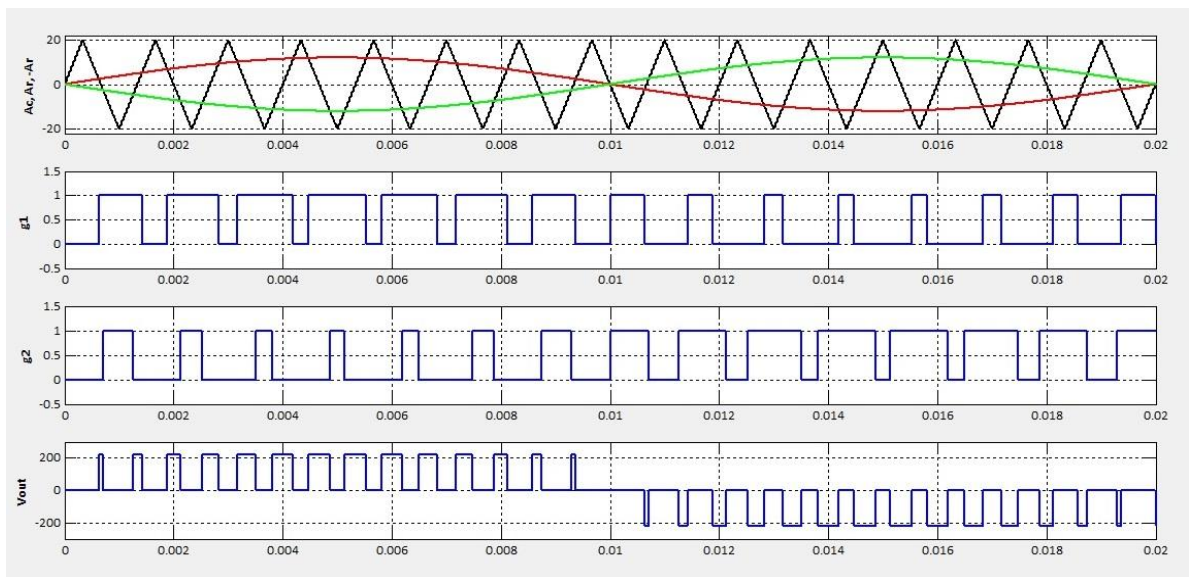

Fig.1.2: Operating principle of SPWM

The output voltage of the three phase SPWM technique is shown in figure 1.3. The carrier signal and three reference signals is shown in 1st subplot. The output voltage of the three phases is shown in 2nd, 3rd and 4th subplot.
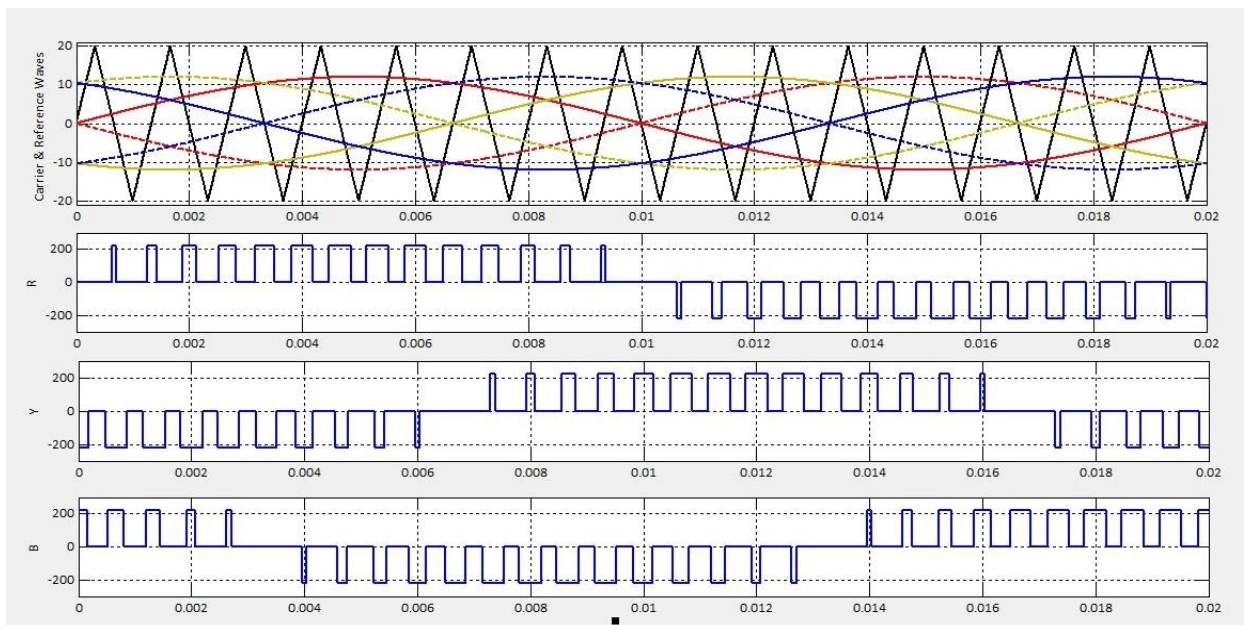
Fig.1.3: SPWM three phase output .

Sinusoidal pulse width modulation technique for multilevel inverter is based on classical two level multilevel inverter technique. In this type of modulation technique, the pulse magnitude is taken to be constant and only pulse width is changed. There are two important defined parameters:

i.   Frequency Ratio $P = \omega_c/\omega_m$
ii.   Modulation Index $M = A_c/A_r$

Here, ω_c is the reference frequency, ω_m is the carrier frequency, A_r is reference signal amplitude and A_c is carrier signal amplitude.

2.3: The Delta Modulation Technique

In this technique, a sinusoidal signal is used as reference. A band is defined along the curvature of the sinusoidal signal with a suitable upper and lower limit. The band is called 'window'. A triangular like carrier signal oscillates within the window. The two switching states of the generated gate signal is defined by the rise and fall of the carrier wave. This technique is also called hysteresis modulation. The output voltage can be changed by changing the frequency of the reference sinusoidal signal.
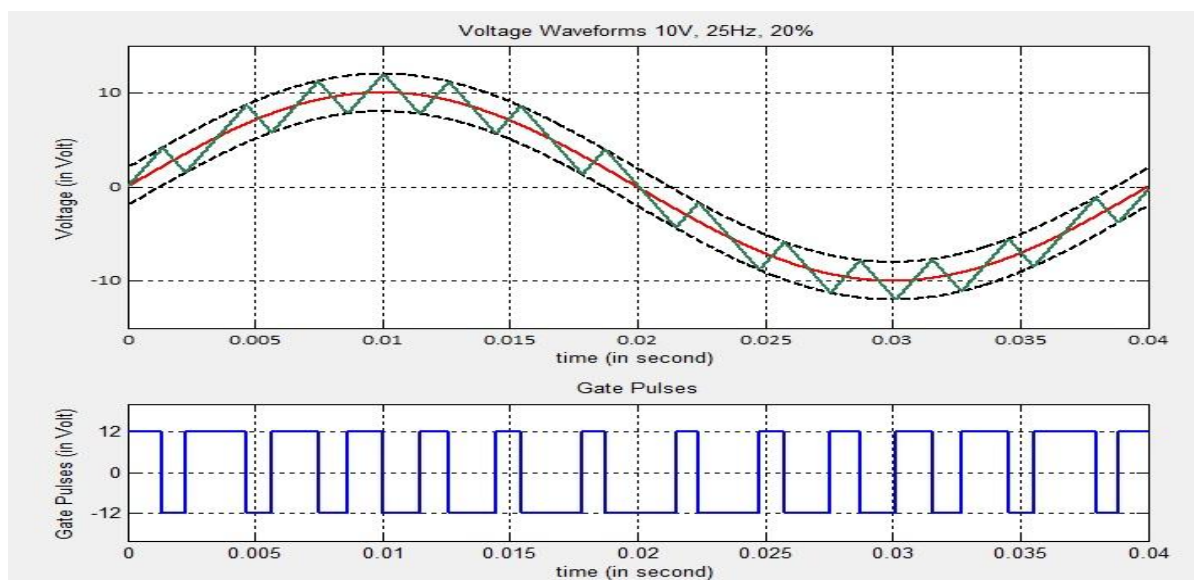

Fig.1.4: Delta modulation waveforms.

A triangular signal performs forced oscillation in a definite window. Comparators are required to compare the reference and carrier waves. A circuit provided in figure 1.4 can generate the delta modulated gate signal.

III.   Multilevel Inversion Techniques

3.1: Diode Clamped Multilevel Inversion Technique (DCMIT):

As the name suggests itself each diode connected across the input dc source is clamped to certain voltage level in order to get desired output voltage in steps. Capacitors are used in parallel with the dc voltage source to divide the potential and the capacitor terminals are used to produce desired voltage level at the output. In an 'm' level diode clamped inverter number of devices required are given by,

- Number of capacitors = m-1
- Number of switching devices = 2*(m-1)
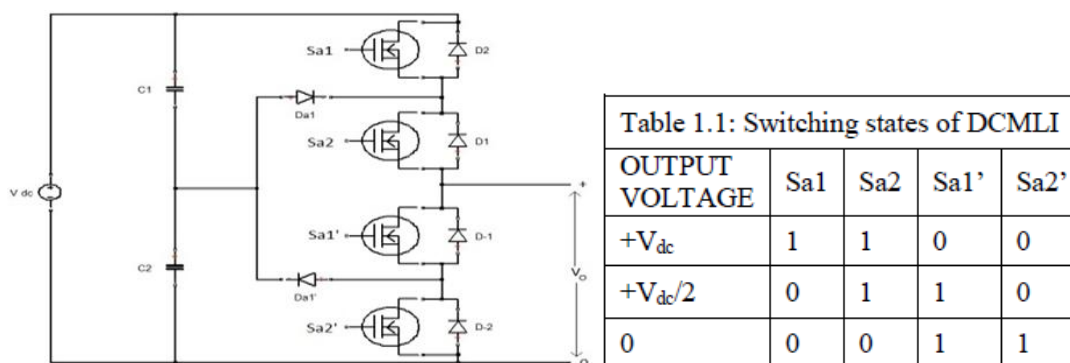- Number of clamping diodes = (m-1)*(m-2)

Table 1.1: Switching states of DCMLI				
OUTPUT VOLTAGE	Sa1	Sa2	Sa1'	Sa2'
$+V_{dc}$	1	1	0	0
$+V_{dc}/2$	0	1	1	0
0	0	0	1	1

Fig.1.5: One leg of diode clamped inverter circuit.

3.2: Flying Capacitor Multilevel Inversion Technique (FCMIT):

Figure 1.6 shows single phase 3 level flying capacitor inverter configuration. A 3 level inverter will require one clamping capacitors per phase leg in addition to two main dc bus capacitors. The voltage levels and the arrangements of the flying capacitors in the FCMLI structure assures that the voltage stress across each main device is same and is equal to $V_{dc}/(m-1)$, for an m-level inverter.
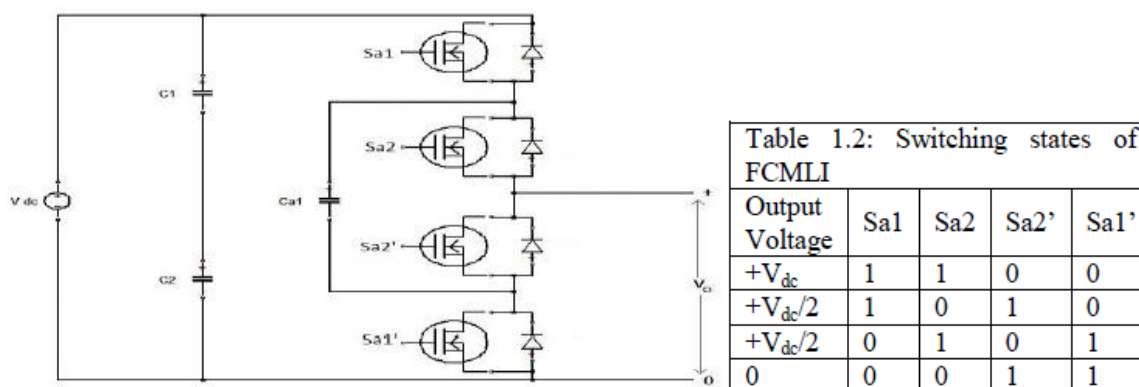

Table 1.2: Switching states of FCMLI				
Output Voltage	Sa1	Sa2	Sa2'	Sa1'
$+V_{dc}$	1	1	0	0
$+V_{dc}/2$	1	0	1	0
$+V_{dc}/2$	0	1	0	1
0	0	0	1	1

Fig.1.6: One leg of flying capacitor inverter circuit.

3.3: Cascaded Multilevel Inverter Technique (CMIT):

A cascaded multilevel inverter consists of single phase, full H bridge inverter units. The general function of this multilevel inverter is to synthesize a desired voltage from several separate dc sources, which may be obtained from batteries, fuel cells, or solar cells. Unlike diode clamped inverter or flying capacitor multilevel inverter, cascaded multilevel inverter does not require any voltage clamping diodes or voltage-balancing capacitors.
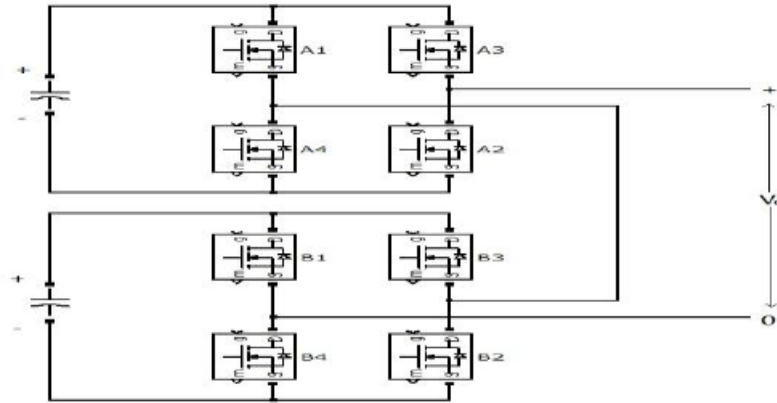
Fig.1.7: One leg of cascaded inverter circuit.
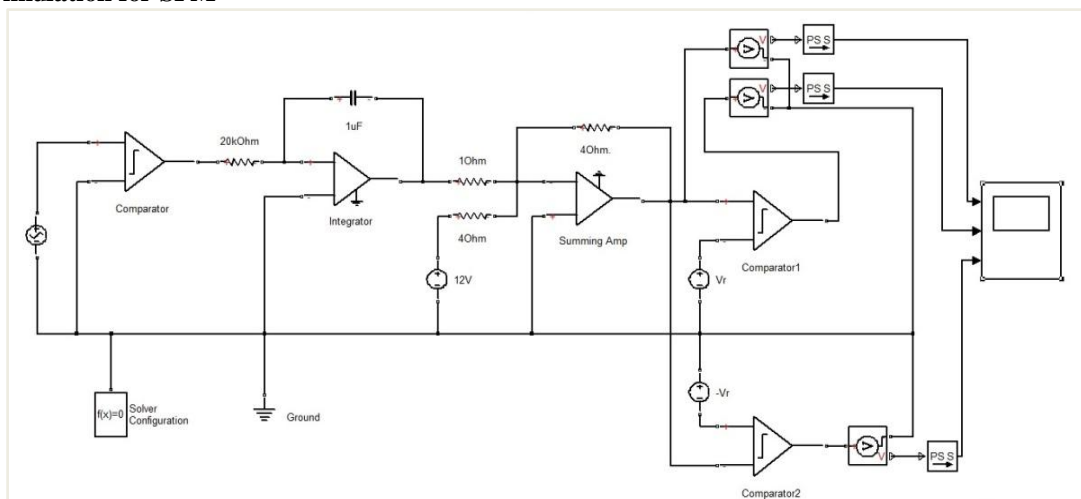
IV. Simulations

4.1: Simulation for SPM

Fig.1.8: Single phase SPM
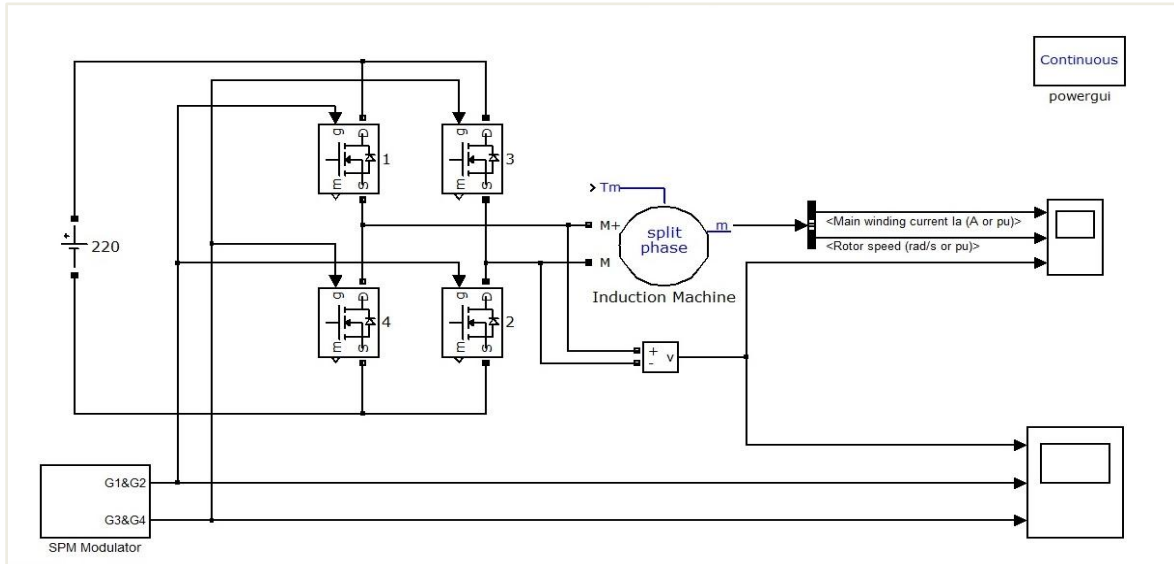

Fig.1.9: Single phase SPM output

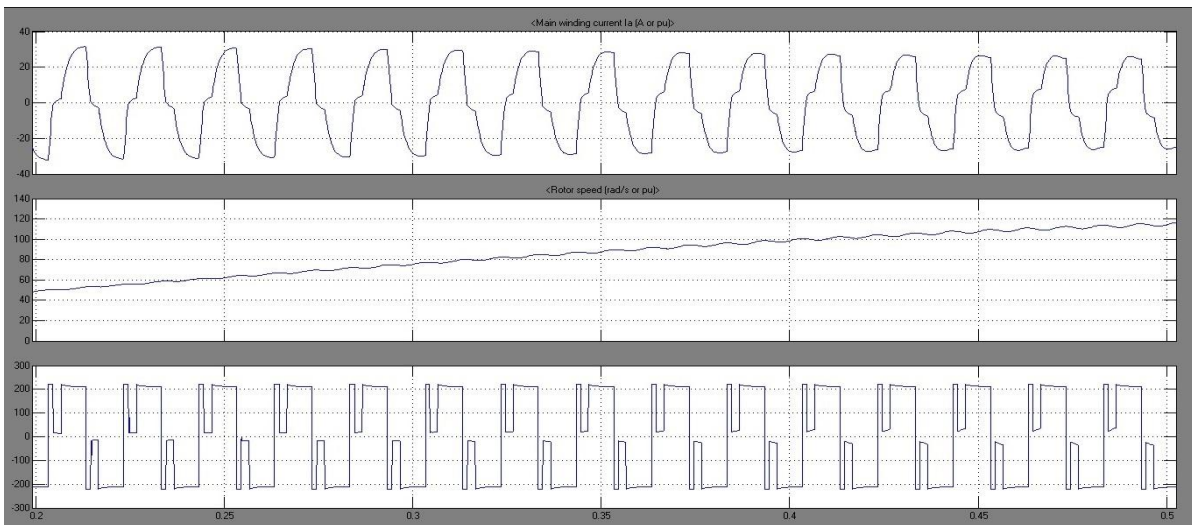**Fig.2.1:** Single phase SPM applied to induction motor.

Fig.2.2: Output of single phase SPM applied to induction motor.
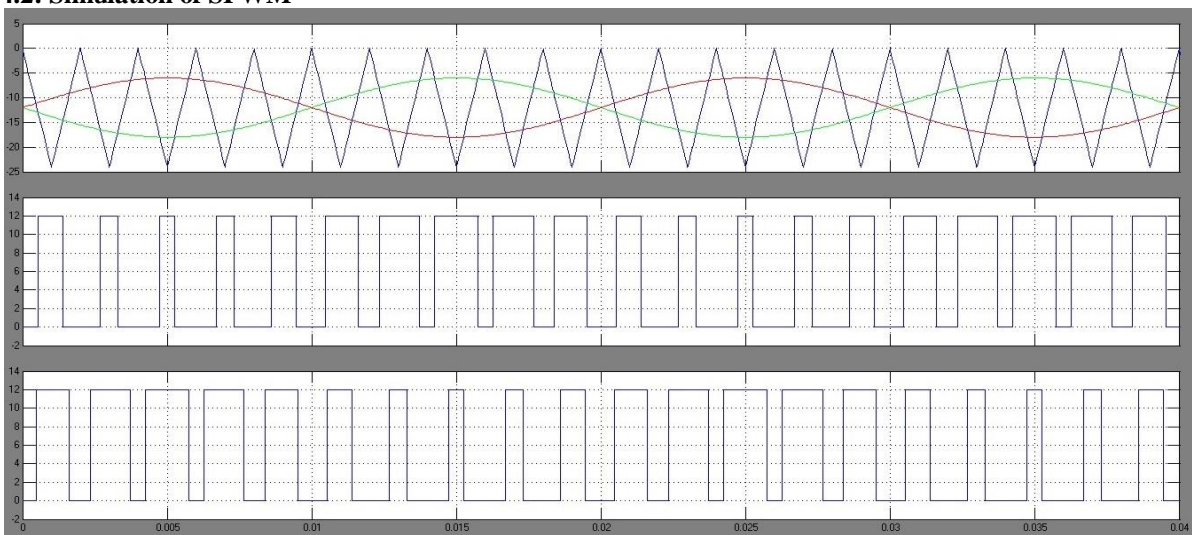
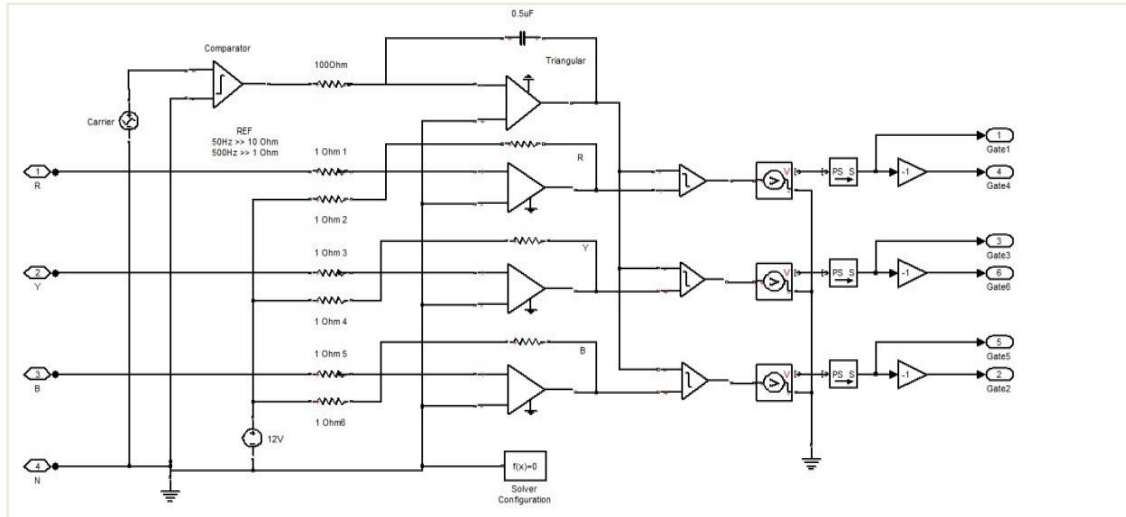## 4.2: Simulation of SPWM

Fig.2.3: Single phase SPWM gate pulses.

Fig.2.4: Three phase SPWM gate pulse generation
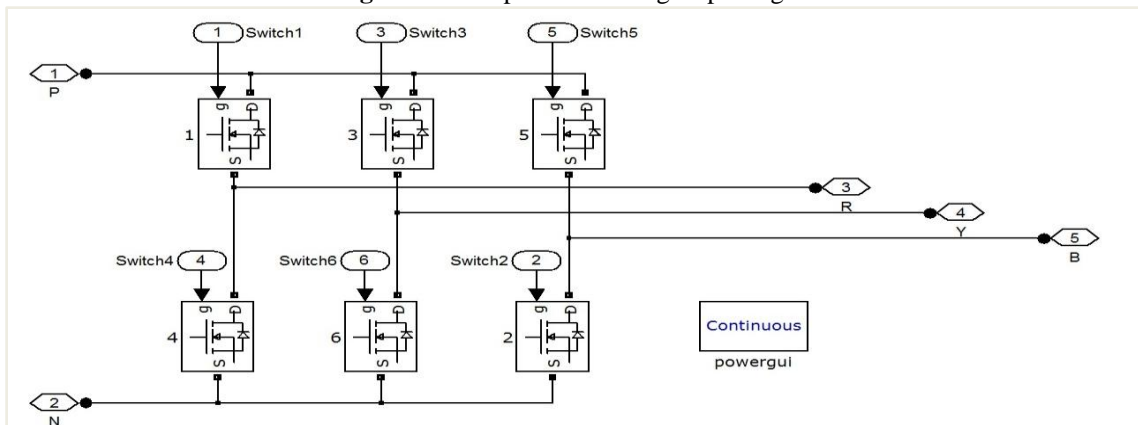
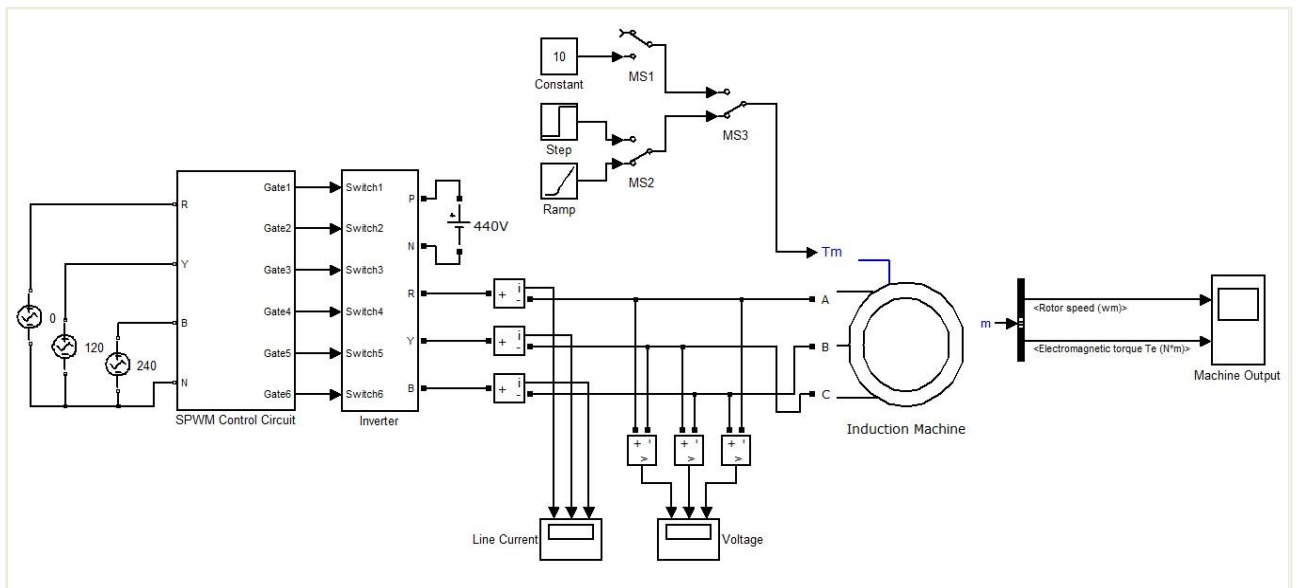**Fig.2.5:** Three phase inverter circuit.

Fig.2.6: Three phase SPWM applied to induction motor
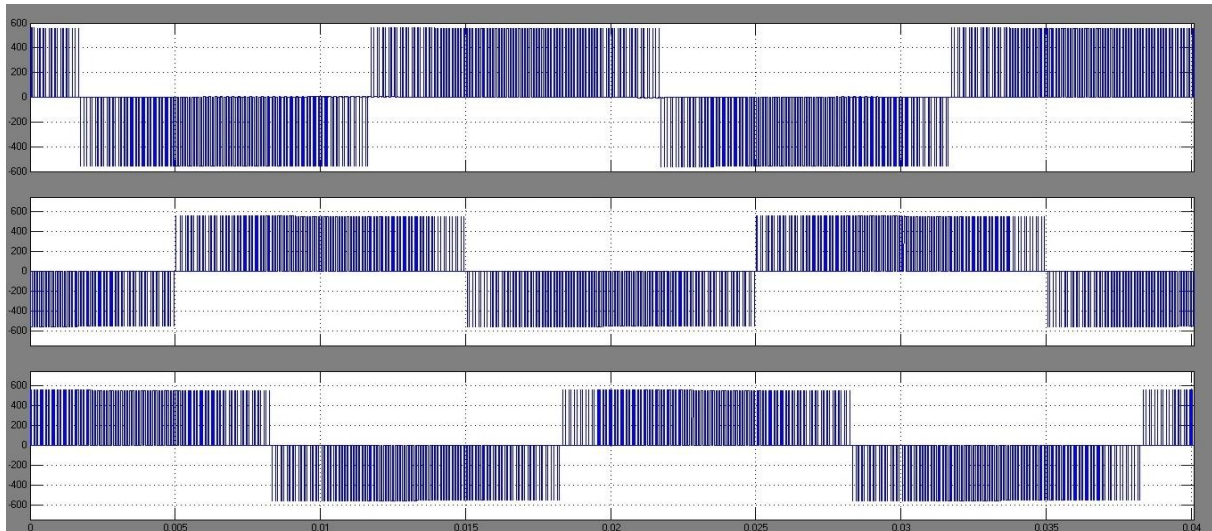
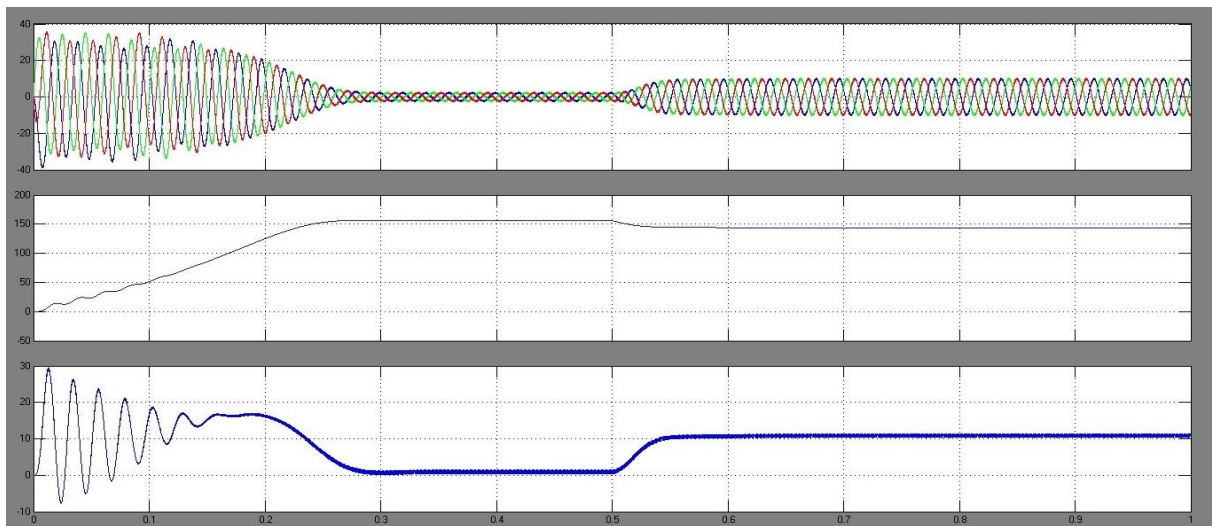**Fig.2.7:** Three phase SPWM output voltage waveforms.

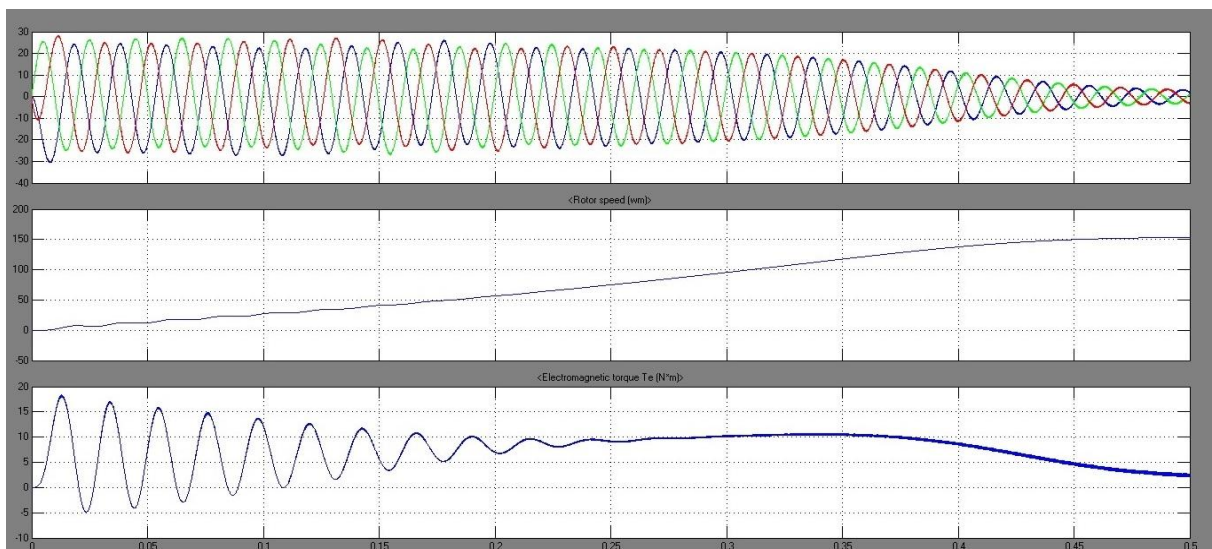**Fig.2.8:** Three phase SPWM line current, speed and torque waveforms.

Fig.2.9: Three phase SPWM line current, speed and torque waveforms with constant load.

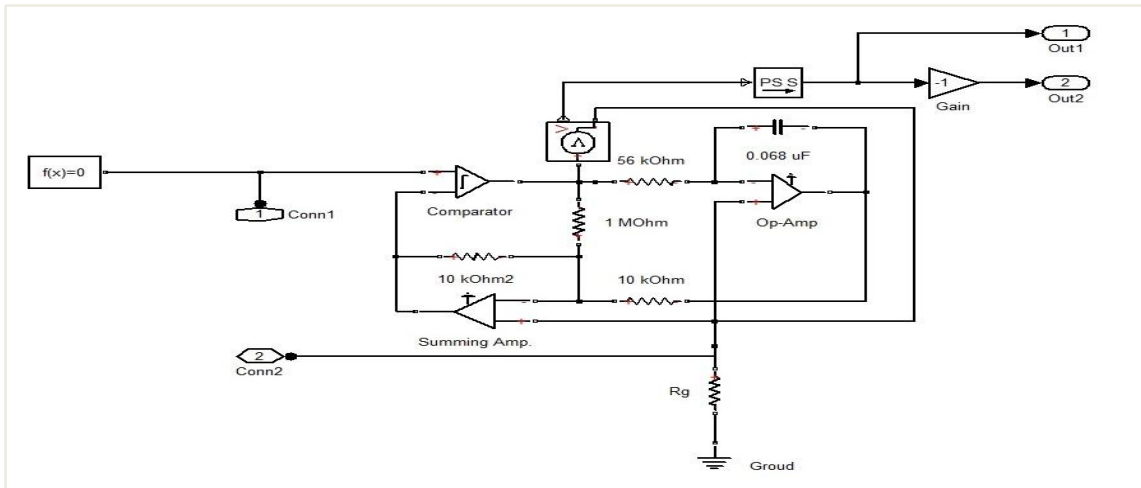**4.3: Simulation of Delta Modulation**.

Fig.3.1: Delta modulation circuit.

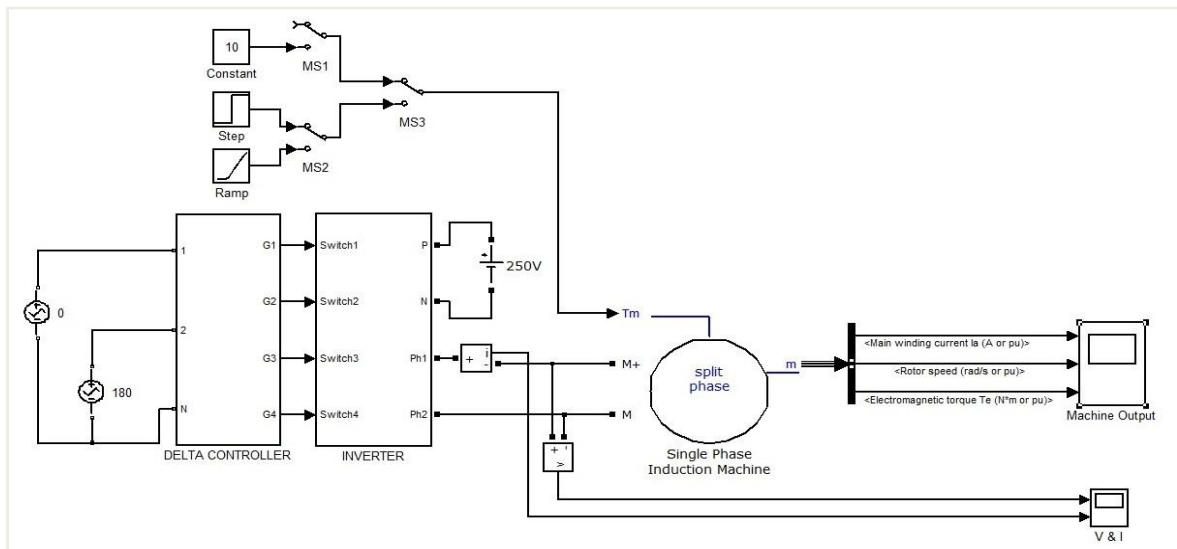**Fig.3.2:** Single phase implementation of delta modulation.
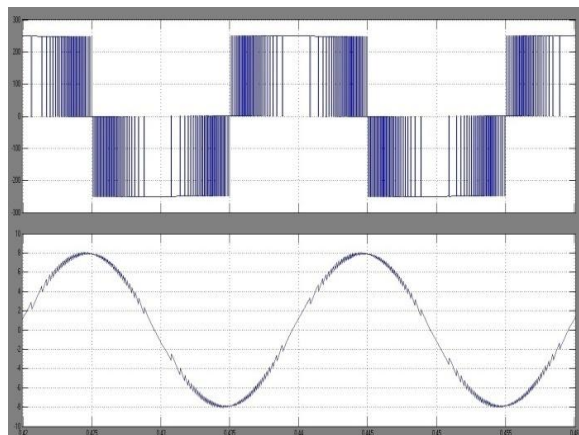
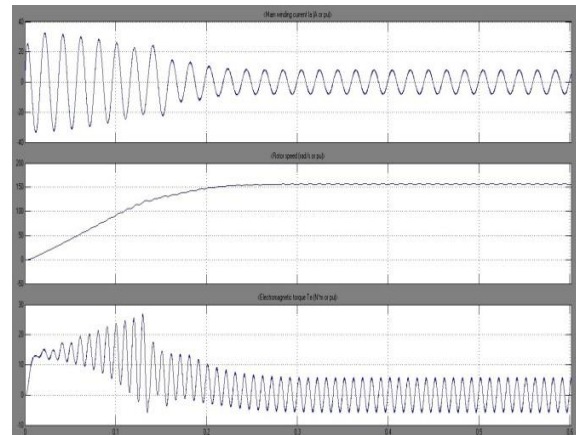**Fig.3.3:** Output voltage and current waveform   **Fig.3.4:** Output current, speed and electromagnetic torque
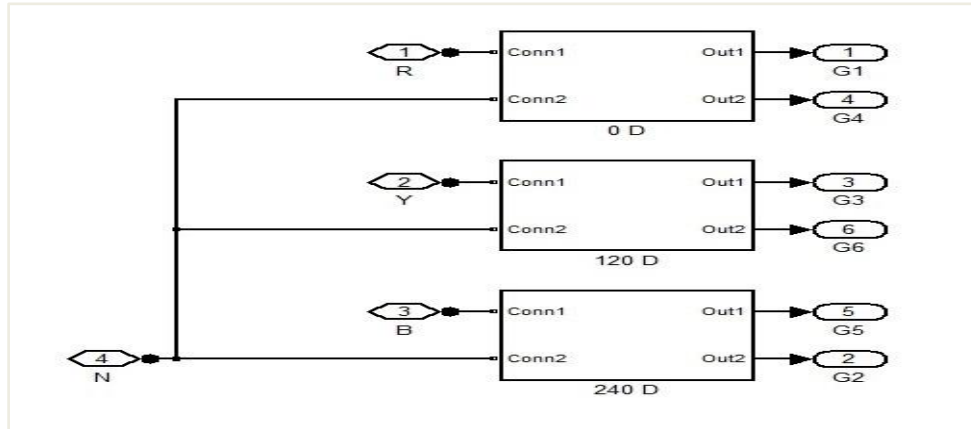
Fig.3.5: Three phase implementation of delta modulation.
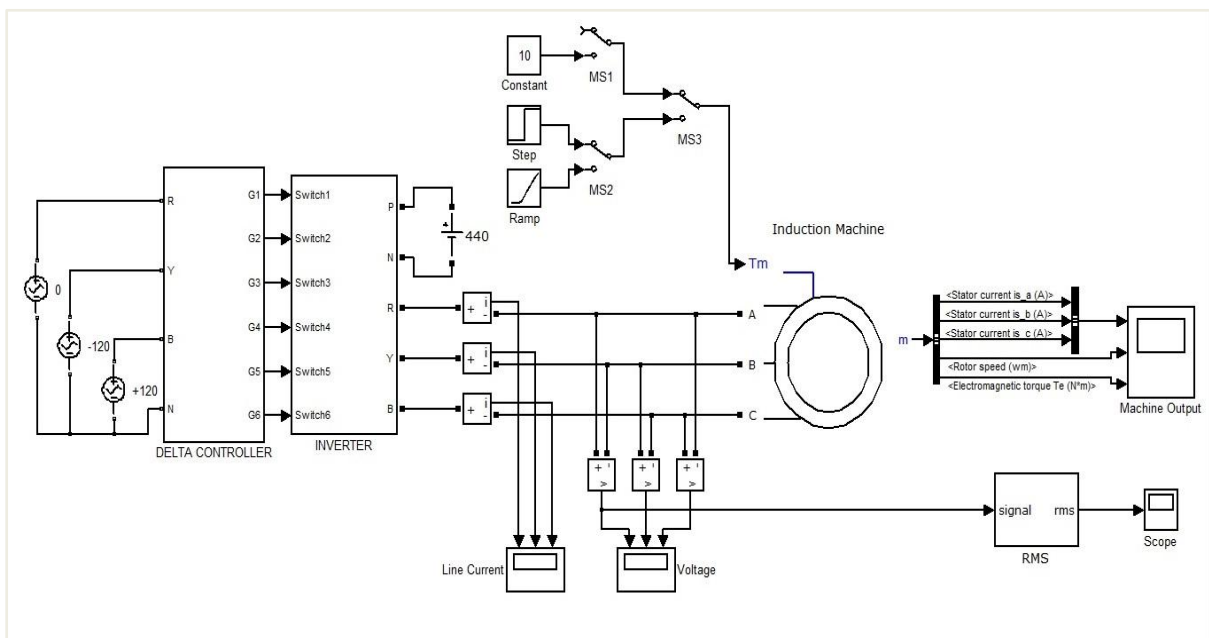

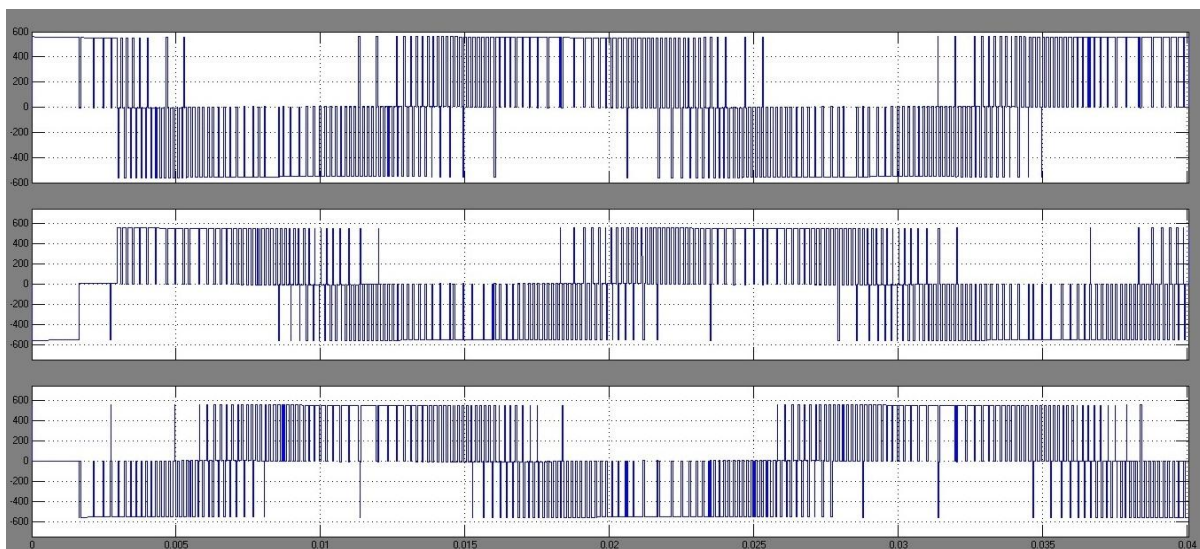**Fig.3.6:** Block diagram of three phase implementation of delta modulation.

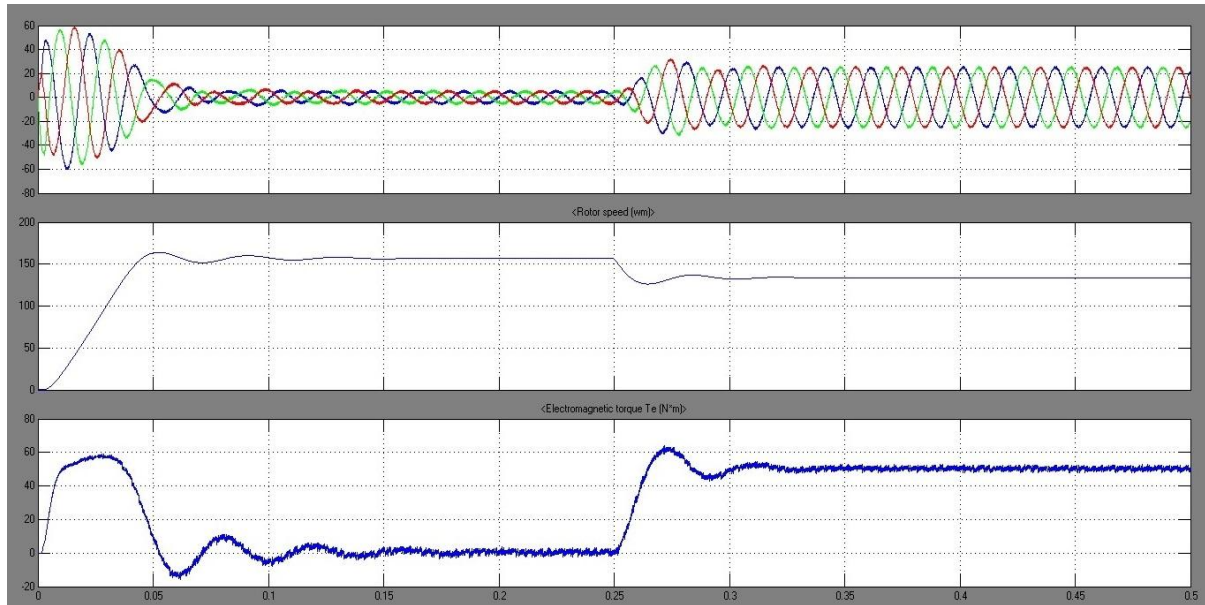**Fig.3.7:** Three phase output line voltage waveforms of delta modulation

Fig.3.8: Line current, speed and electromagnetic torque in three phase DM inverter

V.   Results And Discussion

5.1: Harmonic Content Analysis

Table: 1.3								
Modulation Technique	Single Pulse-width Modulation (SPM)							
Applied DC Voltage (in Volt)	440							
Frequency (in Hz)	50							
RMS Value (in Volt)	381.4918							
Total Harmonic Distortion	0.5970							
Harmonic Content								
	Fundamental	3rd	5th	7th	9th	11th	13th	15th
Volt	463.2319	94.7276	162.3614	120.1473	62.4890	74.7523	60.6352	17.5475
%	100	20.45	35.05	25.93	13.48	16.14	13.09	3.79

Table: 1.4								
Modulation Technique	Sinusoidal pulse Width Modulation (SPWM)							
Applied DC Voltage (in Volt)	440							
Frequency (in Hz)	50							
RMS Value (in Volt)	230.9213							
Total Harmonic Distortion	1.3936							
Harmonic Content								
	Fundamental	3rd	5th	7th	9th	11th	13th	15th
Volt	190.3956	0.0026	0.0052	0.0042	0.0024	0.0030	0.0054	0.0028
%	100	0.00137	0.00273	0.00220	0.00126	0.00157	0.00284	0.00147

Table: 1.5								
Modulation Technique	Delta Modulation (DM) 3 Phase							
Applied DC Voltage (in Volt)	440							
Frequency (in Hz)	50							
RMS Value (in Volt)	349.2848							
Total Harmonic Distortion	0.8390							
Harmonic Content								
	Fundamental	3rd	5th	7th	9th	11th	13th	15th
Volt	378.4159	0.7234	1.2024	0.6445	1.3875	1.7993	0.7178	0.9861
%	100	0.19116	0.31774	0.17031	0.36667	0.47548	0.18968	0.26058

5.2: Discussion
* From the simulation results and harmonics analysis the percentage utilization of dc supply were calculated. Percentage utilization in delta modulation is 79.38% where as that of SPWM is 52.48%. Thus delta modulation is better in utilization of source.
* Harmonic content in SPM is quite more than that of SPWM and delta modulation. In SPWM and delta modulation the harmonic content are nearly equal.

VI.   Conclusion

From the study of different modulation techniques and multilevel inverter concepts we conclude that, SPM modulation technique produces more harmonic content even with multilevel inverters. So it is not a reliable method to implement in ac drives. SPWM minimizes the harmonic content in output voltage but has low percentage dc utilization. Voltage to frequency ratio in SPWM is not constant. The delta modulation provides constant V/Hz up to defined value of frequency. The transition between the constant V/Hz and constant V regions is smooth. Low commutation rates for higher modulation index. On and off time of switches never falls below a given minimum value in delta modulation technique. Output voltage of a multilevel inverter has resemblance with pure sinusoidal waveform. By using multilevel inverter the harmonic content can be reduced up to some extent provided the pulse widths or switch on time of different dc voltage levels are optimized. Higher the level of inverter lesser the harmonic contents. But for higher levels circuit equipment like switches, capacitors and diodes are more. So the cost of the devise is more. Circuit complexity also increases with higher level inverters. Thus much higher level inverters are not preferable for practical application.

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