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The intertwined features of trap charges and surface mobility in the MOS and MOSFET Devices fabricated on elemental Silicon and compound semiconductors such as Silicon Carbide and Gallium Nitride

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Abstract: *4H-SiC and GaN (0001) oriented surfaces compare to the Si (111) surface in terms of planar density of atoms, therefore the charge densities in MOS devices fabricated on these surfaces can be compared. The positive charge and deep "Border" trap densities in the MOS devices on 4H-SiC (0001) surface and the Si(111) surfaces correlate to each other with the charge and trap density in the 4H-SiC MOS devices being three times those in the Si MOS devices at 12 x $10^{11}/cm^2$in the wet oxidised/wet re-oxidised/Ar annealed sample. The N_f values in the p-type and n-type devices on Si-face of 4H-SiC create a window of 36 x $10^{11}/cm^2$ as the charge density. Moving the window to the left through processing increases the leakage current and lowers the oxide breakdown field. Moving the window to the right increases the density of near interface traps (NITs) that reduces the surface mobility of the n-channel MOSFET. A high value of interface trap density implies a higher density of carbon atoms at the SiC/SiO_2 interface. The window of ΔN_f could be related to the density of P_{bC} centres on 4H-SiC which is found to be 30-40 x $10^{11}/cm^2$. One-third of the window represents density of E' centres near the SiO_2/Si(111) interface at 12 x $10^{11}/cm^2$ because of absence of carbon and indicates better interface abruptness. The surface mobility in MOSFETs formed on SiC and GaN are dominated by Coulomb scattering when the mobility is shown to be inversely proportional to the total interface and near interface trap densities at room temperature. This relation gives a surface field effect mobility of electrons on n-channel 4H-SiC MOSFETs to be about 45 cm^2/V-s with the oxide having a high breakdown field of 7.8 MV/cm with charges. This mobility is observed experimentally on 4H-SiC MOSFETs having NO annealed oxides. A higher mobility on n-channel MOSFETs fabricated on (1120) surface has a lower oxide breakdown of about 5MV/cm due to the presence of high density of positive fixed charges in the p-type MOS devices. The MOSFETs on GaN surface is expected to have a similar behaviour as on 4H-SiC giving low mobility of about 45 cm^2/V-s as the trap densities are of the same order of low $10^{12}/cm^2$eV.*

Keywords: *MOS Devices, Si, 4H-SiC, 2H-GaN, Donor and Acceptor traps, surface mobility, Oxide breakdown*

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I. Introduction

An energy barrier between two dissimilar materials forms the founding concept for a diode and therefore of the entire field of Electronics. The "coherer" in the early days of radio telegraphy was one of the first diode device used by Hughes and Branly, followed by the mercury coherer detector devised by Bose in 1899 [1]. The coherer can be modelled as a diode in series with a capacitor having one end grounded. This circuit works as a peak-detector. A brief write-up of the making of a Si MOSFET is the way the author wishes to introduce this article. After the Vacuum tube triode invented in 1907 by De Forest and perfected by 1912-13, J.E. Lilienfeld from Germany came to USA as a physicist and electrical engineer and first patented the solid-state Field Effect Transistor (FET) in Canada in 1925 and then in USA in 1926 and 1928. But practically, the FET did not work. Oskar Heil also had a similar device with a British patent in 1935. Lileinfeld however, was able to make an electrolytic capacitor successfully in 1931, the design of which is still used. A team of Shockley, Bardeen and Brattain started work on the MOSFET. When the FET did not work, Bardeen pointed out that the presence of "surface states" is preventing the voltage signal to control the charge at the semiconductor surface. This was 1946. The team then in December 1947 successfully made a point-contact transistor on a piece of Germanium semiconductor when Brattain devised a double point gold contact. This was a p-n-p Bipolar Junction Transistor (BJT). It worked as a common-base voltage amplifier. Since the surface state problem was overcome by oxidising the semiconductor surface, the BJT was modified further to make a Si MOSFET in 1960 by Kahng and Atalla. It took 35 years for some dedicated, talented and learned scientists and engineers to come up with the device. Some of the concepts involved are: surface states, Fermi-level pinning,

metal-semiconductor contacts, passivation of surface states, bipolar and unipolar conduction etc. It can take a long time for a newcomer to fully understand the making and working of the BJT and MOSFET devices, which is really a game of 'charge control'. The device evolved into integrated circuits and systems. There are myriads of integrated electronic systems developed since the invention of the transistor. A computer is one such system. Research in many data intensive research areas or areas involving long computation times, which were not possible earlier without a computer, are now possible, such as weather prediction or studies in the fields of Genetics, Bioinformatics and Biotechnology and in the fields of security and management. Electronic Voting Machine in India is a microprocessor based integrated system that eased the burden of monitoring and counting votes during political elections. The technology has made life easier. Today, one interacts with another far away on the other side of the globe, or communicates from far away distances in Space with ease. . It is 2019 now, and in 59 years since the invention of the MOSFET in 1960, so much of hardware and software has developed!

This article in the beginning determines the planar density of atoms on the Si (111) surface and the hexagonal planes of 4H-SiC and 2H-GaN (0001) surface and shows that they are nearly equal, and therefore the charge densities on MOS devices in Si (111) are comparable to those in MOS devices on 4H-SiC and 2H-GaN having (0001) orientation for similar processing temperatures. The article further brings out limits to the surface field effect electron mobility in n-channel MOSFETs on 4H-SiC and 2H-GaN compound semiconductors. It also shows a more clear correlation of the positive fixed charge and border trap densities in Si/SiO_2 and 4H-SiC/SiO_2 systems again, by summarising the analysis in a Table. The article finally provides evidence to show that removing carbon reduces negative charges and adding oxygen adds negative acceptor states making the D_{it} distribution with energy in the band gap asymmetric [2-4].

II. Theory

Silicon has a diamond lattice structure that belongs to cubic crystal family. It can be seen as two interpenetrating face-centred-cubic (fcc) sub-lattices with one sub-lattice displaced from the other by one quarter of a distance along a diagonal of a cube, that is, a displacement of a $\sqrt{3}/4$ [5]. The planar density (PD) of atoms on the Si (100) and Si (110) and Si (111) surface can be calculated by knowing the number of atoms on the plane and dividing by the area of the plane. The lattice constant for Si is 0.543 nm denoted by 'a'. The number of atoms on the three faces are 2 on each face, and the areas of the planes are a^2, $a\sqrt{}$ 2a, and $\{(1/2) \times (\sqrt{2}a) \times ((\sqrt{2}a\ (\sqrt{3}/2)) = a^2\sqrt{3}/2\}$, giving PDs tabulated below in Table I. The area of a hexagonal plane is given by 2 times the area of a trapezoid having two parallel sides as 'a' and '2a' and a height of $(a\sqrt{3}/2)$. This equals $(3\sqrt{3}/2)\ a^2$. PD for the hexagonal closely packed (hcp) crystal plane of 6H-SiC or 4H-SiC having (0001) surface orientation and GaN having (0001) surface is therefore given as below in Table I. 'a' for 4H-SiC is 0.3073 nm and for GaN is 0.3186 nm. The number of atoms in the 4H-SiC (1120) plane or a-face is 5/3, and the area of the plane is 'a' x 'c', where a = 0.3073 nm and c = 1.0053 nm for the 4H-SiC polytype. It can be observed that the density of atoms on 4H-SiC (0001) and GaN (0001) face is nearly the same as on Si (111) face. The comparison of N_f values in oxides on 4H-SiC and GaN MOS devices should therefore be made with those in oxides grown on Si (111) face. The PD on a clean semiconductor surface represents P_b centres which act as surface recombination centres. These states on Si surface reduce to 10^{11}-$10^{12}/cm^2$ after oxidation [6, 7].

Table I. Planar density of atoms on the Si cubic faces and on SiC and GaN (0001) hcp faces.

Si(100) (x $10^{14}/cm^2$)	Si(111) (x $10^{14}/cm^2$)	6H-or 4H-SiC (0001) hcp plane (x $10^{14}/cm^2$)	4H-SiC (1120) hcp plane (x $10^{14}/cm^2$)	GaN (0001) hcp plane (x$10^{14}/cm^2$)	Ratio of PD Si(111) / Si(100)	Ratio of PD of 4H-SiC (0001) / Si(111)	Ratio of PD of 4H-SiC (0001) / Si(100)	Ratio of PD of GaN (0001)/ Si (111)
6.7	7.8	8.1	5.4	7.6	1.16	1.04	1.21	0.97

The electrically inactive fixed charges and the three types of interface traps existing in the SiC/SiO_2 system are distinguished. They are tabulated below in Table II. One is at the interface only, and arises from the so-called P_b centres or P_{bC} centres [8]. A P_b centre is Si atom connected to three Si atoms at the interface with one dangling bond or a dangling bond on the second Si atom connected to the Si atom below it. These are known as P_{b0} and P_{b1} in the Si Science and Technology where their density is about $10^{12}/cm^2$ to $10^{13}/cm^2$ on the p-Si (111) surface [9]. The density of P_{b1} is less than the density of P_{b0}. The P_{b0} centre on Si (111) is just denoted as P_b centre [8]. The P_{bC} centres are carbon-dangling bonds on the 4H-SiC surface. There density is found to be 3-4 x $10^{12}/cm^2$ [10]. Similar to P_{bC}, there should be P_{bN} centres of Nitrogen dangling bonds on the 2H-GaN surface having the expected density to be same as in 4H-SiC at 3-4 x $10^{12}/cm^2$. The Si/SiO_2 system has only P_b centres but the SiC/SiO_2 system has both P_b and P_{bC} centres due to Si and C dangling bonds. They can acquire a positive or negative charge and are therefore amphoteric. There is another type of interface traps in the SiC/SiO_2system that arise due to sp^2-bonded carbon clusters and graphite-like carbon [11]. These are mainly donor states or hole traps in the lower half of the SiC bandgap with the intrinsic Fermi level shown to be at E_c-

0.97 eV in 4H-SiC due to intrinsic defect density of 1.1 x 10^{14}/cm^3 [12-13]. Being donor states, they are neutral when occupied with electrons and become positive upon donating an electron or capturing a hole. These add positive charges to p-type MOS device when the Fermi level is near the VB and when the donor states are empty and therefore positively charged. Donor states due to sp^2 bonded carbon and graphite like carbon are reduced in number because they are oxidised in oxygen ambient. High temperature inert anneal in N_2 or Ar gas has high density of donor states and low temperature inert anneal has low density of donor states, so N_f is accordingly higher or lower due to inert anneals [14-16]. The small upper half of the 4H-SiC bandgap of 0.97 eV above the intrinsic Fermi level also has acceptor states coming from sp^2 bonded carbon and graphite like carbon that have been shown to be passivated by NO annealing and add to the traps near VB after being passivated with N [4]. The acceptor states are negative when occupied and neutral when empty. The donor states occupy almost two-thirds of the 4H-SiC bandgap below the intrinsic Fermi level are much larger in density with the sp^2 bonded carbon states starting from E_v + 1.4 eV [11]. The above two types of interface traps are represented as D_{it}. The contribution to D_{it} from the P_b centres is not observed in Si-face of 4H-SiC/SiO_2system by Afanasev et al. [11]. However, after wet re-oxidation [17], the donor states are reduced and acceptor states are increased as observed in Fig. 2 of the report by Williams et al. [4] making the D_{it} distribution asymmetric after re-oxidation. The third type of traps at the SiC/SiO_2 interface are called "border" traps, which are present in the oxide within about 3 nm of the interface and can exchange charge with the Si or SiC CB [18-19]. These are represented as D_{bt} or D_{NIT}. It is difficult to distinguish between the three types of traps by electrical characterisation methods except the fact that border traps are dominant at low frequencies of less than 100 Hz [20-21]. It is to be noted that D_{it} at E_c-0.2 eV is not necessarily the same as D_{NIT} near CB of the semiconductor unless D_{it} is passivated substantially. In the as oxidised dry or wet oxide on Si-face of 4H-SiC having (0001) orientation, the D_{it} at E_c-0.2 eV is at 24 x 10^{11}/cm^{2}eV with Ar annealing gas containing small parts of oxygen [3-4]. Wet re-oxidation at 950^{o}C for 3 hrs has shown to reduce the donor states and increase the acceptor states as mentioned earlier [4]. Similar to 4H-SiC, the intrinsic Fermi level in GaN is shown to be at E_c-0.95eV with the intrinsic defect density of 2.7 x 10^{15}/cm^3 [12-13]. The upper half of the bandgap above the intrinsic Fermi level has acceptor states and the lower half of the bandgap below the intrinsic Fermi level has donor states which forms 72% of the bandgap. The different interface traps are also shown in a schematic diagram of the density of interface traps as a function of trap energy in Fig. 1 of the study by Krieger et al. [22]. The figure also shows the energy-band diagram of a SiO_2/4H-SiC MOS structure indicating the energetic and spatial position of carbon related interface traps and near interface traps (NITs). Knaup et al.[23] performed a density functional study on NITs and identified Si interstitials and carbon dimmers as the source of NITs. The electrically active interface traps at the Si/SiO_2 and 4H-SiC/SiO_2 interfaces, as well as the electrically inactive fixed charges in the SiO_2 are tabulated below in Table II and is also described in the author's earlier study [2]. They are described again in this article to make the article independent and also include the facts about GaN/SiO_2 system.

Table II. Electrically active interface states and inactive fixed charges in Si and SiC MOS devices

Semiconductor	Electrically active interface states that exchange charge with CB or VB			Electrically inactive fixed charges in the oxide that do not exchange charge with CB or VB
Si (111)	P_b		Donor type border traps near CB, Si-O-O-O	Si-O
4H-SiC-Si-(0001)	P_{b0}, P_{b1}, P_{bC}	sp^2-bonded carbon and graphite	Acceptor type border traps near CB, Si-C-O-O	Si-C-O

In MOS devices on semiconductors such as Si and SiC and GaN, the upper half of the bandgap has acceptor type interface states and the lower half has donor type of interface states [24-25]. Oxidised Si (111) has shown donor type interface states in the upper half of the bandgap also [26]. Donor states at the semiconductor/insulator interface are neutral when filled with electrons and become positive after donating electrons (empty) or capturing holes. In the p-type MOS device, the Fermi level is close to the VB. The donor states are empty and are therefore positive. They can represent positive charge in the p-type MOS device coming from donor states. Acceptor states at the semiconductor/insulator interface are negative when filled with electrons and become neutral after donating the electrons (empty). In the n-type MOS device, the Fermi level is close to the CB. The acceptor states are filled and are therefore negative. They can represent negative charge in the n-type MOS device coming from acceptor states. Fixed charges in MOS devices could be positive or negative. They do not exchange charge with the CB. In Si, they can come from Si-O bonded excess Si and are usually positive only due to incomplete oxidation. In SiC, they can come from Si-C-O bonded excess Si or C and O. Excess Si will give positive charges, such as in p-MOS device on 4H-SiC-Si-face [17, 27-28] and excess C will give negative charges in MOS device, such as in C-face of 4H-SiC [29]. The observed low-field

leakage current in this device of 10^{-8}A/cm^2 is more than the oxide displacement current of 5 x 10^{-9}A/cm^2 indicating the absence of NITs and presence of bulk defects due to carbon [29-31]. Absence of NITs on the C-face of 4H-SiC results in large field effect (FE) surface mobility of about 90-118cm^2/V-s which increases to 80-127 cm^2/V-s after H_2 POA [32] but has a low oxide breakdown of about 5MV/cm due to large number of negative fixed charges and bulk defects mainly due to excess carbon [29]. After NO annealing, the FE mobility in n-channel MOSFETs on the c-face of 4H-SiC is identical to that on Si-face at about 35cm^2/ V-s [33].

The Current-Voltage and low frequency (less than 0.5 Hz) and high frequency (1MHz) Capacitance-Voltage traces in a MOS device are interrelated [30]. The oxide breakdown field is obtained from the high field FN tunnelling current-voltage curve. The oxide is said to be in breakdown condition when the current density reaches 10^{-4} A/cm^2 in thick oxides of tens of nanometres. The oxide voltage is corrected by the flat band voltage, and the flat band voltage is obtained from the high frequency C-V trace [34-35]. The breakdown field is obtained from the slope constant B, of the high-field I-V trace and needs to be corrected by the amount of charges in the oxide represented by the flat band voltage. This is the first interrelation. The low voltage leakage current density in the MOS device reduces below the displacement current in the oxide because of trapping electrons in the NITs at the CB edge. The observed low current density can provide the capacitance of NITs at 300K [30]. The capacitance can give the density of the traps at 300K, which can be further extrapolated to 10K temperature by lowering the average electron energy and thus coming closer to the CB edge. Thus the distribution of the D_{NIT} in sub-0.026 eV from the accumulated CB edge can be obtained. Here, the leakage current is related to the low frequency C-V trace. This is the second interrelation. The oxide breakdown and the D_{NIT} can be found on MIS devices fabricated on simple and compound semiconductors like Si, SiC and GaN [30-31]. There is a limitation imposed for the design of a high mobility n-channel MOSFET on simple and compound semiconductors such as Si, SiC and GaN. Reducing NITs near the CB increases leakage current and lowers oxide breakdown strength by increasing the FN tunnelling current. The switching states (NITs) convert to fixed states (fixed oxide charges) due to either processing with O, N, H or by forming gate stacks such as SiO_2/Al_2O_3. The fixed charges are positive charges for the p-substrate MOS that increases the cathode field for electron tunnelling in the n-channel MOSFET, thereby increasing the current and lowering the breakdown field. The fixed charges are negative charges for the n-substrate MOS that increases the anode field for hole tunnelling in the p-channel MOSFET, thereby increasing the current and lowering the breakdown field [2, 31, 36]. The positive charge and deep"Border" trap densities in the MOS devices on the two surfaces of Si (111) and 4H-SiC-Si-face having (0001) orientation correlate to each other with the charge and trap density in the 4H-SiC MOS devices being three times those in the Si MOS devices at 12 x 10^{11}/cm^2 in the wet oxidised/wet re-oxidised/Ar annealed sample [2].

III. Results and Discussion

It is observed that the dry oxidation of n-type Si-face 4H-SiC or 6H-SiC surfaces followed by inert anneal in pure Ar gives a high density of sp^2 bonded carbon and graphite-like states at the oxide/SiC interface that is shown as negative acceptor states giving high negative fixed charge density due to the deep traps. A 10^{20}/cm^3 carbon is detected [3]. It has been pointed out that acceptor states show up as negative fixed oxide charges in the n-type MOS device with the Fermi level close to the CB and all the states below the Fermi level being occupied with electrons. Annealing the pure Ar annealed device in low partial pressure of O_2 (0.001% O_2) at 1500^{o}C for 1 minute removes a lot of the carbon to 10^{18}/cm^3 level thereby reducing the acceptor states or the negative charges in the n-MOS device [3]. Surface carbon density now becomes 2 x 10^{11}/cm^2 for a 2nm interface. The 1MHz high frequency C-V curve shifts left because of removal of carbon. Some positive charge remains which is due to Si-C-O bonded excess Si in the MOS device. These charges are electrically inactive and the N_f obtained is 12 x 10^{11}/cm^2 [3]. Similar observation is made on the MOS device on Si-face of 6H-SiC by Tyagi et al. [37], although 6H-SiC MOS device has less acceptor states near CB. The above analysis deals with removal of carbon to remove negative charges or indirectly add positive charges, shifting the C-V curves to the left. Now, consider the case of wet oxidation to fabricate an n- type MOS device [17]. After wet oxidation followed by inert anneal in Ar, the sp^2 bonded carbon states are present giving negative N_f value of -12 x 10^{11}/cm^2. When this oxide is wet re-oxidised at low temperature of 950^{o}C for 3 hrs, the Si-C-O-O acceptor states having a density of 12 x 10^{11}/cm^2 are formed along with the present sp^2 bonded acceptor states and the total acceptor trap density increases to 24 x 10^{11}/cm^2 giving negative N_f of -24 x 10^{11}/cm^2 in the n-type MOS device [4, 17]. Consider the wet oxidation of p-type MOS device. Wet oxidation of the 4H-SiC surface at 1100^{o}C followed by inert Ar anneal forming a p-type MOS device [17] results in N_f of 24 x 10^{11}/cm^2. The donor states density of 12 x 10^{11}/cm^2 come from the sp^2 bonded carbon and electrically inactive positive charge density of 12 x 10^{11}/cm^2 come from Si-C-O bonds. After wet re-oxidation at 950^{o}C for 3 hrs, 12 x 10^{11}/cm^2 positive charge density coming from the formation of E' centres remain, and the fixed oxide charges from the Si-C-O bonds become negligibly small in density. NO annealing at 1150^{o}C for 2 hrs causes some fresh oxidation of the interface increasing the oxide thickness at the rate of about 2nm/hr. N replaces O and adds a

positive charge as it has one less electron as compared to oxygen. Therefore, the positive charge density in the p-type MOS device doubles and the E' centres which originally had an unpaired electron becomes neutral with the addition of 1N in place of 1O. The D_{NIT} after NO annealing is determined to be 24 x 10^{11}/cm^2 [36], implying that the fresh oxidation due to NO is increasing the density of E' centres representing D_{NIT} and also making it neutral due to addition of 1N in place of 1O. The sp^2 bonded carbon trap states at the interface go to the VB edge after bonding with Nitrogen [4]. A Electrically Detected Magnetic Resonance (EDMR) study recently concluded that the interface disorder is higher after NO anneal and hence the interface abruptness will also be worse than before NO annealing [38]. The above analysis is summarised in the Table III below.

Table III. Processing effects on the wet oxidised 4H-SiC Si-face (0001) oriented surface [4, 17, 36].

Device type	N_f in p-type MOS (x 10^{11}/cm^2)	N_f in n-type MOS (x 10^{11}/cm^2)	ΔN_f window between the p- and n-type MOS devices (x 10^{11}/cm^2)
High temperature (1100^{o}C) wet oxidation followed by Ar inert anneal	24 (12 from sp^2 bonded carbon donor traps + 12 from Si-C-O bonded fixed charges. Donor states are neutral in n-type device.	-12 from sp^2 bonded carbon acceptor traps	36 which appears to be related to P_{bC} density in 4H-SiC
Wet re-oxidation at 950^{o}C for 3 hrs	12 (positive charges from (Si-C-O-O) E' centres + reduced negligible Si-C-O bonded fixed charges	-12 from sp^2 bonded carbon acceptor traps plus -12 (Si-C-O-O) E' acceptor centres giving a total of -24. Acceptor states are neutral in p-type device.	36 which appears to be related to P_{bC} density in 4H-SiC
After NO annealing at 1150^{o}C for 2 hrs causing fresh oxidation at the interface	N replaces O to add a positive charge doubling the density of positive charges	N doubles the density of E' centres and makes them neutral, and sp^2 bonded acceptor states are passivated with N to form states near the VB.	

A high temperature dry oxidation at 1150^{o}C with inert Ar anneal gives the same N_f in the n-type MOS device as -12 x 10^{11}/cm^2 as calculated from the study of Dixit et al. on pre-irradiated dry oxide due to the formation of sp^2 bonded carbon traps representing D_{it} [39]. The E' centres representing D_{NIT} are formed due to long time low temperature re-oxidation process. The sp^2 bonded carbon will have 6 electrons including the sigma bond of a carbon dimmer [23], and with 2 x 10^{11}/cm^2 carbon at the 4H-SiC/SiO_2 interface, the total trap density becomes negative 12 x 10^{11}/cm^2 in the n-type MOS device. This means that both wet and dry oxidation at 1100^{o}C or 1150^{o}C followed by Ar inert anneal gives D_{it} of 12 x 10^{11}/cm^2 eV from sp^2 bonded carbon at the interface, which shows as negative N_f in n-type MOS device on 4H-SiC. But after wet re-oxidation at 950^{o}C for 3 hrs, E' centres and the associated positive charges are formed which represent 12 x 10^{11}/cm^2 of border traps or D_{NIT}. It is to be noted that the sp^2 bonded carbon dimmers and E' centres both are acceptor states giving a total of -24 x 10^{11}/cm^{2}eV after wet re-oxidation at 950^{o}C for 3 hrs.

It can be observed from the above analysis that the n-type and p-type MOS devices have 12 x 10^{11}/cm^2 density of positive charges and 12 x 10^{11}/cm^2 density of D_{NIT} or border traps. These charge densities are completely correlated to the charge densities in the Si/SiO_2 system [2]. It is found that the fixed positive charge density N_f, in n-type and p-type MOS devices on Si-face of 4H-SiC compound semiconductor having (0001) orientation is 12 x 10^{11}/cm^2 and the border trap density of deep acceptor traps or density of near interface traps D_{NIT}, is also 12 x 10^{11}/cm^{2}eV after wet re-oxidation at 950^{o}C for 3 hrs of the dry or wet grown thermal oxide [36]. These charge and trap densities are correlated to the charge and trap densities in the Si/SiO_2 system under similar processing conditions such as the final temperature of 950^{o}C or 920^{o}C. Carbon, having two less electrons compared to oxygen, adds positive charge to the Si-C-O bonded molecules, making the increase in densities three times in 4H-SiC/SiO_2 MOS devices. The positive charge density have been found to be 4 x 10^{11}/cm^2 for the dry or wet oxide on n-or p-type MOS devices on Si (111) surface and fast pulled out from the wet oxidising ambient [2, 6], and the lower bound on the border trap density in the Si MOS devices is found to be ~3 x 10^{11}/cm^{2}eV that contribute to the electrical response in the irradiated Si MOS devices [18-19]. These densities are three times less than those in the 4H-SiC/SiO_2system due to the absence of carbon, completely correlating the charges in the two systems. It can also be observed that low temperature wet re-oxidation shifts the N_f window to the right causing positive charge density to reduce to 12 x 10^{11}/cm^2 from 24 x 10^{11}/cm^2. These charges double after NO annealing and so without wet re-oxidation, the positive charge density will double to 48 x 10^{11}/cm^2 after NO annealing. This will increase the leakage current and lower the oxide breakdown, but keep the surface mobility higher because D_{NIT} will not form because of absence of wet re-oxidation [2]. If the lower oxide breakdown is acceptable then re-oxidation is not required and NO annealing can be performed directly after high temperature oxidation and inert Ar anneal.

The author in his previous study describes a new method of finding the density of NITs (D_{NIT}) [30] utilising the raw data of the author's reliable collaborative samples of n-and p-type MOS devices on 4H-SiC (0001) oriented Si surface where the oxide was NO annealed at 1150^{o}C for 2 hrs after oxide growth at 1100^{o}C in a wet ambient, followed by wet re-oxidation at 950^{o}C for 3 hrs [4, 17, 30, 34]. The same method is now used to calculate the D_{NIT} on GaN MOS samples. Two studies have been chosen to provide the data for the calculation of D_{NIT} in GaN MOS devices. One is by Gaffey et al. [40] at Yale University and the other is by Bisi et al [41] at University of California at Santa Barbara. The first one uses a oxide/nitride/oxide of 24 nm equivalent oxide thickness (EOT) as the gate dielectric and the other uses Al_2O_3 with an EOT of 25 nm. The MOS devices in both the studies show a low field leakage current density of 1.0 x 10^{-9} A/cm^2 with the n-type MOS devices in accumulation having positive voltage at the gate. This observed leakage current is about an order lower than the displacement current density in the oxide as given by equation (1) and shown in Table IV below for 24 nm and 25 nm thick oxides. This is indicative of the presence of NITs near CB of GaN as devised and calculated in the author's earlier study [30]. The displacement current density, $J_{D,ox}$ for the thermal SiO_2 having different thickness and for a slowly changing field, such as having a quasi-static voltage ramp rate of 0.1 V/s.

$$I = C\frac{dV}{dt} \qquad (1)$$

$$J_{D,ox} = \frac{\varepsilon_0 \varepsilon_r}{d}(0.1)$$

$$\varepsilon_0 = 8.854x10^{-14} F/cm \ldots; \varepsilon_r = 3.9 \ldots; \varepsilon_0\varepsilon_r = 34.53x10^{-14} F/cm$$

Table IV. Displacement current densities for different oxide thickness.

Oxide thickness (nm)	$J_{D,ox}$ (A/cm^2), (x 10^{-8})
5	6.9
8	4.3
8.5	4.1
10	3.45
20	1.7
25	1.38
40	0.86
45	0.76
70	0.49
80	0.43

The border trap density or D_{NIT} in GaN/SiO_2 MOS device having EOT of 24 nm of oxide/nitride/oxide (ONO) gate dielectric grown by the Jet Vapor Deposition (JVD) method and annealed at 600^{o}C in N_2 for one hr [40], is calculated by the new method as below:

Low field leakage current density = 10^{-9}A/cm^2.
$J_{D,ox}$ = (34.53x10^{-14}(F/cm) x 0.1 /24 x 10^{-7} cm) =0.144 x 10^{-7} A/cm^2=14.4 x 10^{-9} A/cm^2.
$1/C_{NIT} = 1/C_{eq} - 1/C_{ox}$
C_{eq} = Observed J/(dV/dt) = 1 x 10^{-9} (A/cm^2)/0.1V/s= 1 x 10^{-8} F/cm^2
$C_{ox} = J_{D,ox}/(dv/dt)$ = 14.4 x 10^{-9} (A/cm^2)/0.1(V/s) = 14.4 x 10^{-8} F/cm^2
$1/C_{NIT}$ = (1)-(1/14.4) = 0.9305; C_{NIT} = 1.07 x 10^{-8} F/cm^2.
$D_{NIT} = C_{NIT}/(qA(kT))$ = 25.8 x 10^{11}/cm^2 eV.
D_{NIT} for the MOS device having 25 nm EOT of Al_2O_3 is also calculated to be 25.8 x 10^{11}/cm^{2}eV.

The above two devices had a maximum processing temperature of 600-700^{o}C. The MOS device with ONO gate dielectric was annealed in N_2 ambient for 1 hr at 600^{o}C, and the MOS device with Al_2O_3 gate dielectric had a MOCVD growth temperature of 700^{o}C [40-41]. If the growth temperature of MOCVD deposited Al_2O_3 is raised up to 1000^{o}C, then more N is part of the higher D_{NIT} at 40 x 10^{11}/cm^{2}eV as shown by the change in the fixed charge density (N_f) in Table II of the study by Liu et al. [42]. The accumulation to depletion sweep on the n-type MOS device includes charges trapped in (C_{it} + C_{NIT}) and the depletion to accumulation sweep includes charges trapped in C_{it} only. Therefore, the difference in N_f gives the D_{NIT} in the sample [20-21]. The maximum D_{NIT} of about 40 x 10^{11}/cm^{2}eV inform about the density of dangling Nitrogen bonds at the (0001) surface of the 2H-GaN just as in 4H-SiC [2] and appears to be related to the three times larger bandgap of 4H-SiC (3.24eV) and 2H-GaN (3.4eV) as compared to Si having a bandgap of 1.12 eV and a corresponding maximum D_{NIT} (E' centres) of 12 x 10^{11}/cm^{2}eV [2, 30]. Apart from the electrically active D_{NIT}, the absolute value of N_f is positive for the oxide grown at higher temperature of say 1000^{o}C, indicating that there is a large density of electrically inactive positive charges also in the deposited oxide. D_{NIT} obtained by the two C-V traces method utilised above for the devices with the maximum processing temperatures of 600-700^{o}C

[40-41] is same as the D_{NIT} obtained by the low field leakage current method devised by the author [30], the calculation of which is shown above for the MOS device with ONO and Al_2O_3 gate dielectrics [40-41]. The study by Liu et al. [42] presents the change in N_f in Table II of the reference [42]. The interface states are usually determined by the hysteresis in the high frequency (1MHz) C-V traces, but if the density of near interface traps is higher than the density of interface traps, then the hysteresis will determine the D_{NIT} as described above.

A brief discussion on the surface mobility is made next. The surface mobility in inverted Si or SiC MOSFET devices has been modelled for numerical simulation. It has many carrier scattering components, such as surface acoustic phonons, surface roughness, bulk mobility, Coulomb scattering, and high field mobility [43-47]. The bulk mobility is composed of impurity scattering and lattice scattering [48]. The formula for the inversion mobility is given by many research groups [43-47] as:

$$\mu_{inv} = \left[\frac{1}{\mu_B} + \frac{1}{\mu_{ac}} + \frac{1}{\mu_{SR}} + \frac{1}{\mu_C} \right]^{-1} \qquad (2)$$

where the scattering components are due to bulk, surface acoustic phonons, surface roughness and Coulomb scattering. The bulk mobility is given by the formula [48]:

$$\mu_B = \left[\frac{1}{\mu_L} + \frac{1}{\mu_I} \right]^{-1} \qquad (3)$$

where the two scattering components are due to lattice and impurity scattering. The above formula is developed based on empirical results. In 1972 [49], it has been shown that the fixed oxide charge in weak inversion affects the low-field mobility but not in strong inversion when the charges are screened. Lombardi et al. suggested that the fixed charges can be replaced by interface charges with the MOSFET in inversion and then the mobility is affected by Coulomb scattering [43]. It was shown that Coulomb scattering is dominant near the inverted surface of the device when the interface trap density is high near the surface and at low temperatures [44]. Potbhare et al. [45-47] introduced the temperature effect also and a component of high field mobility in their latest model [47], but they also agreed with the Coulomb scattering being dominant near the interface at high interface state densities of greater than 5 x $10^{11}/cm^2eV$. The dominant mobility due to Coulomb scattering is inversely proportional to the $D_{NIT} + D_{it}$ at a given temperature [46]. Therefore, the surface mobility of the 4H-SiC MOSFET can be determined from the known mobility and trap density of the Si MOSFET and the trap density in the 4H-SiC MOSFET. The calculation is shown below:

$$\frac{\mu_1}{\mu_2} = \frac{D_{it2} + D_{NIT2}}{D_{it1} + D_{NIT1}} \qquad (4)$$

Since the trap density in 4H-SiC MOSFET is $30x10^{11}/cm^2eV$ after NO annealing [36] which is three times more than the trap densities in Si-MOSFET, where it is $10x10^{11}/cm^2eV$ [50], therefore the FE surface mobility is expected to be three times less in 4H-SiC MOSFET. The High K Metal Gate (HKMG) Si-MOSFET having N_2 annealed $HfO_2$with an EOT of 1 nm is recently been shown to have a peak electron mobility of about 140 cm^2/V-s [51]. Therefore, the peak mobility in the 4H-SiC MOSFET is expected to be 140/3, which equals about $46cm^2/V$-s. The observed peak effective mobility of $37cm^2/V$-s and an average effective mobility in our NO annealed collaborative sample is $33cm^2/V$-s [52]. The observed peak field effect (FE) mobility on the 4H-SiC MOSFET in the study of Dhar et al. [53] is 45 cm^2/V-s after NO annealing of the dry oxide grown at 1150 ^oC on 4H-SiC (0001) oriented Si-face surface, which is consistent with the above observation of peak mobility on HKMG Si MOSFET. This vouches for the mobility relation given by equation (4) above. Since the D_{it} + D_{NIT} in the GaN MOS devices are of the same order of low $10^{12}/cm^2eV$, therefore the mobility in the n-channel MOSFET on GaN is also expected to be about $45cm^2/V$-s. Few words about an important parameter of a power MOSFET is mentioned. It is the specific on resistances for the power 4H-SiC MOSFETs. It is of the order of 1-10 milliohms-cm^2 for a 1 KV device and is limited by the resistance of the drift region of the MOSFET [54]. A similar value is obtained for GaN based power MOSFETs also.

A study by Saks and Agarwal [55] has pointed out that for the MOSFETs fabricated on 4H-SiC, the Hall bulk mobility is much larger than the surface effective mobility due to reduced density of free electrons caused by trapping at the interface traps and due to Coulomb scattering. To demonstrate this effect, Δn_{free} and Δn_{total} are compared at room temperature. It is observed that Δn_{free} is about 35% less than Δn_{total} in non-nitrided deposited oxide based 4H-SiC MOSFETs [56] due to trapping of electrons at the interface states. For the nitrided (NO annealed) grown oxide based MOSFETs, the Δn_{free} is only about 10% less than Δn_{total} and about 25% less in nitrided deposited oxide based 4H-SiC n-channel MOSFETs [57]. Also, Arnold et al. [58] have extended the charge sheet model for inversion carriers from Silicon to SiC having incomplete ionisation at 300K. It gives higher carrier densities in inversion at low gate voltages but becomes identical to the

conventional model when the inversion carrier density reaches to low $10^{12}/cm^2$ and greater. The above analysis confirms the trapping of electrons and Coulomb scattering phenomenon in 4H-SiC n-channel MOSFETs fabricated on Si-face of (0001) oriented surfaces.

Table V. Comparison of mobility of n-channel MOSFETs fabricated on 4H-SiC and 2H-GaN on (0001) and(1120) oriented surfaces.

Device Interfaces	D_{it} at E_c-0.2 eV ($x10^{11}/cm^2eV$)	D_{NIT} ($x10^{11}/cm^2eV$)	D_{it} + D_{NIT} D_{it} is throughout the bandgap ($x10^{11}/cm^2eV$)	Comparison of anneals	Surface FE mobility in n-channel MOSFET (cm^2/V-s)	Oxide breakdown field with charges (MV/cm)
As-oxidised on 4H-SiC-Si-face (0001) oriented surface	24	12	24 + 12	poor	5-7	>8
As-oxidised + NO annealing at 1150°C or 1175°C for 2 hrs.	6	24	6 + 24	NO (good)	35-45 35 is effective mobility	≥7.8
4H-SiC-Si-face (1120) oriented surface, NO annealed interface					90-100	Lower, High density of donor states near VB giving more positive charge in p-type device , thus lowering the oxide breakdown to 5MV/cm..
Deposited CVD oxide on 2H-GaN – Ga-face (0001) oriented surface With and without forming gas annealing at 420°C for 20 min.	20	25	20+25	poor	5-25	Lower, expected, (probably more Nitrogen bonded)
Deposited Oxide/Nitride/oxide or Al_2O_3 gate dielectric fabricating vertical MOSFETs having a-face (1120) oriented channels.	One order lower			good	Two device examples with 131 and 185	Lower, expected due to excess Nitrogen containing states

The data in Table V does not need much explanation. NO annealing for the 4H-SiC has proven to be useful in reducing interface trap density and increasing the surface mobility up to $45cm^2/V$-s [52-53]. GaN surfaces have been treated with sulphur, but the interface trap density remains near low $10^{12}/cm^2eV$ order [40-41, 59]. Some research groups have shown low trap density near the CB and higher trap density near the VB along with higher positive fixed charge density of about 8 x $10^{12}/cm^2$ in the p-type device [60]. The GaN MOS device on the a-face has also shown higher mobility of 131 and 185 cm^2/V-s [61-62]. The current discussion is not final but the limited data set analysed informs the author that the GaN is similar to the 4H-SiC with a high density of Nitrogen dangling bonds at about 40 x $10^{11}/cm^2$ and the D_{NIT} is calculated to be in the low $10^{12}/cm^2$ limiting the surface mobility to up to 25-45 cm^2/V-s on the (0001) oriented surface. More research needs to be done in the area of GaN MOS devices to have a clear understanding and trend of trap densities and processing effects to compare favourably or otherwise with the 4H-SiC MOSFETs, particularly for power applications. A technology based article has highlighted the complimentary applications for the power MOSFETs on the two semiconductors. The SiC power MOSFETs are proposed for applications such as Smart grids, railways and HVDC transmission, whereas the GaN power MOSFETs are proposed for applications such as Industry, Power supplies, Consumer electronics, lighting etc. The automobile sector is common to both materials [63].

Table VI. Fixed charge density N_f, and interface trap density D_{it} at E_c-0.2 eV, at different oxide annealing ambient condition on n-SiC-Si-face MOS device.

n-type SiC-MOS device, Oxide Annealing temperature (^oC)	Oxide Annealing ambient % O_2	Oxide Annealing Time (minutes)	Fixed charge density, N_f ($x10^{11}/cm^2$)	Interface trap density at E_c-0.2 eV D_{it} ($x10^{11}/cm^2eV$)
1100	Small parts O_2 in Ar	30	-12(mainly sp^2 C)	24
950	Wet re-ox	3 hrs	-24(adds O)	60
1300	0.001	1	-3(removes sp^2 C)	49
1300	0.1 (like re-ox)	1	-12 (adds O)	49
1500	Pure Ar	1	-24(adds sp^2 C)	62
1500	0.001	1	+12(removes sp^2 C)	24
1500	0.1 (like re-ox)	1	-16 (adds O)	63

Table VII. Fixed charge density N_f, and interface trap density D_{it} at E_c-0.2 eV, at different oxide annealing ambient conditions on n- and p-4H-SiC-Si-face MOS devices in the order of 1MHz C-V curve shifts.

n-type SiC-MOS device, Oxide Annealing temperature (^oC)	Oxide Annealing ambient % O_2	Detected carbon cm^{-3} (cm^{-2} for 2 nm interface)	Oxide Annealing Time (minutes)	Fixed charge density, N_f in p-type MOS device ($x10^{11}/cm^2$)	Fixed charge density, N_f in n-type MOS device ($x10^{11}/cm^2$)	Shift in 1MHz High Frequency C-V curve	Interface trap density at E_c-0.2 eV D_{it} ($x10^{11}/cm^2eV$)
1500	Pure Ar	10^{20} (2 x 10^{13})	1		-24(adds sp^2 C)		62
1300	0.001		1		-3(removes sp^2 C)	left	49
1500	0.001	10^{18} (2 x 10^{11})	1		+12(removes sp^2 C, excess Si)	Further left	24
1100	Small parts O_2 in Ar		30	24	-12(mainly sp^2 C, same D_{it},	Right	24
1300	0.1 (like re-ox)		1		-12 (adds O, increases D_{it})	Same as previous	49
1500	0.1 (like re-ox)		1		-16 (adds O, increases D_{it} further)	Further Right	63
950	Wet re-ox		3 hrs	12	-24(adds O, increases D_{it} further	Further right	72

The data presented in Table VI and VII are analysed next. In Table VI it is shown that 1 minute anneal at the same temperature of 1300^{o}C or 1500^{o}C but having larger partial pressure of oxygen (at 0.1%) acts like a re-oxidation process giving higher negative N_f in the n-type MOS device. Higher negative N_f represents higher density of near interface traps or D_{NIT}. Higher temperature of 1500^{o}C also gives higher interface trap density D_{it}, implying higher concentration of carbon at the interface. The N_f and D_{it} data of Table VI which is obtained from the study of Kobayashi et al. [3] is rearranged in Table VII along with the N_f and D_{it} data from the study of Chung et al. [17] in the order of left and right shifts of the 1MHz high frequency C-V curves that represents removal of carbon and addition of oxygen at the SiC/SiO_2 interface. D_{it} is 8 x $10^{11}/cm^2$ eV at E_v + 0.2 eV as shown in Fig.2 of Williams [4]. Si-C-O-O E' centres in wet re-oxidised SiC MOS sample have one unpaired electron on the Si atom in each one of them. If 1N replaces 1O, then a positive charge is added and an E' centre becomes neutral. The N_f after NO annealing in n-MOS device therefore becomes zero whereas the positive charge doubles. Carbon is reduced to 2 x $10^{11}/cm^2$ at the interface with 0.001% O_2 ambient at 1500^{o}C for 1 min as presented in Table VII. Since Carbon has 4 valence electrons, each one can contribute to the interface state charge. Therefore, carbon states at the VB edge become 4 x 2 x $10^{11}/cm^2$ eV which equals 8 x $10^{11}/cm^2eV$ as can be seen in Fig.2 of Williams et al. [4]. Similarly, Si-C-O-O correlated bonds have (4+4+2+2) bonded valence electrons equalling 12. Each of them can contribute to the interface state giving D_{it} of 12 x 2 x $10^{11}/cm^2eV$. This equals D_{it} of 24 x $10^{11}/cm^2eV$ near the CB edge at E_c-0.2 eV. This is the minimum D_{it} achievable. After wet re-oxidation at 950^{o}C for 3 hrs, the D_{it} is 72 x $10^{11}/cm^2eV$. This means that the carbon content has gone up to 72/12 equals 6 x $10^{11}/cm^2$at the SiC/SiO_2 interface. This also means that the volume density at the interface is now 3 x $10^{18}/cm^3$ for a 2 nm interface. It can be concluded that low temperature re-oxidation for a long time of 3hrs tends to increase the carbon density at the interface. The charges in the MOS devices fabricated on n- and p-type (111) oriented Si surface are usually positive and therefore only positive charges obtained on the 4H-SiC MOS devices fabricated on the n- and p- (0001) oriented surfaces are correlated with those in the MOS devices fabricated on Si (111) surfaces. Also, the border traps in Si/SiO_2 and 4H-

SiC/SiO_2system are correlated. The negative N_f due to the acceptor traps in the n-type MOS device implies more carbon at the interface even if it is occurring with the addition of oxygen. This can be observed in Table VII, where the higher D_{it} at E_c-0.2 eV is related to higher negative N_f values in the n-MOS devices indicating higher carbon content at the interface as explained earlier.

Observing data in Table VII informs the author that if D_{it} and D_{NIT} is low near the CB without NO annealing as determined from the n-type MOS device, then the fixed charges N_f in the p-type MOS device is higher due to higher density of donor states and therefore leakage current and oxide breakdown is lowered for the n-channel MOSFET due to increase in the cathode field for electron tunnelling [31]. The switching states are converted to fixed states. If the N_f in the p- and n-type devices is observed then it can be concluded that the difference in N_f is the same at 36 x $10^{11}/cm^2$. N_f after oxidation at 1100^{o}C followed by inert Ar anneal for 30 min is 24x$10^{11}/cm^2$ in the p-type device and -12 x $10^{11}/cm^2$ in the n-type device. This study by Chung et al. [17] shows that after wet re-oxidation at 950^{o}C for 3 hrs, N_f in the p-type device reduces to 12x$10^{11}/cm^2$, but N_f in the n-type device increases to -24x$10^{11}/cm^2$, keeping the same difference in N_f at 36x$10^{11}/cm^2$. It has also been observed that reducing D_{NIT} with high temperature oxidation increases D_{it} at E_c-0.2 eV, and D_{NIT} is doubled after NO annealing in the n-type device along with fixed states in the p-type device [36]. It can be inferred from the above observations and analysis that N_f in the p-type MOS device annealed at 1300^{o}C in 0.001% O_2 as shown in the Table VII will be about 33x$10^{11}/cm^2$ which will increase the low-field leakage current and high-field tunnelling current and thus lower the breakdown field in the oxide [31]. After NO annealing this N_f will double to 66x$10^{11}/cm^2$ in the p-type device increasing the leakage current and lowering the oxide breakdown field further. Observing the 1500^{o}C annealing temperature having 0.1% O_2 in the ambient as shown in Table VII, N_f in the p-type MOS device would be 20x$10^{11}/cm^2$ which after NO annealing would double and lower surface mobility and oxide breakdown field in the n-channel MOSFET. N inclusion at the interface is desirable to reduce D_{it} to much lower levels from the pre-NO annealed state for improving surface effective and field effect (FE) mobility. It seems that wet re-oxidation needs to be done to reduce D_{NIT} to 12 x $10^{11}/cm^2$ before NO annealing and to keep the density of positive charges in the p-type MOS device to 12 x $10^{11}/cm^2$. This will increase to 24x $10^{11}/cm^2$ after NO annealing. Since the charges have been shown to correlate to the Si/SiO_2 system, not much can be done further to increase mobility of n-channel 4H-SiC MOSFET fabricated on Si-face of (0001) oriented surface without sacrificing oxide breakdown field [31]. The window of ΔN_f in p-type and n-type MOS device of 36x$10^{11}/cm^2$ before NO annealing informs the author that not much can be done to reduce this window. If the window is more to the left then the fixed states in the p-type device is higher which increases the leakage current and lowers the oxide breakdown field as explained earlier that the switching states are converting to fixed states [31, 36]. If the window is more to the right, the D_{NIT} and D_{it} becomes higher that will reduce the surface mobility in the MOSFET, although the fixed charges due to D_{NIT} in the n-type device will neutralise by inclusion of N while D_{it} is reduced by one order throughout the bandgap [4, 17, 64]. It can also be inferred that one-third of the window represents the density of E' centres near the SiO_2/Si(111) at 12 x $10^{11}/cm^2$ due to the absence of carbon and indicates better interface abruptness [65]. This density closely matches the density of E' centres reported in Fig. 16 of a 1998 review article that promotes MOS/EPR studies [66]. Oxidised Si (111) has donor states in the upper half of the Si band gap also [26]. They therefore show up as positive charge in p-type MOS device and are neutral in n-type MOS device. One data set in Deal's 1967 study shown in Table III (A) of his reference [6], shows N_f of 10 x $10^{11}/cm^2$ when p-Si (111) is annealed at 550^{o}C in O_2 ambient for 90 minutes. Thermal silicon dioxide on p-Si (100) having an 8.5 nm thickness, has also shown D_{NIT} of the order of 12 x$10^{11}/cm^2$eV with p-Si in inversion [30]. Now, if N_f in thin oxide on Si of 1 to 10 nm is 12x$10^{11}/cm^2$ [50, 67], then they could be coming from NITs in the p-type device on Si as donor states in the form of fixed positive charge. Long-time low temperature re-oxidation results in 'rechargeable' E' centres of the order of low $10^{12}/cm^2$.along with electrically inactive excess Si. Oxidised 4H-SiC Si-face-(0001) has acceptor states in the upper half of the band gap [17, 36]. They therefore show up as negative charges in n-type MOS device. They are neutral when empty in p-type MOS device. N_2O oxidised 4H-SiC MOS device on (1120) oriented surface shows a high density of donor states near the VB as shown in Fig. 3 of the reference of Noborio et al. [68] as compared to the density on (0001) or (0338) oriented surfaces. These high donor states appear as positive fixed charges in the p-type MOS device. They enhance the cathode field for electron tunnelling in the inverted p-type MOS device as an n-channel MOSFET giving lower oxide breakdown field reported as 5 MV/cm [36]. Forming gas annealing of a MOS device can cause the ΔN_f window to become smaller as observed in the study by Yano et al. [28]. This behaviour is elaborated in the author's previous article [2]. The effect of hydrogen passivation and activation of oxygen complexes in a MOS device which are electrically active and inactive has been studied by other research groups also, showing that the effect involves low binding energy of hydrogen of less than 1 eV [69]. This study corroborates the analysis by the author of the reduced ΔN_f window in 4H-SiC MOS devices.

IV. Conclusion

The calculated D_{NIT} on the GaN MOS devices utilising a novel method of observing the low-field leakage current in a MOS device in accumulation, is comparable to those on 4H-SiC MOS devices at 26 x $10^{11}/cm^2eV$. The dominant Coulomb scattering in the n-channel MOSFETs causes surface mobility in MOSFETs to be inversely proportional to the total density of traps at or near the surface and at room temperature, giving field effect surface electron mobility on 4H-SiC and GaN MOSFETs of about 45 cm^2/V-s with nitrided oxides on SiC. The electron trapping at the interface is minimum in nitrided gate oxides on 4H-SiC because of the passivation of interface traps with nitrogen. The oxides formed on the c-face of 4H-SiC having (0001) surface orientation and (1120) surface orientation have a lower breakdown field due to higher fixed charge densities. The planar density of atoms in 2H-GaN and 4H-SiCT (0001) oriented surface is almost same as that on Si (111) surface and therefore close to 70% of the bandgap forms the lower half of the bandgap having donor states. Therefore, the charge densities on these surfaces can be compared. The positive charge density due to excess Si in the wet oxidised/wet re-oxidised/Ar annealed n-type and p-type 4H-SiC MOS device on (0001) oriented Si surface is completely correlated to the positive charge density due to excess Si in the wet oxidised Si MOS device on (111) oriented surface. The density of positive charges in the 4H-SiC MOS device of 12 x $10^{11}/cm^2$ is three times the density of positive charge in the Si-MOS device which is 4 x $10^{11}/cm^2$. The addition of carbon in the Si-C-O bonded excess Si has two less electrons so as to bring about a three times change in the positive charge density. Similarly, the border trap density in the Si MOS device is correlated to the D_{NIT} in the 4H-SiC MOS device. The lower bound on the border trap density in Si MOS devices is ~3 x $10^{11}/cm^2eV$ that contributes to the electrical response in the MOS devices. This density is about three times less than D_{NIT} in the 4H-SiC MOS device at 12 x $10^{11}/cm^2eV$. A ΔN_f window of 36 x $10^{11}/cm^2$ is observed between the p-type and n-type 4H-SiC MOS device. A left shift of this window through high temperature processing will increase the fixed positive charge density in the p-type MOS device coming from deep traps. It will further increase after the desirable NO annealing. This will result in higher leakage current and lower oxide breakdown field. The switching states convert to fixed states. A right shift of the window causes the D_{NIT} to increase, that lowers the surface mobility in the n-channel 4H-SiC MOSFET. Higher interface trap density represent higher carbon content at the SiC/SiO_2 interface. The high temperature annealing of the oxides in the MOS devices at 1300^oC or 1500^oC in higher low partial pressure of O_2 acts like a re-oxidation anneal which adds oxygen and forms negative acceptor states on n-type MOS devices.

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