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Design and simulation of low Readout Noise and wide Dynamic Range CMOS Image sensor using Diode Connected Load Technique

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Abstract:*This paper presents the design and implementation of a low readout noise and wide dynamic range CMOS image sensor (CIS) with high sensitivity based on diode connected load technique. The sensor is simulated, designed and implemented in a 130 nm CMOS technology. The proposed pixel area reaches to 3 µm x 3 µm and consists of six NMOS transistors with one capacitor. The parameters of readout circuit features very low output noise of 19 μV_{rms} with a 4 MHz bandwidth for pixel circuitry. Power dissipation of 11.2 µW was achieved at low voltage operation of 1.6 V for pixel circuitry. The sensor has a combination of low noise and a 97 dB wide dynamic range due to the diode connected load configuration.*

Background*: CMOS image sensorisconsidered the main part in digital cameras, and withoutit the camera can not beoperateproperly. So, the development of CMOS sensorparametersistakinggreatattension. The dynamic range of CMOS image sensoris one of the most important parameter of image sensor, so if the dynamic range has been extended, then the sensorbe able to detect all the image parts. Also, the readout noise of CMOS image sensorisconsidered an important parameterwhich must bereduced to improve the quality of image sensor. In thisstudy the diode connectedload technique isused to improvedynamic range also to reducereadout noise of CMOS image sensor.*

Materials and Methods*: In this study, two CMOS image sensor circuitries are simulated, one of them is the traditional CMOS image sensor which is the circuit we start from and the other circuit is the proposed wide dynamic range CMOS image sensor. The traditional pixel circuitry provides a method to extend the dynamic range of CMOS image sensor by using a lateral overflow integration capacitance, but this method has a drawback in reducing the bandwidth of CMOS image sensor, so we provide the proposed wide dynamic range CMOS image sensor. In the proposed CMOS image sensor we can remove the lateral overflow integration capacitance which reduces the bandwidth and a diode connected load technique is used. We simulated the two circuitries and compared between them to illustrate the advantages of using diode connected load technique.*

Results*: The readout noise analysis for the two circuitries is provided. The linearity analysis of the traditional and the proposed circuitries are simulated. The layout of the proposed pixel circuitry is provides. The simulated results comparison between traditional and proposed circuitry are provided.*

Conclusion:*The diode connected load technique which used with proposed pixel circuitry improves a lot in extending the dynamic range and reducing readout noise of CMOS image sensor also, it extend the bandwidth of CMOS image sensor.*

Key Word*: CMOS image sensor (CIS); Wide dynamic range (WDR); Diode connected load; Readout noise.*

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I. Introduction

Image sensor is considered the main part of a digital camera, which converts optical information of the light photons into electrical signals. Nowadays, CMOS based imaging arrays have a great growing stage. Besides the low cost and low power consumption advantages, the continued growth of CMOS image sensor popularity goes to other factors such as the ability to integrate the sensors with electronics and the ability to achieve fast, customizable frame rates[1].In all image sensors the low noise and high dynamic range are considered two important parameters determine the sensor performance[2].

Nowadays, the development of CMOS image sensor technology is requiring a lot of efforts to be done to get CMOS image sensor with parameters suitable with the existence requirements for imaging technology.CMOS image sensors (CIS) can be divided into voltage mode and current mode, categorized by readout circuit types. In a voltage mode CIS, after the electrons are converted from the charge domain into the voltage domain, they are stored on the floating diffusion region (FD) and are read out through a source follower

(SF)[3]. In current mode CIS, the readout transistor is biased in the linear region or the velocity saturation region to generate a current instead of a voltage. This CIS is suited for high-speed readout and focal-plane processing. However, poorer noise performance and higher nonlinearity have prevented it from being widely used[4]. Dynamic range of CMOS image sensor is considered one of the most important parameters of the sensor which must be improved to increase the sensor quality in capturing the image details[5,6,7]. In this decade, increasing of the dynamic range of CMOS image sensor became the main target even though there are initial methods were already proposed in most commercial sensors in which the dynamic range of sensor is limited to 72 dB[8]. There are more common implementation using multiple exposures which achieved a high dynamic range of 112 dB[9]. Reference[10] is focused on the reduction of the input referred noise as the temporal read-out noise is reduced below 0.5 electron to increase the dynamic range. The CIS in[11] reduced readout noise to less than 0.7 e− rms, this method achieved 40% reduction in the input–referred temporal noise. This paper focuses on increasing the dynamic range of voltage-mode CMOS image sensor and reducing its noise by introducing a new CIS technique based on diode connected load and get CIS with high speed.

II. Overview of CMOS Image Sensor

A functional block diagram of a typical CIS system is shown in Figure 1. The sensor structure consists of a pixel this one pixel can be extended to an array of pixels. The output of the pixel is amplified by the programmable gain amplifier (PGA) which acts as a variable gain amplifier. The amplification will controlled by the values of the capacitor array connected between the input and output nodes of the amplifier. The sample and hold circuit (S&H) is used as correlated double sampling circuit (CDS) to reduce the sensor noise. The CDS output is then digitized by using analog to digital converter (ADC).

As shown in Figure 2. The pixel utilizes photodiodes (PD) to convert photons of an optical signal into a photocurrent in the electrical signal. After the lightfalls on the photodiode (PD), the charges will be accumulated and (electron/ hole) pairs will be generated. These charges will be converted into voltage through the floating diffusion capacitance (C_{FD}). Then the produced voltage signal is transferred to the output through a source follower amplifier (SF). As a result, the total image system converts the input light into voltage signal which is converted into digital signal at the output of the sensor. This process produces an output signal in linearity with the input signal.

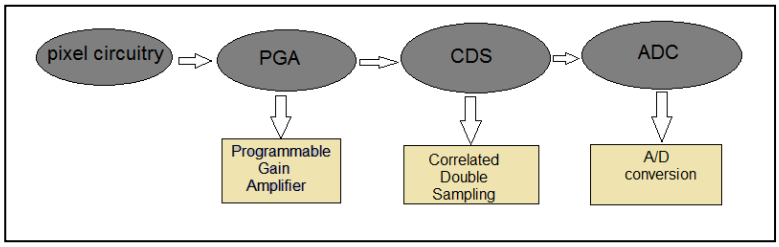

Fig. 1: Block diagram of CMOS image sensor

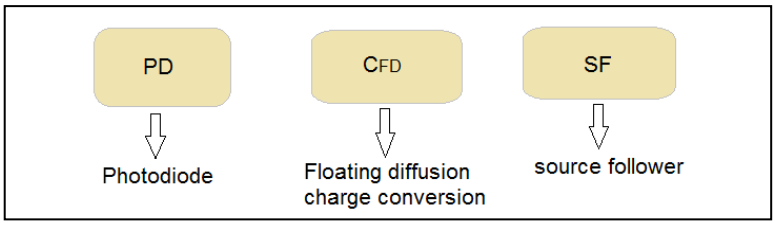

Fig. 2: Pixel circuitry structure

III. Circuitry of The proposed CIS

In this section the traditional wide dynamic range and proposed wide dynamic range CIS will be discussed in details and a comparison between these configurations will be presented. The advantage of the proposed diode connected load technique will be discussed with results.

Circuitry of the traditional WDR CIS using Lateral Overflow Integration Capacitance

The traditional voltage mode image sensor circuit diagram[12,13]is shown in Figure 3. The pixel circuit contains a photodiode, switch (M1) for charge transfer from PD to be stored in C_{FD}. The voltage on C_{FD} will be transferred to the output node via source follower input transistor (M4), (M5) switch for row selection and (M6) is the biasing transistor which can be shared by multiple rows of pixels, for the reset operation, there are reset1

switch (M2) and reset 2 switch (M3). A lateral overflow capacitor (C_v) is used to improve the dynamic range[12,13].

The sequence of operation is as follow. Initially the photodiode (PD) is empty from any charges. The reset 2 switch (M3) and the row select switch (M5) are ON, and at the same time the remaining transfer switch (M1) and the reset 1 switch (M2) are OFF. The reset 1 switch (M2) is then ON to enable resetting the floating diffusion capacitance (C_{FD}) and for resetting (Cv). After turning the switch (M3) OFF, the transfer gate switch (M1) is turned ON, then for getting the voltage on (C_{FD}) another read is occurring. After transferring the generated charges in the photodiode to the floating diffusion capacitance (C_{FD}), the signal will be read by SF (M4, M5, M6). So the total signal will be read out after turning the reset 2 switch (M3) ON. The dynamic range of this technique will increase by increasing the area of the overflow capacitor (Cv) to get a large one. This will reduce the sensor bandwidth so the dynamic range will increase. The drawback of this CIS is the reduction in the bandwidth of the sensor, this reduction in the bandwidth will decrease the camera speed and the maximum frame rate. Also the complexity in designing of the driver control signals circuits is increased.
In the next section we will introduce our proposed WDR CIS, which solve the bandwidth problem required for high frame rate applications.

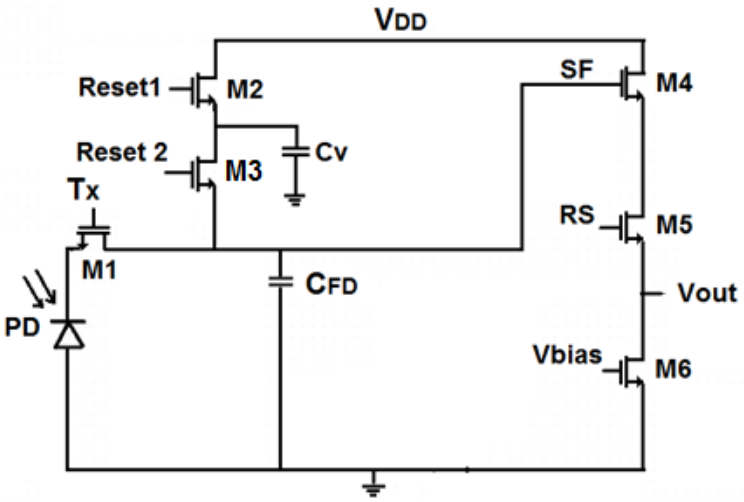

Fig. 3: Circuitry diagram of the traditional WDR CIS[12,13]

Circuitry diagram of the proposed WDR CIS using Diode connected load

The proposed voltage mode WDR image sensor is shown in Figure 4. To determine the effect of the additional diode connected transistor (M7) on the dynamic range, the output noise and the linearity of the image sensor. That the additional transistor (M7), which is a diode connected transistor, improves the dynamic range by introducing second current pass and by reducing the readout noise. As M7 gate and drain are short, and the following saturation condition always holds: VDS > VGS - VT (the transistor operating in saturation)
In saturation for diode mode ($V_{DS} = V_{GS}$) so:

$$I_{DS} = \mu C_{OX} (W/2L)(V_{DS} - V_{TH})^2 \quad (1)$$

The equivalent resistance of this device is:

$$R = V_{DS}/I_{DS} = 2L/W\ (1/\mu C_{OX})\ V_{DS}/(V_{DS} - V_{TH})^2 \quad (2)$$

Therefore, the equivalent resistance will be changed by changing output voltage ($V_{DS} = V_{out}$). As the photodiode current I_{ph} increases and so the voltages on C_{FD} will be increased. Then M4 tries to increase its I_{DS} but it is constant because of the M6 is a constant current source. If M7 is not connected, there will be a large increase in the $V_{DS,M6}$ (V_{out}) to keep $V_{GS,M4}$ constant and so its $I_{DS,M4}$. If M7 is connected, M7 introduces a second path for the currents, so $I_{DS,M4}$ can increase when reducing C_{FD} which results in a smaller increase in $V_{DS,M6}$ (V_{out}). This effect will increase the maximum output voltage linear range at high input photocurrent I_{ph}. The maximum output noise occurs if the transistor sees only its own output impedance as the load. So the noise current of the MOS transistor decreases if the transconductance drops. As M7 is connected in parallel with the current source M6, so a smaller current and smaller g_{m6} can be used, and this will decrease M6 noise and the total output noise of the CIS. By using M7 $I_{Ds,M4}$ can be larger as it equal to $I_{DS,M6}+I_{Ds,M7}$ and higher transconductance of source follower $g_{m,M4}$ is achieved. The source follower noise decreases by increasing its g_m. so the total output noise of the circuit will be decreased.

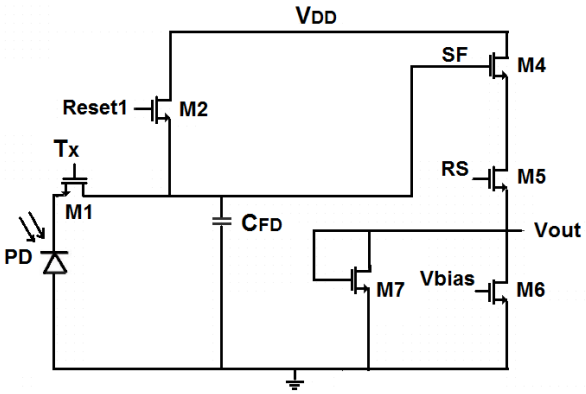

Fig. 4: Circuitry of the proposed WDR CIS with Diode Connected Load

IV. Result

We made a comparison between the traditional and the proposed WDR CIS in their results, such as maximum input photocurrent, maximum output voltage, bandwidth, output noise, dynamic range and linearity to show the effect of adding diode connected load transistor. This comparison is shown in Table no 1. As expected the proposed WDR CIS has a bandwidth of (4 MHz) which is higher than the traditional WDR CIS using a lateral overflow integration capacitor, because of the elimination of the overflow capacitor C_v. A higher dynamic range of 97 dB is also achieved because of the diode connected M_7 effect.

Table no 1. Comparison between the proposed WDR CIS with and without diode connected load M7 and the traditional CIS.

Parameter	Traditional WDR CIS	WDR CIS without M7	Proposed WDR CIS
Maximum input photocurrent (I_{ph})	10 µA	11 µA	20 µA
Output noise	94.5 μV_{rms}	92 μV_{rms}	19 μV_{rms}
Maximum output voltage	1.5 V	1.4 V	1.4 V
Bandwidth	43 KHz	45 KHz	4 MHz
Dynamic range	83.7 dB	83.6 dB	97 dB
Non Linearity	2.2 %	1.8 %	1 %

Noise Modeling of the proposed WDR CIS

Noise reduction for the proposed CIS can be proved mathematically as following. Firstly, we will prove the total output noise of the circuit before adding the diode connected transistor M7 as in Figure 5 and Figure 6 by using the small signal model of the circuit as follow:

from Figure 6. We can calculate the components of the output noise, the first component of the noise ($V_{n,out1}$) is due to transistors (M4& M6)

$$V_{n,out1}(1-g_{m4}Z_{out})=(I_{n,M4}+I_{n,M6})Z_{out} \quad (3)$$

$$Z_{out}= r_{ds4}//r_{ds6}//X_{CL} \quad (4)$$

The second component of the noise ($V_{n,out2}$) is due to R_x

$$V_{gs4}= V_{g4}-V_{s4}= I_{n,Rx}X_{CFD}-V_{n,out2} \quad (5)$$

$$V_{n,out2}=g_{m4}V_{gs4}Z_{out} = g_{m4}Z_{out}(I_{n,RX}X_{CFD}-V_{n,out2}) \quad (6)$$

$$V_{n,out2}(1+g_{m4}Z_{out}) = g_{m4}Z_{out}I_{n,Rx}X_{CFD} \quad (7)$$

As $g_{m4}\, Z_{out}<1$ for the SF, so from the two components of the noise the total output noise can be reduced by reducing the output resistance Z_{out}. Therefore, if we will be able to reduce the output resistance we can reduce the total output noise of the circuit. This can be done by adding the diode connected transistor (M7) to the circuit as in Figure 7 and Figure 8. We replaced the diode connected model with an output resistance = $r_{ds7} = 1/g_{m7}$ and it is very small resistance so as will be discussed later the total output resistance of the circuit will be reduced and the total output noise will be decreased.

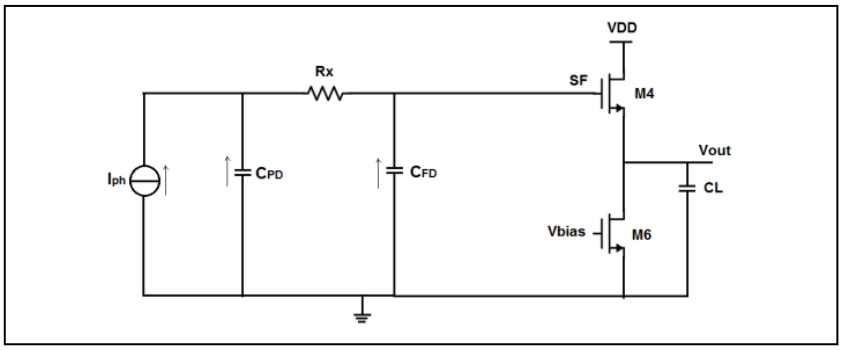

Fig. 5: Equivalent circuit for Noise analysis

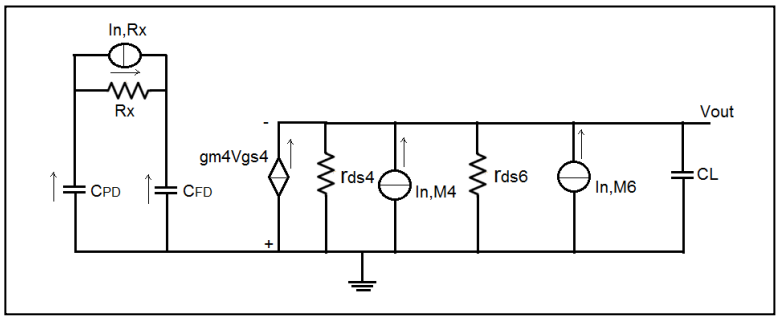

Fig. 6: small signal noise equivalent circuit

Now we calculate the output noise after adding the diode connected transistor (M7) as in Figure 8. The first component of the noise ($V_{n,out1}$) is due to transistors (M4, M6 and M7)

$$V_{n,out1}=(I_{n,M4}+I_{n,M6}+I_{n,M7}+g_{m4}v_{n,out1})Z_{out} \quad (8)$$

$Z_{out} = r_{ds4} // r_{ds6} // r_{ds7} // X_{CL}$ so it is very small resistance because of r_{ds7} of the diode connected transistor is very small

$$V_{n,out1}(1-g_{m4}Z_{out}) = (I_{n,M4}+I_{n,M6}+I_{n,M7})Z_{out} \quad (9)$$

The second component of the noise ($V_{n,out2}$)is due to R_X

$$V_{n,out2}(1+g_{m4}Z_{out}) = g_{m4}Z_{out}I_{n,Rx}X_{CFD} \quad (10)$$

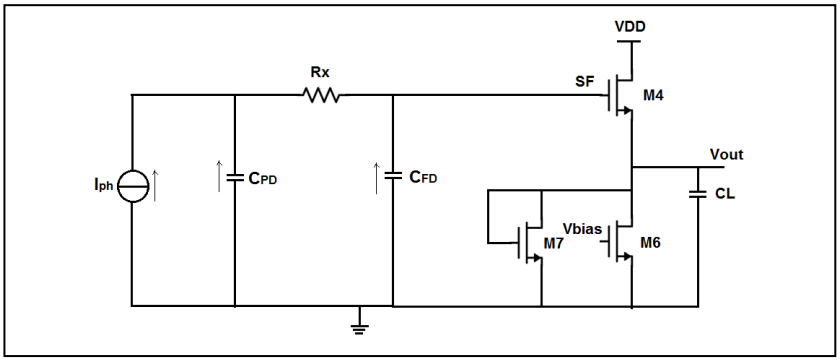

Fig. 7: Equivalent circuit for noise analysis of proposed WDR CIS

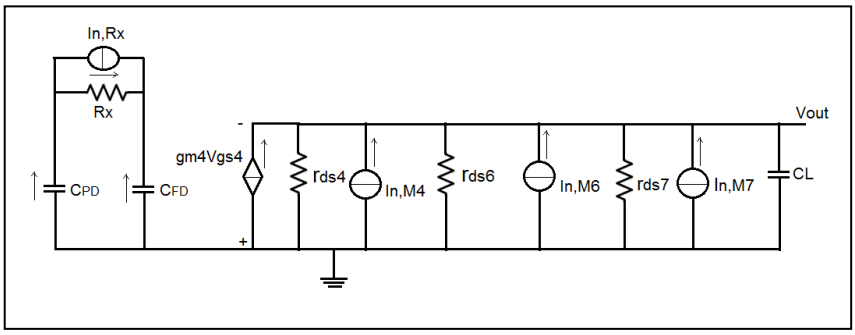

Fig. 8: small signal model and noise equivalent circuit for proposed WDR CIS

In addition, to ensure that our noise model is accurate, we made a comparison between the proposed CIS simulated output noise results using Cadence and the Matlab results of the developed mathematical noise model. As is clear from Table no 2 that both results are nearly equal to each other, this proves that our noise model is valid. Figure 9and Figure 10 prove the validation of the proposed noise model by plotting the output noise power spectral density results obtained by circuit simulation using Cadence and Matlab calculations in the developed noise model.

Table no 2. Comparison between the output noise values by using Cadence and the developed mathematical model using Matlab.

Traditional WDR CIS	In Cadence = 94.5μV_{rms}	In Matlab = 95μV_{rms}
Proposed WDR CIS	In Cadence = 19 μV_{rms}	In Matlab = 20 μV_{rms}

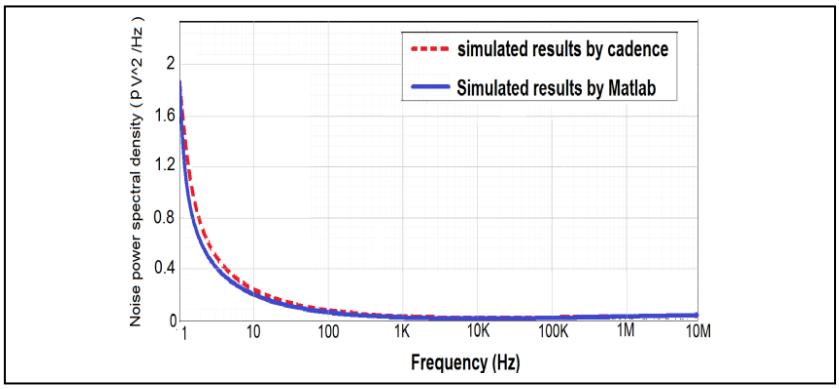

Fig. 9: The simulated output noise power spectral density of the image sensor by Cadence compared with calculated noise model results by Matlab for proposed WDR CIS

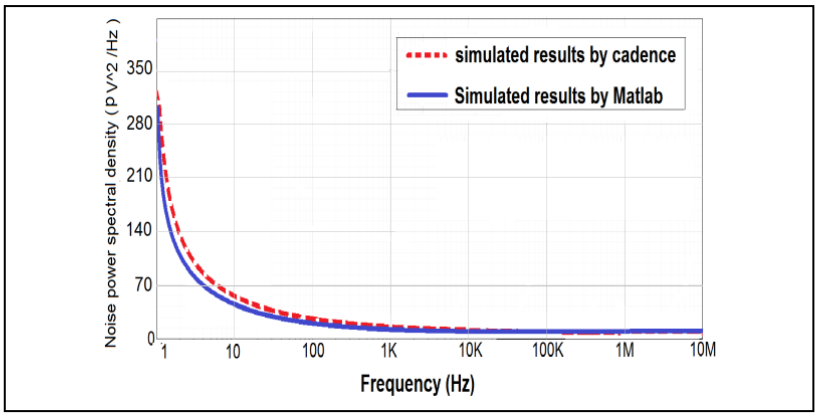

Fig. 10: The simulated output noise power spectral density of the image sensor by Cadence compared with calculated noise model results by Matlab for the traditional CIS

Figure 9and figure 10 show the plotted results of the mathematical noise power model by Matlab and simulated results for the proposed pixel output noise power using Cadence. It is clear from the plotted results that they are nearly equal to each other. The proposed CIS output noise power shown in Figure 9 is smaller than the CIS output noise power for traditional CIS shown in Figure 10.

Figure 11 shows the timing diagram of the CMOS image sensor readout. Figure 11shows the input and the output signals shapes on transfer gate switch (M1), Reset1 switch (M2), Row select switch (M5), and the pixel output. During readout the photodiode accumulates the photogenerated electrons. The transfer gate switch (M1) will transfer these charges from the photodiode to the floating diffusion (FD). During readout the Row select switch (M5) is always on, and the Reset1 switch (M2) is turned on to empties the floating diffusion (FD) from electrons. After the accumulation of the photoelectrons in the photodiode, the transfer gate switch (M1) is turned ON to transfer the cumulative photoelectron to the capacitor (C_{FD}). Then the source follower (SF) will sense the voltage on (C_{FD}) so the reading out of the signal is performed.

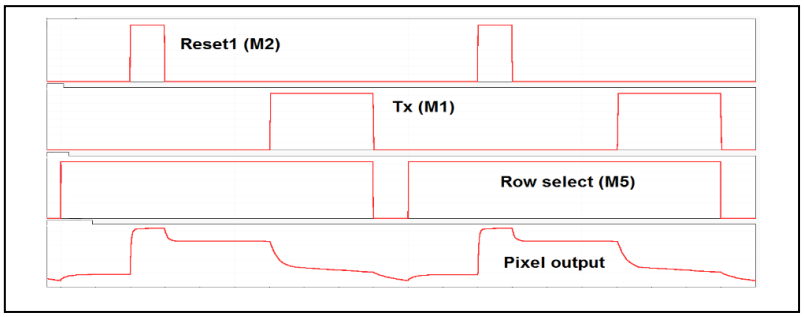

Fig. 11: The simulated transient waveforms of (transfer, reset, row select and pixel output) at input current of 100 Na

Figure 12 shows how the sensor nonlinearity can be measured. The calculation of the nonlinearity begins with the plot of the output signal level versus the input photocurrent. The signal level is typically represented as analog voltage in order to have a clearer view of the output swing as plotted in Figure 9. The nonlinearity value is usually expressed in percentage, based on the swerve of the output signal from an ideal straight line, based on the measurement results, there will be some restrictions that must be taken into account during the analysis of the proposed CMOS image sensor to reduce the nonlinearity of the sensor such as the sizing of the source follower transistor and the floating diffusion capacitance, which must be kept as small as possible to get a high linearity. From the plotted results it is clear that the linearity of the image sensor is ensured for input photocurrents up to 20 µA, since the pixel nonlinearity reaches to 1%.

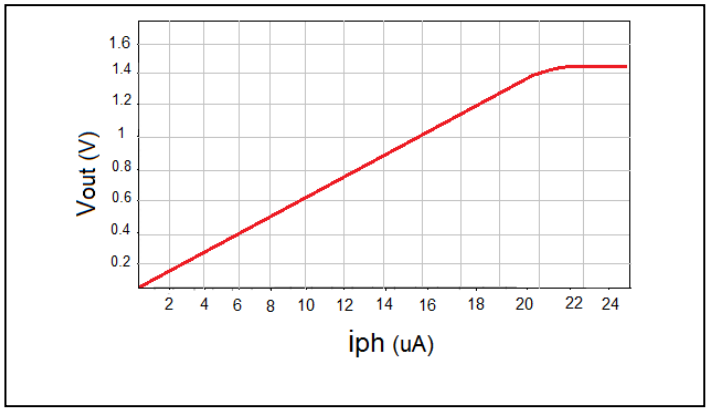

Fig. 12: Simulated results of the input photo current with the image sensor output voltage

Figure 13 shows a typical layout of the proposed image sensor. The sensor was designed and implemented in a 130 nm CMOS technology: the pixel occupies area of 3 µm x 3 µm containing six NMOS transistors with onecapacitor. For getting a good fill factor for the sensor, the distance between the n-well, the neighboring NMOS and the capacitors must be as small as possible, also the layout keeps all the rules required for the technology.

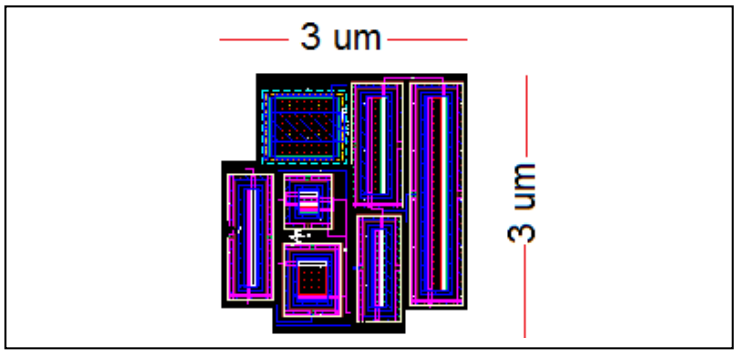

Fig. 13: Proposed Pixel Layout

Table no 3 summarizes all the simulated results for the proposed CMOS image sensor. From these results it is clear that the dynamic range is enhanced to 97 dB. This WDR is achieved by reducing the noise of the image sensor which reached to 19 μV_{rms}, in addition to extending the maximum input current range up to 20 µA. Also the bandwidth extends to 4 MHz, which helps to increase the CIS frame rate. The pixel is consuming 11.2 µW using 1.6 V single power supply which is considered as low voltage operation compared with CIS state of the art.

Table no 3. Summary of The post Layout Simulation Results Obtained From The analysis of the proposed CMOS Image Sensor

Parameter	Results
Technology	130 nm CMOS technology
Power supply	1.6 V
Maximum input current (I_{ph})	20 µA
Maximum output voltage	1.4 V
Conversion gain	32 µV/electron
Output noise	0.6 e-rms (19 µVrms)
Bandwidth	4 MHz
Dynamic range	97 dB
Dissipated power	11.2 µW
Non Linearity	1 %

Table no 4 compares the proposed CIS performance with the state of the art of recently published CIS. It is clear from this comparison that the proposed noise results are reduced a lot compared with the others work. Also, the supply voltage operation (1.6 V) is considered a small supply compared with the others work. The dynamic range was extended to 97 dB. The pixel area which is considered small and suitable area for high fill factor CIS. The only drawback in our work is the slightly bandwidth reduction of CIS, but our value is still considered a suitable value for CMOS image sensor (CIS).

Table no 4. Comparison of the proposed CMOS image sensor (CIS) with the recently published CIS

	[10]	[14]	[15]	[16]	[17]	This Work
Technology	180 nm	0.35 µm	0.14 µm	BSI	65 nm	130 nm
Supply Voltage	3.3 V	5 V	2.7/1.8 V	----	1.2V/2.5V	1.6 V
Bandwidth	300 KHz	12 MHz	72 MHz	----	----	4 MHz
Readout noise	0.48e-rms	270µVrms	1.3 e-rms	1.1e-rms	6.2 e-rms	0.6 e-rms (19 µVrms)
Dynamic range	82.5 dB	74 dB	----	90 dB	121 dB	97 dB
Pixel area (µm²)	6.5x6.5	10.5x 10.5	1.65x1.65	3 x 3	3 x 3	3 x 3

V. Discussion

Based on the obtained results, the effect of adding diode connected load technique improves a lot in the dynamic range and readout noise of CMOS image sensor. As shown in the traditional WDR CIS the use of overflow integration capacitance reduces the bandwidth of sensor and so its speed is reduced, by using diode connected load the readout noise reduced to 19 uV_{rms} compared with traditional CIS which reached to 94 uV_{rms} also, bandwidth in proposed circuitry is extended to 4 MHz compared to traditional in which reached to 43 KHz. As this reduction in readout noise in the proposed CIS the dynamic range is extended to 97 dB compared to traditional in which reached to 83 dB.

VI. Conclusion

This paper provided a new technique which uses a diode connected load transistor in parallel with CMOS image sensor output to reduce readout noise and increases dynamic range of CMOS image sensor.

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