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Distinctly lower border trap density in ultra-dry oxide grown on Si-face of 4H-SiC epi-surface compared to wet re-oxidized oxide projecting higher surface field-effect mobility in MOSFETs

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Abstract: *This article demonstrates, through calculations, a six times lower border trap density in the MOS device having grown oxide in the ultra-dry oxidizing ambient containing less than 1 part per million of water. The BT density comes down from 24 x 10^{11}/cm^2eV for the wet re-oxidized oxide to about 4 x 10^{11}/cm^2eV for the ultra-dry oxide. A significantly higher surface field-effect mobility of over 60 cm^2/V-s is projected because of the ultra-dry oxidation of the Si-face of 4H-SiC (0001) oriented epi-surface. The presence of moisture in the oxidizing ambient promotes formation of higher BT density by forming near-interfacial oxygen vacancy defects.*
Keywords: *Border traps, Metal-Oxide-Semiconductor, Mobility, Oxidation, Silicon Carbide.*

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I. Introduction

Silicon Carbide is the semiconductor material of choice for high power, high temperature and high frequency electronic devices with the power MOSFET in focus in this article. Attempts to increase the surface field-effect (FE) mobility in the power MOSFET is underway, when different processing and annealing techniques are being employed to achieve a passivated SiO_2/SiC interface and get higher surface FE mobility in the n-channel enhancement-mode MOSFET device. Reduction of the interface trap density is thus the goal. It is shown in this article that an ultra-dry oxide has markedly lower border trap density as compared to wet re-oxidized oxide. The author has devised a new method in the recent past (2019-2021) of determining the border trap (BT) or near-interface trap (NIT) density in metal-insulator-semiconductor (MIS) devices [1-6]. This method is based on the displacement current obtained at low electric fields up to the Fowler-Nordheim (FN) onset field with the n-type MOS device in accumulation. The method is used to determine the BT density in wet re-oxidized thermal oxide grown on Si-face of n-type 4H-SiC (0001) oriented epi-surface of the MOS device to be 24 x 10^{11}/cm^2eV [1-6]. This is reviewed in the brief research-cum-review article published by the author recently in June 2021 [7].

In the present article, the above method is used to determine the BT density in the ultra-dry oxide grown on the Si-face of n-type 4H-SiC epi-surface of the MOS device and the value is compared to the BT density in the wet re-oxidized oxide, wet re-oxidized at 950ºC for 3 hrs after the high temperature oxidation at 1100ºC followed by 30 min annealing in inert atmosphere of Ar gas. The ultra-dry oxide is grown in dry O_2 ambient at a high temperature of 1100ºC having less than 1 ppm H_2O in O_2. This results in about six times lower BT density as shown in the results and discussion section of this article. This reduces the total interface trap density in the MOS device and increases the peak surface FE mobility in the MOSFET device, given that the peak FE mobility is limited by the Coulomb scattering mechanism at the inverted interface of the MOSFET [5].

II. Theory

The two concepts of interface trap density and peak surface FE mobility in a MOSFET device are correlated with inverse proportionality between the two at low oxide fields giving the following formula [5]:

$$\frac{\mu_2}{\mu_1} = \frac{D_{it1}+D_{bt1}}{D_{it2}+D_{bt2}} \qquad (1).$$

Here, μis the peak surface FE mobility in the MOSFET device and D_{it} and D_{bt} are the interface trap density and border trap densities at the semiconductor/insulator interface. The above formula can be used when one absolute measurement of mobility and total interface trap density is known from a MOSFET and the corresponding MOS device.

There are four main type of interface states present at the SiO_2/SiC interface. There are 'fast' states due to dangling bonds of Si and Carbon, right at the interface known as P_b and P_{bC} centres. Then, there are donor and acceptor interface states due to carbon interstitials, dimers or clusters in the lower and upper half of the bandgap

of 4H-SiC. There are deep acceptor states due to the bulk semiconductor defects such as $Z_{1/2}$ and EH_5 in SiC, and finally there are border traps as near-interface oxide traps near the SiC conduction band (CB) associated with the E' centre in the SiO_2 about 2-3 nm in the oxide near the interface which are electrically active 'slow' traps dominant at low frequencies of less than or equal to 100 Hz [3, 6-7]. There are many methods of finding the density of interface traps which are embodied in an excellent 900 pages textbook by E.H. Nicollian and J.R. Brews [8]. The fastest technique that covers the entire bandgap of the semiconductor is the high-low C-V technique which is predominantly used in the SiC MOS studies, although the conductance technique pioneered by Nicollian is the most accurate. The author has devised a new method of finding the border trap density [1-3, 6]. The method could also be considered as an I-V based method of finding positive fixed oxide charge density in a good quality oxide with negligible bulk traps.

Bulk mobility in a semiconductor is basically defined as the drift velocity in cm/s per unit electric field in V/cm giving the unit of $cm^2/V\text{-}s$. It is more involved than this basic definition. From the studies of the Si MOSFETs, it is learnt that the surface FE mobility in a MOSFET device in inversion is limited by three main effects. At low oxide fields, the Coulomb scattering at the interface of the SiO_2/semiconductor limits the peak FE mobility. Surface phonon scattering and surface roughness limits the surface FE mobility in the MOSFET device in inversion at higher oxide fields. The present article mainly focusses on the peak surface FE mobility. The relation is presented in the author's earlier article [5].

III. Results and Discussion

In the Si VLSI technology of the 1970s and 1980s, dry oxidation of the Si <100> surface was usually performed with less than 1 part per million (ppm) water by passing the gas through a cold trap [9]. Oxidation in dry oxygen was preferred for minimum fixed oxide charge number density Q_f/q of $10^{11}/cm^2$ [10]. In the study of the 6H and 4H-SiC MOS devices, wet re-oxidation has shown to lower oxide charges and interface states in the p-type devices, but forms deep acceptor type border traps of high density of 24 x $10^{11}/cm^2eV$ near the CB in the n-type devices [1-3, 7], with higher interface trap density and Carbon content at the interface that results in higher BT density of the Si-C-O-O type [4]. The increased interface state density of 50 x $10^{11}/cm^2eV$ at E_c-0.2 eV in the n-type 4H-SiC MOS device after wet re-oxidation has also been shown by Pippel et al. [11]. This high BT density is reduced by six times to less than 4 x $10^{11}/cm^2eV$ in the MOS devices having ultra-dry oxides grown with less than 1 ppm water in O_2 oxidation ambient. This is calculated by the new method of finding BT density [6], and is presented below in column 3 of Table I using the I-V characteristics given in Fig.9 of reference [12]. The reference [13] provides the BT density in dry oxides and oxygen plasma grown oxides on 4H-SiC with NO annealing in columns 5 and 6 of Table I. They can be observed to be in the 1-5 x $10^{11}/cm^2eV$ range. The reduced BT density with ultra-dry oxide will reduce the total interface trap density in the MOS devices and will significantly increase the surface FE mobility in the MOSFET device according to equation (1). This is calculated and presented in Table II below for various oxidation conditions in 4H-SiC MOS devices including the above.

Table I. Border trap density in silicon dioxides grown in different oxidation and annealing conditions.

Parameter/Type of high temperature oxide grown at 1100-1200°C	Dry/Wet oxide at 1100°C with Ar anneal +Wet re-oxidation at 950°C for 3 hrs + NO anneal at 1150-1175°C for 2 hrs. Ref. [1-3]	As-oxidised dry (<1 ppm H_2O in O_2) thermal oxide on 4H-SiC Ref. [12] (from I-V of Fig.9)	Dry thermal oxide on Silicon Ref. [6] (from Table I of reference)	Dry thermal oxide on 4H-SiC with NO annealing at 1175°C for 2 hrs Ref. [13] (from Table I of reference)	Oxygen Plasma Oxide grown at 850-950°C on 4H-SiC with NO annealing at 1175°C for 2 hrs Ref. [13] (from Table I of reference)
Near-Interface Trap or Border Trap Density, D_{bt} (x $10^{11}/cm^2eV$)	24 (at all fields till FN onset field)	0.71 (at 2MV/cm oxide field) 3.6 (at 5.5 MV/cm oxide field just before FN onset)	4.0 (No anneal) 0.8-1.25 (inert N_2 anneal) (at 6.5 MV/cm oxide field just before FN onset)	1.2 – 6.1 (by different methods)	1.0-5.0 (by different methods)

Several observations can be made from the Table I above. First, density of BTs given as D_{bt} is reducing as the water content in the oxidation ambient is reducing. This implies that the formation of the interfacial oxygen vacancy defect is dependent on the water content in the oxidation ambient. Second, D_{bt} is field-dependent as presented in column 3 of the table. It has also been demonstrated by Afanasev et al. [14]. Third, NO annealing does not change the density of BTs. Fourth, there is no difference in D_{bt} values in the high temperature dry oxides grown on Si [6] and 4H-SiC with no-anneal condition and about 3 times difference after inert N_2 anneal in Si MOS devices. The minimum BT densities of 1.25 x $10^{11}/cm^2eV$ in Si MOS and 3.6 x $10^{11}/cm^2eV$ in 4H-SiC MOS could be related as a factor of three due to Si-C-O-O E' centre with a corresponding positive charge centre

in 4H-SiC MOS and Si-O-O-O E' centre with a corresponding positive charge centre in Si MOS. Carbon containing 2 less electrons than Oxygen can cause a 3 times change in the minimum positive fixed charge density in p-4H-SiC MOS or BT density in the n-type device.

The high temperature NO annealing of the SiO_2/SiC interface at to 1175°C for 2 hrs passivates the Si and Carbon dangling bonds and the Carbon-based donor and acceptor states by forming CN bonds that become located in energy near the valence band (VB). The interface states density due to the bulk semiconductor defects of EH_5 and $Z_{1/2}$ located at E_v + 2.2 eV and E_v+ 2.6 eV also get reduced to 10^{11}/cm^{2}eV level after NO annealing [15-16]. The Table II below shows the significantly enhanced mobility of 63 cm^2/V-s in the MOSFET device due to the reduction of mainly the density of BTs (D_{bt}) by choosing to oxidise the Si-face of 4H-SiC epi-surface in ultra-dry oxidation ambient containing less than 1 ppm water. Here, the formula in equation (1) is used to calculate the mobilities, given that the FE mobility of N_2 annealed Si-MOSFET having a SiO_2/HfO_2 stack with EOT of 1 nm provides a mobility of 140cm^2/V-s as device 1 in equation (1) [17]. The Si-MOSFET device has the total interface trap density of 10 x 10^{11}/cm^{2}eV [18]. The ultra-dry condition is not specified in reference [16] and the D_{it} at E_c-0.1 eV could be lower after NO annealing if the oxide in reference [16] is not grown in ultra-dry condition and will be grown in the ultra-dry condition. The resulting surface FE mobility could then be higher than 63cm^2/V-s.

Table II. Total interface trap density versus FE mobility for ultra-dry and wet re-oxidised oxidation condition in 4H-SiC MOS devices.

Oxidation Condition	D_{it} atE_c-0.1eV (x 10^{11}/cm^{2}eV)	D_{bt} (x 10^{11}/cm^{2}eV)	D_{it} + D_{bt} (x 10^{11}/cm^{2}eV)	Peak Surface Field Effect (FE) mobility (cm^2/V-s)
Dry (<1ppm H_2O) Ox at 1100°C with 30 min Ar anneal + NO annealing at 1175°C for 2 hrs.	18 Ref. [16]	3.6 (from I-V at 5.5 MV/cm ox field just before FN onset) 0.71 (from I-V at 2MV/cm ox field) Fig. 9, Ref. [12] (As-oxidised)	~22	~ 63 (projected)
Dry/Wet Ox at 1100°C with 30 min Ar anneal + Wet Reox at 950°C for 3 hrs + NO anneal at 1175°C for 2 hrs.	16 Ref. [15]	24 Ref. [1-3, 7] (from I-V and Quasi-static C-V)	40	~ 35 Ref. [7, 19]

Four other cases of enhanced mobility are observed from the survey of research papers. One, a peak FE mobility of 100 cm^2/V-s is observed when the (0338) surface of 4H-SiC is utilized in fabricating a MOSFET device having 50 nm dry NO annealed oxide [20]. Two, a peak FE mobility of 57 and 45cm^2/V-s is observed in a MOSFET having dry oxide grown at 1150°C followed by 30 min Ar anneal on the Si-face of 4H-SiC (1120) and (0001) oriented epi-surface, which is then NO annealed at 1175°C for 2 hrs [21]. In this device, the ultra-dry condition of less than 1ppm water in the oxidising ambient is not mentioned and therefore could be a case of not-so-dry oxide with larger border trap density. The D_{it} observed at E_c-0.1 eV is nearly 10 x 10^{11}/cm^{2}eV after NO annealing. Three, a peak FE mobility of 140 and 230 cm^2/V-s is observed with a buried channel. This however is only observed sharply at the lower oxide field [22]. Four, a recent study on a MOSFET with NO annealed deposited oxide gives a peak FE mobility of 55 cm^2/V-s even with a low total interface trap density of less than 5 x 10^{11}/cm^{2}eV [23].

IV. Conclusions

The foremost conclusion drawn is that an ultra-dry oxide having less than 1ppm water in the oxidising O_2 ambient grown on Si-face of 4H-SiC (0001) oriented epi-surface gives a six times lower border trap density when compared to a device having wet re-oxidised oxide. This will yield a substantially higher peak surface field-effect mobility in the MOSFET device because of the lowering of the total interface trap density. The second conclusion drawn is that the cause for high BT density in wet re-oxidised oxide is the larger water content in the oxidising ambient and higher Carbon content at the SiO_2/SiC interface. The third conclusion drawn is that the MOSFET fabricated on the (0338) oriented surface of 4H-SiC gives a peak FE mobility of 100 cm^2/V-s. The buried channel device gives only a sharp FE mobility of 140 and 230 cm^2/V-s at low oxide voltage. Lastly, the origin of positive fixed oxide charges in a good quality oxide with negligible bulk traps appears to be the border traps in both Si and SiC MOS devices.

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