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# High Speed Comparators for Analog-To-Digital Converter

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***Abstract***: *High speed devices such as ADC, operational amplifier are of great importance and for this high speed application, a major thrust is given towards low power methodologies. Minimization in power consumption in these device can be achieved by smaller feature size processes. Dynamic comparator are being used in today's A/D converters extensively because of their speed , lesser power dissipation , zero static power consumption and full-swing digital level output voltage in shorter time duration. Back to back inverter in these dynamic comparator provides positive feedback mechanism which convert a smaller voltage difference in full scale digital level output. A pre-amplifier based comparator can amplify a small input voltage difference to a large enough voltage to overcome the latch offset voltage and reduce the kickback noise. However the pre-amplifier based comparator suffer large static power consumption as well as reduced intrinsic gain with the reduction of the drain to source resistance due to continuous technology scaling.*

***Keyword***: *Comparators ,High speed Analog-to-digital converter ,Regenerative comparator.*

## I. Introduction

Comparators are second most widely used electronic component, after operational amplifier. It is also known as single bit analog- to- digital converter and due to that in today technology they are mostly used in high speed A/D converter. A/D converter during its conversion process get sample signal at the input of the comparator to determine the digital output, hence the input analog signal is converted into digital domain. The input to output conversion of a comparator depends upon the decision making response time of the comparator. Comparator has many application such as in switching power regulator circuit ,BLDC operating motors, data transmission etc. The functionality of these comparator is to determine whether a signal is smaller or larger than zero, it can also be used to compare an input signal with reference signal and produce binary signal at the output based on the comparison.

## II. Definition

Comparator can be simply define as a circuit that compare two signal(voltage). The input signal that are applied at the input must be analog in nature and the output must be digital signal base on the comparison at the input. The schematic of voltage comparator is shown in Fiigure-1(a), and Figure-1(b) shows its ideal transfer characteristic. Vp is the input voltage(pulse) applied to the positive input terminal of comparator and Vn is the reference voltage (constant DC voltage) applied to the negative terminal of comparator . if Vp, is at higher potential than the Vn, the output of the comparator is logic 1,where as if the Vp is at lower potential than Vn , the output is logic 0.

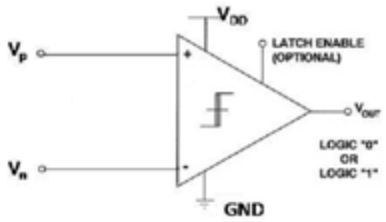


Fig -1(a) Schematic of voltage comparator

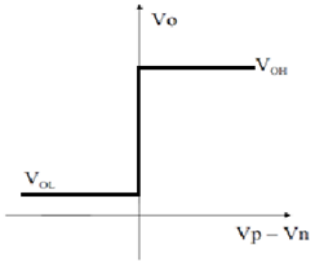


Fig-1(b) Ideal transfer characteristic of a comparator

If Vp >Vn , then Vo = logic 1
If Vp< Vn , then Vo = logic 0

## III. Comparator Types

Comparator can be of two types: Open loop comparator and Regenerative comparator. The open loop comparator is similar to sense amplifier or flip flop . The regenerative comparators are as follows

## A. **Preamplifier Based Comparator**

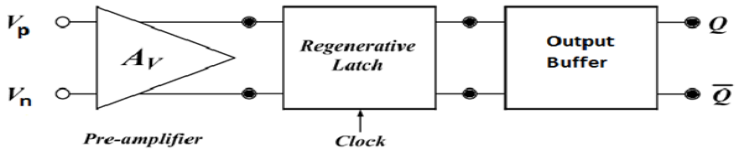


Fig 2 :-Block diagram of Preamplifier based comparator

The Block diagram of preamplifier based comparator is shown in the Fig 2 .It is shown that it consists of three Blocks preamplifier, regenerative latch and output buffer. Preamplifier stage can amplify a small input voltage difference to a large enough voltage to overcome the latch offset voltage, thereby reduce kickback noise[7]. However the preamplifier based comparator suffer large static power consumption as well as from the reduced intrinsic gain with a reduction of the drain to source resistance $r_{ds}$ due to the continuous technology scaling. The Fig :-3 shows the preamplifier based comparator (it is basically a self bias differential amplifier followed by an inverter which gives the digital output).

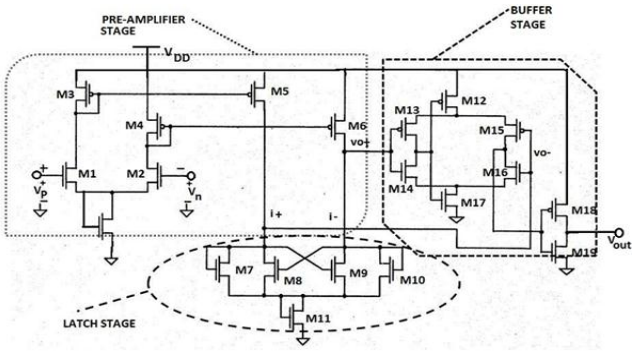


Fig 3 :- Preamplifier based comparator[4]

The preamplifier stage is basically a differential amplifier with active load, amplify the input signal to improve the comparator sensitivity ( i.e increase the maximum input signal with which the comparator can make a decision ) and isolates the input of the comparator from switching noise (often called kickback noise) coming from the positive feedback stage [7]. It also can reduce input referred latch offset voltage the size of M1 and M2 are set by considering the differential amplifier transconductance and the input capacitance. The transconductance sets the gain of the stage ,while the size of the transistor M1 and M2 provides the input capacitance of this comparator. The positive feedback latch stage is used to determine the input signal and amplify their differences. It takes positive feedback from the cross gate connection of M8 and M9. Consider i+ >> i- so that M7 and M9 are ON and M8 and M10 are OFF. Here also $\beta_7=\beta_{10}=\beta b$ for which Vo- is ~0V and V0+ is Vo+ $=\sqrt{(i+/\beta_a)} + V_{th}$.

If we start to increase i- and decrease i+, when drain to source voltage of M9 is equal to the threshold voltage , $V_{th}$ of M8, switching takes place. At this point M8 takes current away from M7 which decreases drain to source voltage ofM7 and M9 turns off, if we assume that maximum value of V+ or V- is equal to $2V_{th}$ , then under this circumstances M8 and M9 operate under cut-off or triode region under steady state condition [7].then voltage across M9 becomes V and it enters into saturation region. The current mode of M9 is

i- = $(\beta_b/\beta_a)$i+

This is the point at which switching takes place ;i.e. M9 turns off and M8 turns on. if $\beta_a=\beta_b$ , then switching takes place when the currents, i+ and i-, are equal. A similar analysis of increasing i+ and decreasing i- result in

i+ = $(\beta_b/\beta_a)$ i-

The output buffer, converts the output of the latch into a full scale digital level (logic 0 or logic 1). The output buffer should accept a differential input signal and not have slew-rate limitations. Buffer is basically a self-biased differential amplifier followed by an inverter. The inverter is added as a separate additional gain stage and isolates any load capacitance from differential amplifier [7]

In summary, the preamplifier based comparator offers high speed and less offset voltage but huge static power consumption.

## B. Fully Dynamic Latch Based Comparators

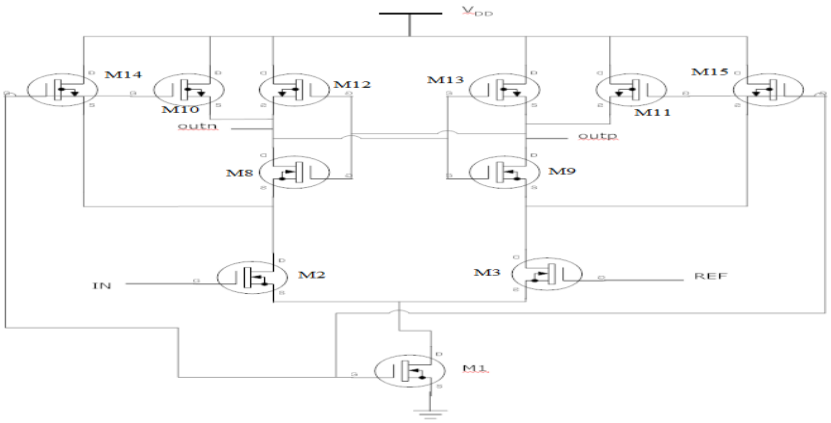


Fig- 4 A Latch Type Voltage Sense Amplifier [1, 2].

Latch type sense amplifier are used to read the contents of the different type of memory , A/D converters, data receivers and on-chip transistors as they yield fast decision due to positive feedback [3].Figure 4 shows the circuit diagram of the latch type voltage sense amplifier to generate positive feedback. This circuit was introduce in 1993 by kobayashi [1]. The current flow of the differential input transistors M8 and M9 controls the latch circuit. A large output voltage is produce due to current flow in the differential input transistors M8 and M9 . Extra switching transistors M10 and M11 are added to increase its characteristics. These circuits are used in sense amplifier based flip-flop, current-sensed SRAM [2].

**Operation:** During reset phase when clk=0V, the output nodes of the comparator are reset to VDD through the reset transistors M10 and M11. During evaluation phase when clk=VDD, M1 turns ON and the input transistors M2 and M3 starts to discharge Ni node voltages to GND. When any of Ni node voltages falls from VDD to VDD-$V_{tn}$ , NMOS transistors of the cross coupled inverters turn ON initiating positive feedback. Further when any of outn voltage drops to VDD-$V_{tp}$ PMOS transistors of the inverters turns ON and further enhances the positive feedback and converts a small input voltage difference to large full scale output.

**Drawbacks :** To increase the drive current of the cross-coupled latch stage, M1 has to be size up. If size of M1 is increased, then the drain currents of both M2 and M3 will be increased during the evaluation phase (clk = VDD). Because of that the Ni nodes of M2, M3 will be discharged from VDD to ground in a very short period because of which the time duration of M2 and M3 being operated in the saturation region decreases. Hence the lower amplification of the input voltage difference will be made. Moreover this structure shows very strong dependency on speed with different common mode input voltages, it is now become less attractive for ADCs [5]. Using this Sense Amplifier in low-voltage deep-sub-micron CMOS technologies is difficult because stack of the four transistors requires large voltage headroom. Speed and offset of Sense Amplifier is very much dependent on the common mode voltage of the input because of which it is problematic to use in A/D converters where wide common mode ranges are used [3].

## C. Double-Tail Latch Type Voltage Sense amplifier

Figure 5 shows the schematic of the Double-Tail Latch type Voltage Sense Amplifier. Double-Tail derived from the fact that the comparator uses one tail for input stage and another for latching stage. It has less stacking and can therefore operate at lower supply voltages [3].Large size of the Transistor M14 enables large current at latching stage which is independent of common mode voltages at inputs and small size of M1 offers lower supply voltages resulting lower offset.

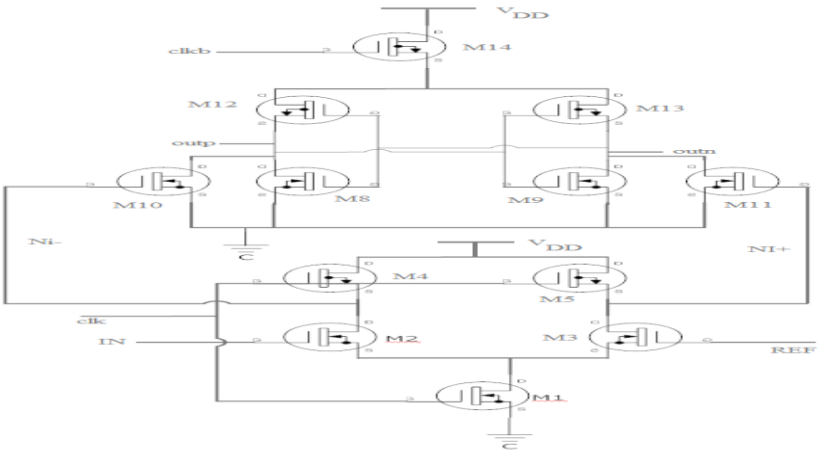


Fig- 5 Double-Tail Latch Type Voltage Sense Amplifier [3]

**Operation:** During rest phase (clk = 0V), M4 and M5 charges to VDD which in turn charges Ni nodes to VDD. Hence M10 and M11 turns on and discharges output nodes to GND. During evaluation phase (clk=VDD), the tail current transistors M1 and M14 turns ON. On Ni nodes common mode voltage decreases and one input dependent differential mode voltage generates. M10 and M11 pass this differential mode voltage to latch stage. The inverters start to regenerate the voltage difference as soon as the common-mode voltage at the Di nodes is no longer high enough for M10 and M11 to clamp the outputs to ground [3]. M10 and M11 also provide additional shielding between the input and output which in turn reduces kickback noise.

**Disadvantages :** clk and clkb requires high accuracy timing because the latch stage has to regenerate the differential input voltage coming from input stage at very limited time. if we replace the clkb with the inverter whose input is clk signal then clk has to drive heavier load in order to drive largest transistor M14 in a smallest possible delay. Now if clkb leads clk, then comparator will undergo increased power dissipation and if clkb lags clk, it results in increased delay means less speed of operation due to short circuit current path from M14 to M10/M11 through M12/M13 [5].

## D. Energy Efficient Two Stage Comparator

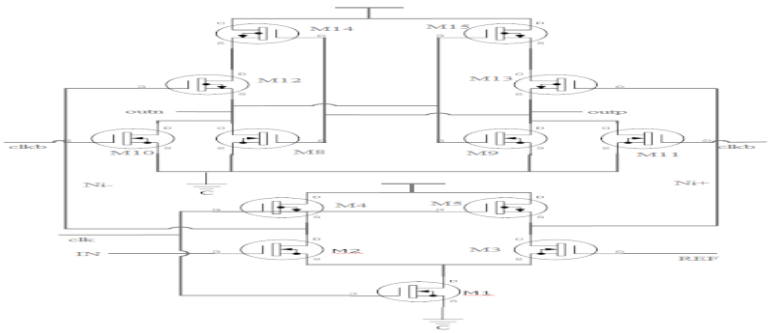


Fig- 6: Two-Stage Comparator [8]

Figure 6 shows the Energy efficient two-stage comparator. The circuit is almost same as Figure.2.3 except the output latch stage. By modifying the output latch stage during reset phase (clk=0V and clkb=VDD), the drain diffusion capacitances of PMOS transistors M14 and M15 & NMOS transistors M2 and M3 is much lesser than the Ni node capacitances. And hence it can be operated in lesser power dissipation and higher speed than the previous comparator. But still the clocking problem was not solved since clk and clkb is operating in same clock signal as that was in previous comparator.

### E. Dynamic Comparator Without Calibration

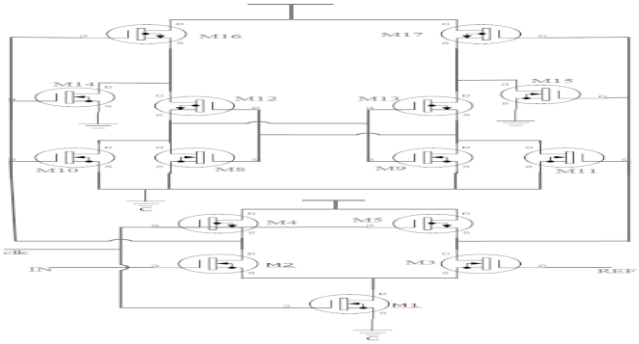


Fig-7 Self-Calibrating Dynamic Comparator [4]

Figure 7 shows the Self-Calibrating Dynamic Comparator. This comparator resolved the above said problem by replacing clkb signal with Ni nodes. But it results in increased delay since transistor M16/M17 use Ni node voltages as their input signal which shows a slow exponential decay shape and hence the current drivability of the output node decreases. The input referred latch offset is also reduced in this circuit due to the fact that output latch stage takes load from the M10/M11 and M16/M17. Maximum drive current of the output node also decreased to half since the supply voltage VDD has been divided into two transistors

### F. Double-Tail Dual-Rail Dynamic Latched Comparator

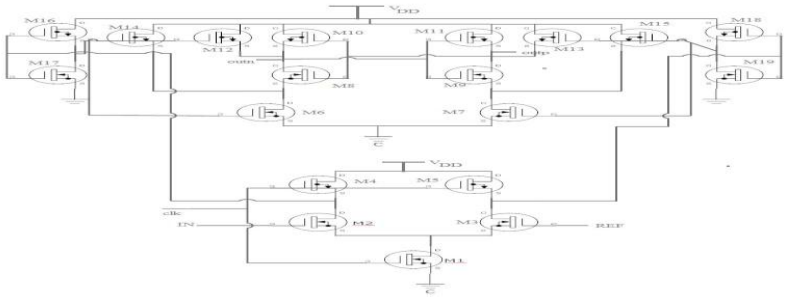


Fig-8 Double-Tail Dual-Rail Dynamic Comparator

Figure 8 shows the Schematic of the Double-Tail Dual-Rail Dynamic Comparator. The above comparator eliminate weakened Ni nodes by inserting an inverter between input and output stages. Due to inverter, weak signal of Ni node is regenerated and fed to the output stage. The above comparator shows faster operation and hence has lesser power dissipation than the previous comparators.

## IV. Conclusion

Comparators are the fundamental building block in analog-to-digital converters (ADC). Today's high speed ADCs(i.e flash ADCs) requires small chip area, low power ,high speed. High speed comparator in CMOS Technology are suffering from low supply voltage. Hence designing High speed comparator is more challenging when supply voltage is low. Hence we have to think some technique to meet the low voltage design challenges in high speed ADCs.

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