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# Power Quality Improvement by IUPQC with Fuzzy Control Technique

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***Abstract:*** *This paper proposes a new connection for a unified power quality conditioner (UPQC) to improve the power quality of two feeders in a distribution system. A UPQC consists of a series voltage-source converter (VSC) and a shunt VSC both joined together by a common dc bus. It is demonstrated how this device is connected between two independent feeders to regulate the bus voltage of one of the feeders while regulating the voltage across a sensitive load in the other feeder. Since the UPQC is connected between two different feeders (lines), this connection of the UPQC will be called an interline UPQC (IUPQC). The structure, control and capability of the IUPQC with PI and FUZZY controller technique are discussed in this paper. The efficiency of the proposed configuration has been verified through simulation studies using MATLAB.*

***Index Terms*****:** *distribution static compensator (DSTATCOM), distribution system, dynamic voltage restorer (DVR), fuzzy logic controller, power quality (PQ), Interline unified power quality conditioner (IUPQC) .*

## I. Introduction

Voltage Source Converter (VSC) based custom power devices are increasingly being used in custom power applications for improving the power quality (PQ) of power distribution systems. Devices such as distribution static compensator (DSTATCOM) and dynamic voltage restorer (DVR) are the facts devices. A DSTATCOM can compensate for distortion and unbalance in a load such that a balanced sinusoidal current flows through the feeder. It can also regulate the voltage of a distribution bus. A DVR can compensate for voltage sag/swell and distortion in the supply side voltage such that the voltage across a sensitive/critical load terminal is perfectly regulated .A unified power quality conditioner (UPQC) can perform the functions of both DSTATCOM and DVR. The UPQC consists of two voltage-source converters (VSCs) that are connected to a common dc bus. One of the VSCs is connected in series with a distribution feeder, while the other one is connected in shunt with the same feeder. The dc links of both VSCs are supplied through a common dc capacitor. It is also possible to connect two VSCs to two different feeders in a distribution system. In, a configuration called IDVR has been discussed in which two DVRs are connected in series with two separate adjacent feeders. The dc buses of the DVRs are connected together. The IDVR absorbs real power from one feeder and maintains the dc link voltage to mitigate 40% (about 0.6p.u.) voltage sag in the other feeder with balanced loads connected in the distribution system. It is also possible to connect two shunt VSCs to different feeders through a common dc link. This can also perform the functions of the two DVRs mentioned above, albeit with higher device rating. This paper presents a new connection for a UPQC called interline UPQC (IUPQC). The single-line diagram of an IUPQC connected distribution system is shown in Fig. 1.

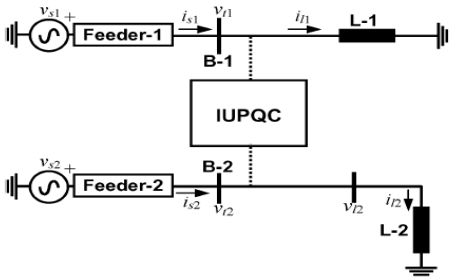



**Fig.1:** Single-line diagram of an IUPQC-connected distribution system.

Two feeders, Feeder-1 and Feeder-2, which are connected to two different substations, supply the system loads L-1 and L-2. The supply voltages are denoted by$V_{s1}$ and $V_{s2}$ It is assumed that the IUPQC is

connected to two buses B-1 and B-2, the voltages of which are denoted by $V_{t1}$ and $V_{t2}$ respectively. Further two feeder currents are denoted by $i_{s1}$ and $i_{s2}$ while the load currents are denoted by $i_{l1}$ and $i_{l2}$. The load L-2 voltage is denoted by $v_{t2}$. The purpose of the IUPQC is to hold the voltages $V_{t1}$ and $V_{t2}$ constant against voltage sag/swell, temporary interruption in either of the two feeders. It has been demonstrated that the IUPQC can absorb power from one feeder (say Feeder-1) to hold $V_{t2}$ constant in case of a sag in the voltage $V_{s2}$ this can be accomplished as the two VSCs are supplied by a common dc capacitor. The dc capacitor voltage control has been discussed here along with voltage reference generation strategy. Also, the limits of achievable performance have been computed. The performance of the IUPQC has been evaluated through simulation studies using MATLAB.

## II. Structure and Control

The IUPQC shown in Fig. 1 consists of two VSCs (VSC-1 and VSC-2) that are connected back to back through a common energy storage dc capacitor $C_{dc}$. Let us assume that the VSC-1 is connected in shunt to Feeder-1 while the VSC-2 is connected in series with Feeder-2. Each of the two VSCs is realized by three H-bridge inverters.

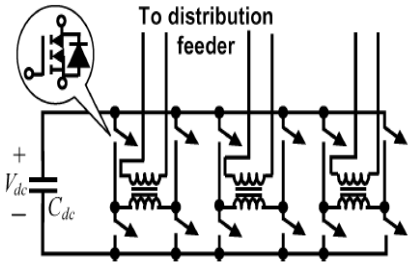



**Fig.2:** Schematic structure of VSC.

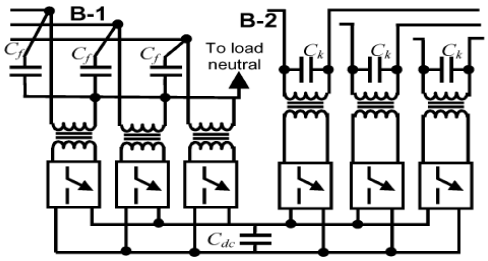



**Fig.3:** Complete structure of an IUPQC.

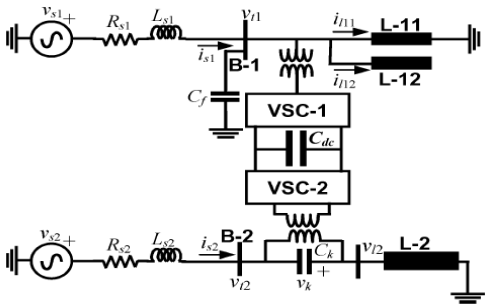



**Fig.4:** Typical IUPQC connected in distribution System

The schematic structure of a VSC is shown in Fig. 2. In this structure, each switch represents a power semiconductor device (e.g., IGBT) and an anti-parallel diode as shown in Fig. 2. All the inverters are supplied from a common single dc capacitor $C_{dc}$ and each inverter has a transformer connected at its output.

The complete structure of a three-phase IUPQC with two such VSCs is shown in Fig. 3. The secondary (distribution) sides of the shunt-connected transformers (VSC-1) are connected in star with the neutral point being connected to the load neutral. The secondary winding of the series-connected transformers (VSC-2) are directly connected in series with the bus B-2 and load L-2. The ac filter capacitors $C_f$ and $C_k$ and are also connected in each phase (Fig. 3) to prevent the flow of the harmonic currents generated due to switching. The six inverters of the IUPQC are controlled independently. The switching action is obtained using output feedback control. The controller is designed in discrete-time using pole-shifting law in the polynomial domain as discussed in Appendix A.

## III. System Description

An IUPQC connected to a distribution system is shown in Fig. 4. In this figure, the feeder impedances are denoted by the Pairs ($R_{s1}$, $L_{s1}$) and ($R_{s2}$, $L_{s2}$). It can be seen that the two feeders supply the loads L-1 and L-2. The load L-1 is assumed to have two separate components-an unbalanced part (L-11) and a non-linear part (L-12). The currents drawn by these two loads are denoted by $i_{t11}$ and $i_{t12}$ respectively. We further assume that the load L-2 is a sensitive load that requires uninterrupted and regulated voltage. The shunt VSC (VSC-1) is connected to bus B-1 at the end of Feeder-1, while the series VSC (VSC-2) is connected at bus B-2 at the end of Feeder-2. The voltages of buses B-1 and B2 and across the sensitive load terminal are denoted by Vt1 and Vt2 respectively. The aim of the IUPQC is two-fold:

1. To protect the sensitive load L-2 from the disturbances occurring in the system by regulating the voltage ($V_{t2}$).
2. To regulate the bus B-1 voltage $V_{t1}$ against sag/swell and or disturbances in the system.

In order to attain these aims, the shunt VSC-1 is operated as a voltage controller while the series VSC-2 regulates the voltage $V_{t2}$ across the sensitive load. The system parameters used in the study are given in Table I. The length of Feeder-1 is arbitrarily chosen to be twice that of Feeder-2. The voltage of bus B-1 and load L-1 currents, when no IUPQC is connected to the distribution system, are shown in Fig. 5.

**Table:1** System Parameters

| System quantities | Values |
|---|---|
| System fundamental frequency (f) | 50Hz |
| Voltage source $V_{s1}$ | 11kV (L-L, rms), phase angle 0° |
| Voltage source $V_{s2}$ | 11kV (L-L, rms), phase angle 0° |
| Feeder-1 ($R_{s1}$+j2πf$L_{s1}$) | Impedance : 6.05+j36.28Ω |
| Feeder-2 ($R_{s2}$+j2πf$L_{s2}$) | Impedance : 3.05+j18.14Ω |
| Load L-11 Unbalanced RL Component | Phase – a 24.2+j60.50Ω<br>Phase – b 36.2+j78.54Ω<br>Phase – c 48.2+j94.25Ω |
| Load L-12 Non-linear component | A three phase diode rectifier that supplies a load of 250+j31.42Ω |
| Balanced load L-2 impedance | 72.6+j54.44Ω |

In this figure and in all the remaining figures showing three phase waveforms, the phases a, b and c are depicted by solid, dashed and dotted lines, respectively. It can be seen from Fig. 5(a) that due to the presence of unbalanced and non-linear loads L-1, the voltage $V_{t1}$ is both unbalanced and distorted. Also, the load L-11 causes an unbalance in the current $i_{t12}$ while load L-12 causes distortion in the current $i_{t11}$. We shall now demonstrate how these waveforms can be improved using the Interline Unified Power Quality Conditioner (IUPQC).

## IV. IUPQC Operation

As mentioned before, the shunt VSC (VSC-1) holds the voltage of bus B-1 constant. This is accomplished by making the VSC-1 to track a reference voltage across the filter capacitor $C_f$ . The equivalent circuit of the VSC-1 is shown in Fig. 6(a) in which $u_l.V_{dc}$ denote the inverter output voltage where is dc capacitor voltage and u1is switching action equal to (+ or – n) where $n_1$ is turns ratio of the losses and leakage inductance of the transformers are denoted by $R_{fl}$ & $L_{fl}$ respectively. All system parameters are referred to the line side of the transformers.

Defining the state space model for the VSC-1 is written as

$$\dot{x}_1 = F_1 x_1 + G_1 z_1$$
$$y_1 = V_{t1} = H x_1 \qquad (1)$$

Where

$$F_1 = \begin{bmatrix} 0 & 1/Cf \\ -1/Lf1 & -Rf1/Lf1 \end{bmatrix}$$

$$G_1 = \begin{bmatrix} 0 & -1/Cf \\ Vdc/Lf1 & 0 \end{bmatrix} \quad H = [1 \quad 0] \quad z_1 = \begin{bmatrix} uc1 \\ ish \end{bmatrix}$$

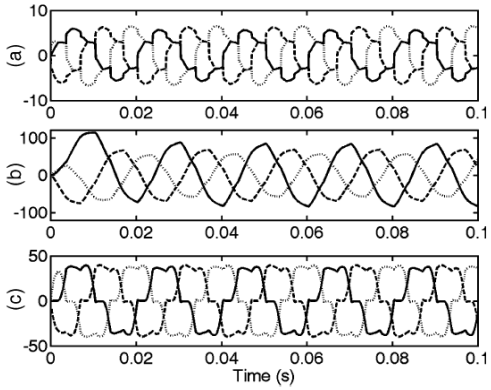



**Fig .5:** Voltage & Currents in the absence of IUPQC: (a) B-1 bus voltage($V_{t1}$), KV, (b) L-11 load current($i_{l11}$),A, & (c) L-12 load current ($i_{l12}$) ,A.

Note that $u_{lc}$ is the continuous time equivalent of $u_l$. The system given in (1) is descretized and is written in input–output form as

$$A_1(z^{-1})y_1(k) = B_1(z^{-1})u_{1c}(k) + C_1(z^{-1})n_1(k) \qquad (2)$$

Where $n_1$ is a disturbance which is equal to $i_{sh}$. A pole-shift controller is used to determine the switching action $u_l$ from $u_{lc}$. The controller is discussed in Appendix A and is used to track a reference signal $y_{1ref}(k)$.

The reference $y_{1ref}(k)$ is the desired voltage of the bus B-1.The peak of this instantaneous voltage is pre-specified and its has angle is adjusted to maintain the power balance in the system. To set the phase angle, we note that the dc capacitor (in Fig. 4) must be able to supply VSC-1 while maintaining its dc bus voltage constant by drawing power from the ac system. A proportional controller is used for controlling the dc capacitor $V_{dc}$ voltage and is given by

$$\delta_1 = K_p (V_{dcref} - V_{dcav}) \qquad (3)$$

Where $V_{dcav}$ is the average voltage across the dc capacitor over a cycle $V_{dcref}$ is its set reference value and is the proportional gain. It is to be noted that the average voltage is obtained using a moving average low pass filter to eliminate all switching components from the signal.

**Table:2** IUPQC Parameters

| System quantity | Parameters |
|---|---|
| System frequency | 50Hz |
| VSC-1 single phase transformers | 1 MVA,3/11kV<br>10% Leakage reactance |
| VSC-2 single phase transformers | 1 MVA,3/11kV<br>10% Leakage reactance |
| Losses | $R_{f1}$=6.0Ω<br>$R_{f2}$=1.0Ω |
| Leakage reactance | $2\pi f L f_1$=12.1Ω<br>$2\pi f L f_2$=12.1Ω |
| Filter capacitor ( Cf) | 50 µF |
| Filter capacitor ( Ck) | 30 µF |
| DC capacitor ( Cdc) | 3,000 µF |
| $V_{dcref}$ | 6.5kV |

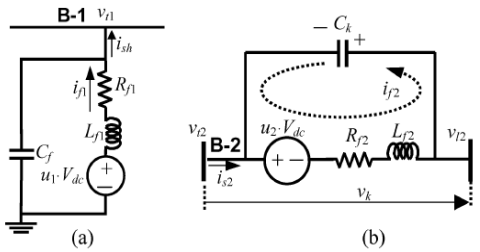



**Fig.6:** Single-phase equivalent circuit of (a) VSC-1 & (b) VSC-2.

The equivalent circuit of the VSC-2 is shown in Fig. 6(b) and is similar to the one shown in Fig. 6(a) in every respect. Defining a state and input vector, respectively, as $x_2^T = [V_k \;\; i_{f2}]$ and $z_2^T = [u_{2c} \;\; i_{s2}]$ and the state space model for VSC-2 is given as

$$\dot{x}_2 = F_2 x_2 + G_2 z_2$$
$$y_2 = V_k = H x_2 \qquad (4)$$

Where $F_2$ and $G_2$ are matrices that are similar to $F_1$ and $G_1$, respectively. The discrete-time input–output equivalent of (4) is given as

$$A_2(z^{-1})y_2(k) = B_2(z^{-1})u_{2c}(k) + C_2(z^{-1})n_2(k) \qquad (5)$$

Where the disturbance $n_2$ is equal to $i_s$. We now use a separate pole-shift controller to determine the switching action from so as to track the reference signal $y_{2ref}(k)$ .

Note from Fig. 4 that the purpose of the VSC-2 is to hold the voltage across the sensitive load L-2 constant Let us denote the reference load L-2 voltage as $V_{l2}^*$. Then the reference $y_{2ref}(k)$ is computed by the application of Kirchhoff's voltage law as [see Fig. 6(b)]

$$y_{2ref} = V_{l2}^* - V_{t2} \qquad (6)$$

We shall now demonstrate the normal operation of the IUPQC through simulation using MATLAB IUPQC parameters chosen are listed in Table II and the system parameters are given in Table I. It can be seen from Fig. 7(a), that the three-phase B-1 voltages $V_{t1}$, are perfectly balanced with a peak of 9 kV. Once these voltages become balanced, the currents drawn by Feeder-1, $i_{s1}$ ,also become balanced. The load L-2 bus voltages $V_{t2}$, shown in Fig. 7(c) are also perfectly sinusoidal with the desired peak of (9 kV) as the converter VSC-2 injects the required voltages in the system. The bus B-2 voltages can be seen to have a much smaller magnitude (about 7.75 kV peak). The dc capacitor voltage $V_{dc}$ is shown in Fig. 8(a). It can be observed that it has a settling time of about 4 cycles (0.08 s) and it attains a steady-state value of about 4.17 kV. The phase angle ($\delta_1$) shown in Fig. 8(b) settles at -33.88.

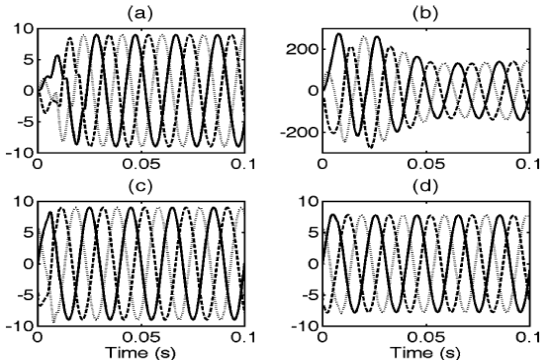



**Fig.7:** System performance with an IUPQC: (a) B-1 bus voltage($V_{t1}$), kv,(b)Feeder-I current($i_{s1}$), A,(c) L-2 load voltage($V_{l2}$), kv, (d) B-2 bus voltage($V_{t2}$), kv.

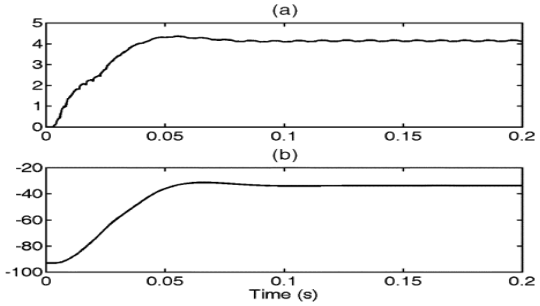



**Fig.8:** (a) DC capacitor voltage ($V_{dc}$), kV, and (b) phase angle of B-1 bus voltage ($\delta_1$), deg.

## V. Transient Performance of IUPQC

*A. Voltage Sag in Feeder-1*

With the system operating in the steady state, a 5 cycle (100ms) voltage sag occurs at 0.14 s in which peak of the supply voltage, reduces to 6.5 kV from their nominal value of 9 kV. The various waveforms of only one phase (phase-a) are shown in Fig. 9. The trends in the other two phases are similar. It can be seen that the dc capacitor voltage, drops as soon as the sag occurs. If the bus voltage remains constant, the load power also remains constant. However, since the source voltage has dropped, the power coming out of the source has

reduced. In order to supply the balance power requirement of the load, the drops. To offset this, the angle retards such that the power supplied by the source increases. As the sag is removed, both the voltage and phase angle returns to their steady state values. The current through Feeder-1 is also shown in Fig. 9. It can be seen that in order to supply the same load power at a reduced source voltage, the feeder current increases. Also, the transients in this current occur at the inception and the removal of the sag due to the change in the source voltage.

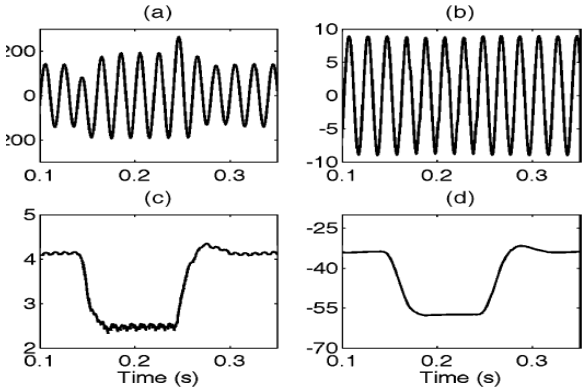



**Fig.9:** System response during voltage sag in Feeder-1: (a) phase-a Feeder-1 current, A, (b) phase-a B-1 bus voltage, kV, (c) DC capacitor voltage ($V_{dc}$), kV, and (d) phase angle of B-1 bus voltage ($\delta_1$), deg.

It has been observed that bus B-1 voltage starts getting distorted when the voltage sag causes the peak of the source voltage to drop below 6.0 kV. Also, for deeper voltage sags, the peak of reduces and the VSC-1 is not able to hold the bus voltage. The next sub-section explains the cause for this.

*B. Voltage Sag in Feeder-2*

With the system operating in the steady state, Feeder-2 is subjected to a voltage sag at 0.14 s in which the peak of all three phases of the supply voltage reduces to 3.0 kV from their nominal value of 9.0 kV. The sag lasts for 5 cycles (100 ms). The system response is shown in Figs. 10. The bus B-2 voltage, the dc link voltage, and the angle are shown in Fig. 10. It can be seen that $v_{dc}$ drops to around 2.3 kV during the sag while $\delta_1$ retards to about -60 degrees.

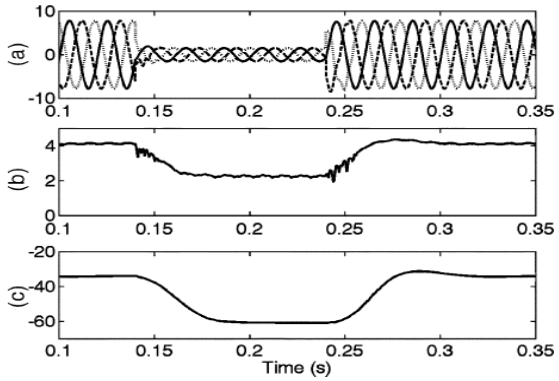



**Fig.10:** (a) B-2 bus voltages ($v_{t2}$), kV (b) DC capacitor voltage ($V_{dc}$ ), kV, and (c) phase angle of B-1 bus voltage ($\delta_1$), deg.

*C. Upstream Fault in Feeder-2*

The performance of the IUPQC is tested when a fault (L-G, L-L-G, and three-phase to ground) occurs in Feeder-2 at bus B-2. The system response is shown in Fig. 11 when a 10 cycle L-G fault occurs at 0.14 s such that the a-phase of B-2 bus voltage becomes zero. When the fault occurs, the power fed to load L-2 by Feeder-2 is reduced. To meet the power requirement of the load L-2, the dc capacitor starts supplying this power momentarily. This causes the dc capacitor voltage to drop from 4.1 kV to 3.5 kV. It can be seen from Fig. 11(b), that the L-2 load voltages remain balanced throughout the fault period.

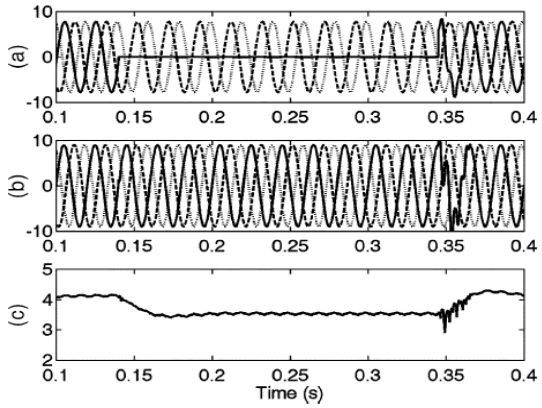



**Fig.11:** System response during L-G fault at bus B-2: (a) B-2 bus voltages ($v_{t2}$), kV, (b) L-2 load voltages ($v_{l2}$), kV, and (c) DC capacitor voltage ($V_{dc}$), kV.

The system response is shown in Fig. 12 when a 10 cycle L-L-G fault occurs at 0.14 s such that both the a and b-phases of B-2 bus voltage become zero. B-2 bus voltages are shown in Fig. 12(a). It can be seen from Fig. 12(b), that the L-2 load voltages remain balanced. However, the dc capacitor voltage now drops to about 2.65 kV and $\delta_1$ from -34 deg to -55 deg. Still it is enough to regulate both the load voltages.

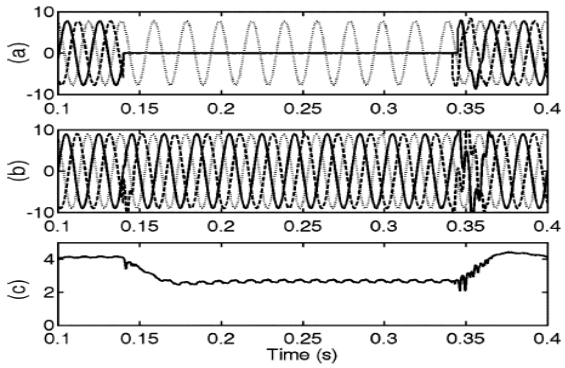



**Fig.12:** System response during L-L-G fault at bus B-2 (a) B-2 bus voltages ($v_{t2}$ ), kV, (b) L-2 load voltages ($v_{l2}$ ), kV, and (c) DC capacitor voltage ($V_{dc}$ ), kV.

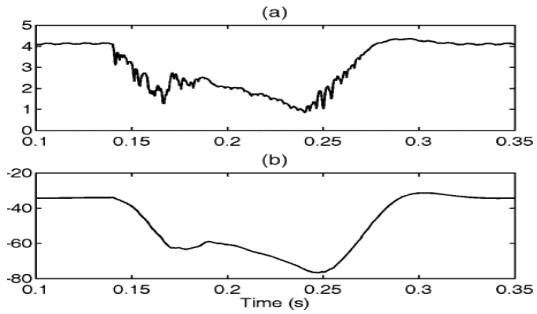



**Fig.13:** (a) DC capacitor voltage ($V_{dc}$), kV, and (b) phase angle of B-1 bus voltage (δ1) in deg. for a fault at B-2.

Now, the system performance has been tested when a three phase fault occurs at 0.14 s in Feeder-2 at bus B-2 such that the voltage becomes zero. The system response is shown in Figs.13 and 14 where the fault is assumed to last 5 cycles only. When the fault occurs, the power fed to load L-2 by Feeder-2 becomes zero. To meet the power requirement of the load L-2, the dc capacitor starts supplying this power momentarily. This causes the dc capacitor voltage to drop and, to offset the voltage drop, the angle retards. As a result, power is drawn from the source through Feeder-1 and supplied to both the loads L-1 and L-2. These two quantities regain their nominal steady state values once the fault is cleared. This is evident from Fig.13.

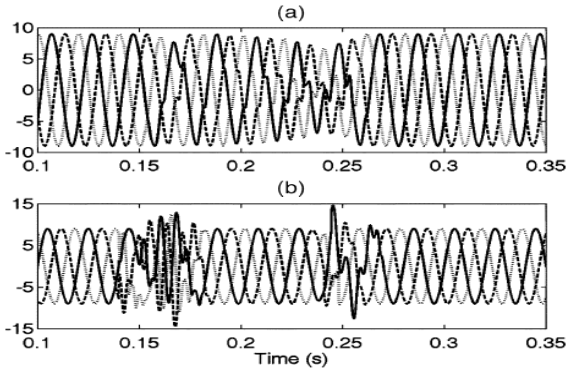



**Fig.14:** (a) B-1 bus voltages ($v_{t1}$), kV and (b) L-2 load voltages ($v_{l2}$) in kV for a fault at bus B-2.

The bus B-1 voltage and the load L-2 voltage are shown in Fig.14. It can be seen that barring transients at the beginning and at the end of the fault, the voltage across the sensitive load remains balanced and sinusoidal. However, since the angle drops below -75 deg, the bus B-1 voltage gets distorted and its magnitude also reduces. These voltages, however, regain their nominal values within a cycle of the removal of the fault.

## VI. Fuzzy Logic Controllers

The word Fuzzy means vagueness. Fuzziness occurs when the boundary of piece of information is not clear-cut. In 1965 Lotfi A.Zahed propounded the fuzzy set theory. Fuzzy set theory exhibits immense potential for effective solving of the uncertainty in the problem. Fuzzy set theory is an excellent mathematical tool to handle the uncertainty arising due to vagueness. Understanding human speech and recognizing handwritten characters are some common instances where fuzziness manifests. Fuzzy set theory is an extension of classical set theory where elements have varying degrees of membership. Fuzzy logic uses the whole interval between 0 and 1 to describe human reasoning. In FLC the input variables are mapped by sets of membership functions and these are called as "FUZZY SETS".

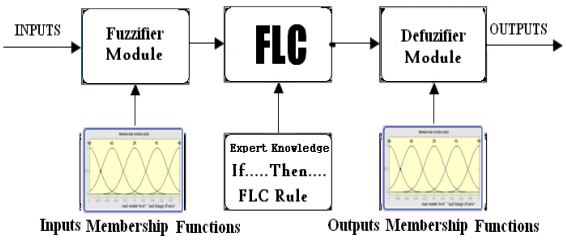



**Fig.15:** Fuzzy Basic Module

Fuzzy set comprises from a membership function which could be defines by parameters. The value between 0 & 1 reveals a degree of membership to the fuzzy set. The process of converting the crisp input to a fuzzy value is called as "fuzzification". The output of the fuzzier module is interfaced with the rules. The basic operation of FLC is constructed from fuzzy control rules utilizing the values fuzzy sets in general for the error, change of error & control action. The results are combined to give a crisp output, controlling the output variable and this process is called "defuzzification".

**Fuzzy Logic Control Rules:**

| $e \backslash \Delta e$ | NB | NM | NS | Z | PS | PM | PB |
|---|---|---|---|---|---|---|---|
| NB | NB | NB | NB | NB | NM | NS | Z |
| NM | NB | NB | NB | NM | NS | Z | PS |
| NS | NB | NB | NM | NS | Z | PS | PM |
| Z | NB | NM | NS | Z | PS | PM | PB |
| PS | NM | NS | Z | PS | PM | PB | PB |
| PM | NS | Z | PS | PM | PB | PB | PB |
| PB | Z | PS | PM | PB | PB | PB | PB |

**Fig.16:** Control Strategy based on 49 Fuzzy control rules with combination of seven error states multiplying with seven changes of error states.

## VII. Simulation Results

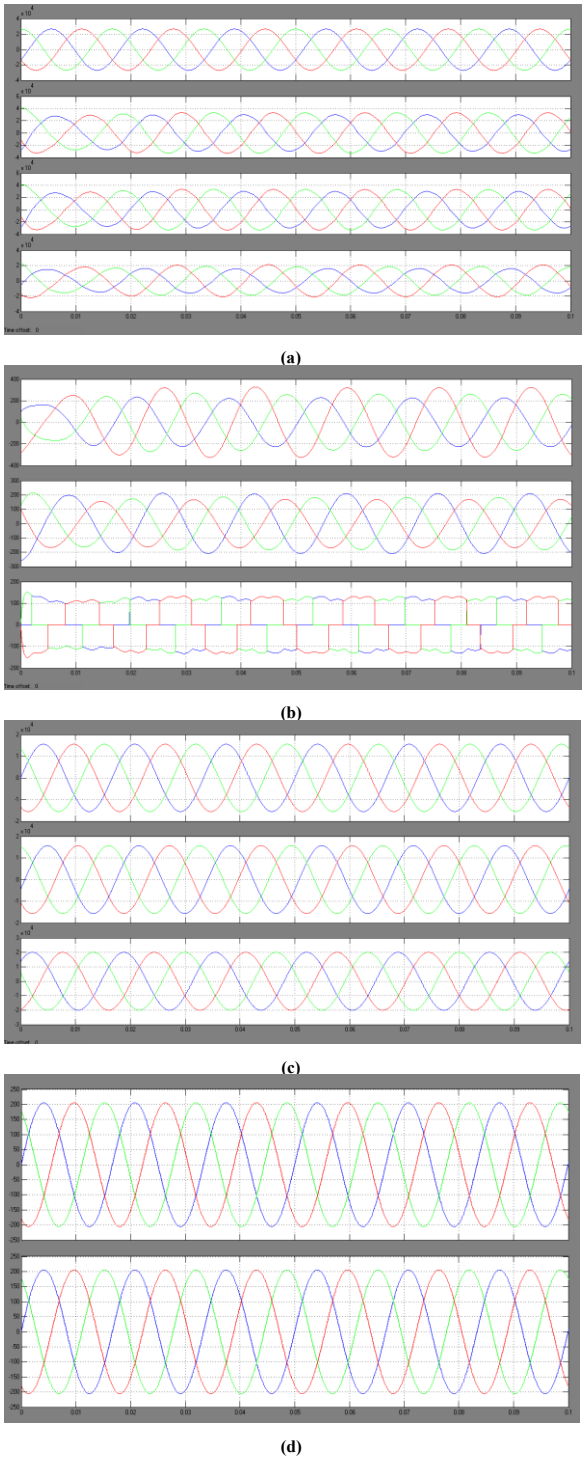



**Fig.17:** Voltages and currents in the absence of IUPQC: **(a)** Feeder-1 source voltages($v_{s1}$), kv, B-1 bus voltages($v_{t1}$), kv, L11 Unbalanced load voltages($v_{L11}$), kv, L12 Non-linear load voltages($v_{L12}$) **(b)** Feeder-1 source currents($I_{s1}$),A, L-11 Unbalanced load currents ($i_{L11}$ ), A, L-12 Non-linear load currents ($i_{L12}$ ), A. **(c)** Feeder-2 source voltage($V_{s2}$), kv, B-2 bus voltage($v_{t2}$), kv, L2 load voltages($v_{L2}$), kv, **(d)** Feeder-2 source currents($I_{s2}$), A, L2 balanced load currents($I_{L2}$), A.

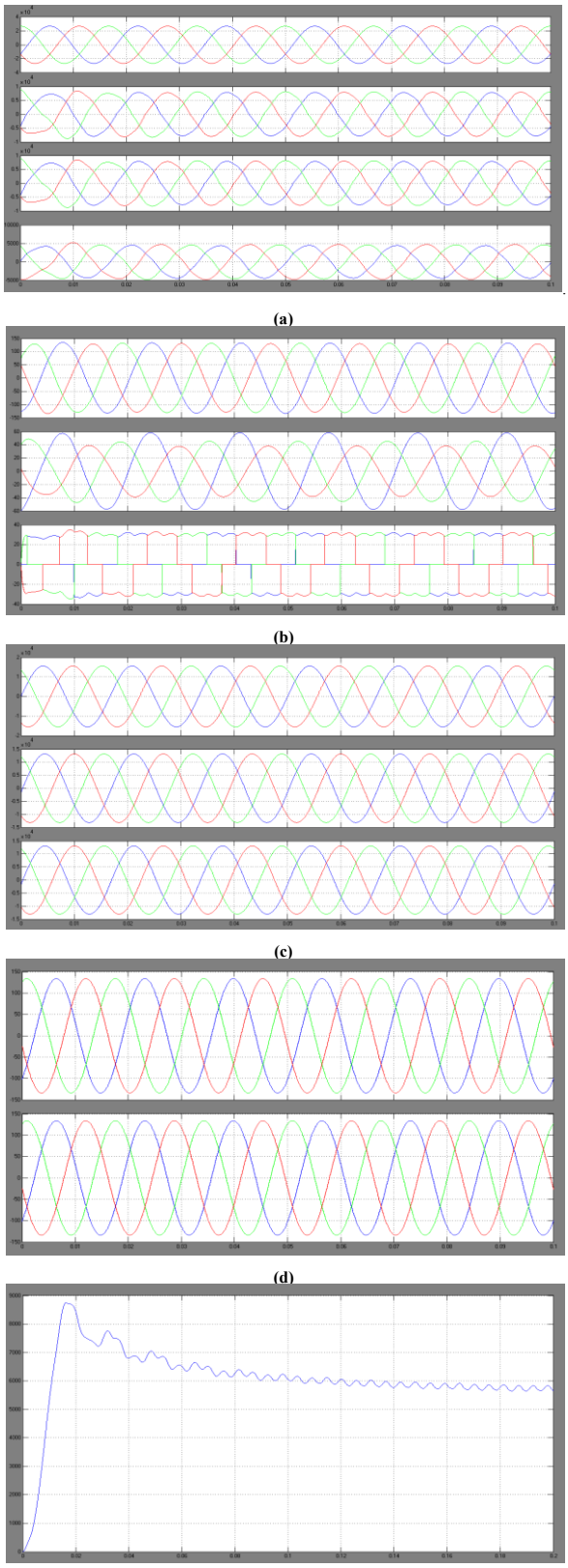
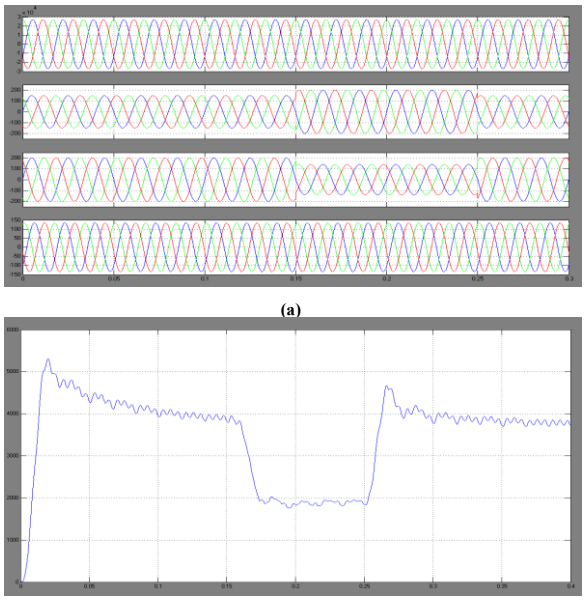


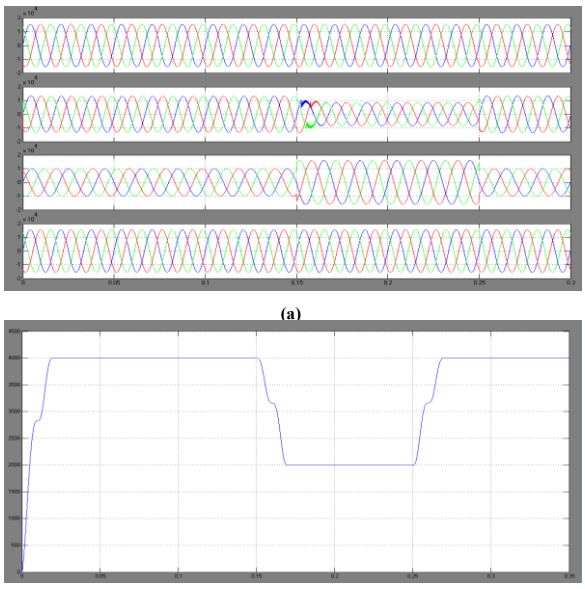

**Fig.18:** System performance with an IUPQC: **(a)** Feeder-1 source voltages($v_{s1}$), kv, B-1 bus voltages($v_{t1}$), kv, L11 Unbalanced load voltages($v_{L11}$), kv, L12 Non-linear load voltages($v_{L12}$) **(b)** Feeder-1 source currents($I_{s1}$),A, L-11 Unbalanced load currents ($i_{L11}$ ), A, L12 Non-linear load currents ($i_{L12}$ ), A. **(c)** Feeder-2 source voltages ($V_{s2}$), kv, B-2 bus voltage ($v_{t2}$), kv, L2 load voltage ($v_{L2}$), kv, **(d)** Feeder-2 source currents($I_{s2}$), A, L2 balanced load currents($I_{L2}$), A, **(e)** DC capacitor voltage ($V_{dc}$), kV.



**(a)**

**(b)**

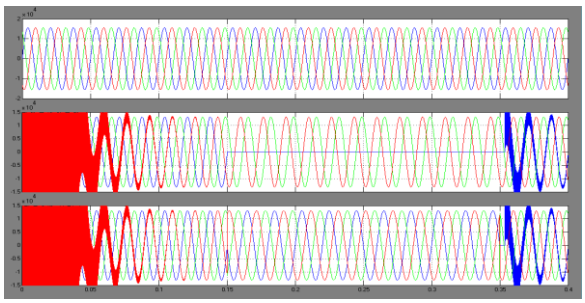
**Fig.19:** System response during voltage sags in Feeder-1: **(a)** Feeder-1 source voltages($V_{s1}$), kv, Bus-1 currents(A), Shunt injected currents ($I_{inj}$), (A), $L_2$- balanced load currents(A), **(b)** DC capacitor voltage ($V_{dc}$), kV.



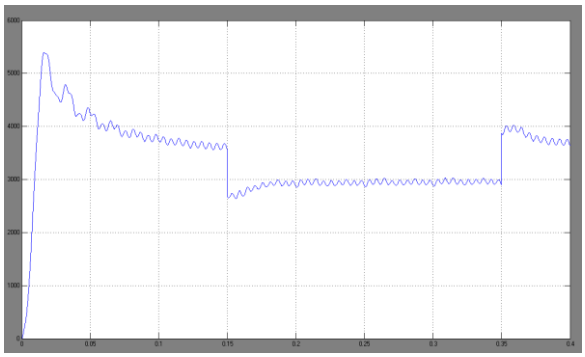
**(a)**

**(b)**

**Fig.20:** System response during voltage sags in Feeder-2: **(a)** Feeder-2 source voltages ($V_{s2}$), kv, B-2 bus voltages ($v_{t2}$), kV, Series injected voltages ($V_{inj}$), kv, $L_2$-balanced load voltages ($VL_2$), kv, **(b)** DC capacitor voltage ($V_{dc}$), kV.

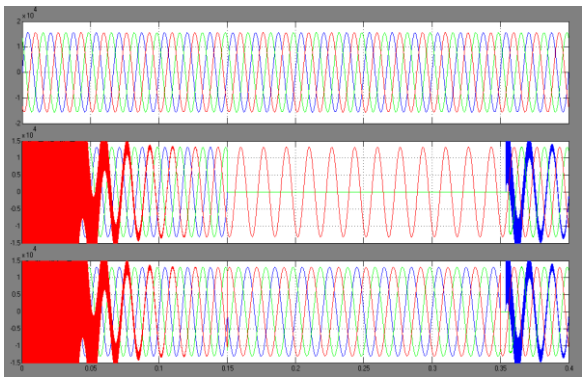


**(a)**

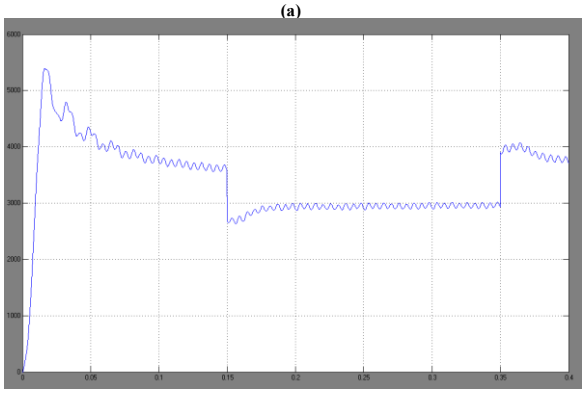


**(b)**

**Fig.21:** System response during L-G fault at bus B-2: **(a)** Feeder-2 source voltages($v_{s2}$), kv, B-2 bus voltages ($v_{t2}$), kV, L-2 balanced load voltages ($v_{l2}$),kV, and **(b)** DC capacitor voltage ($V_{dc}$), kV.

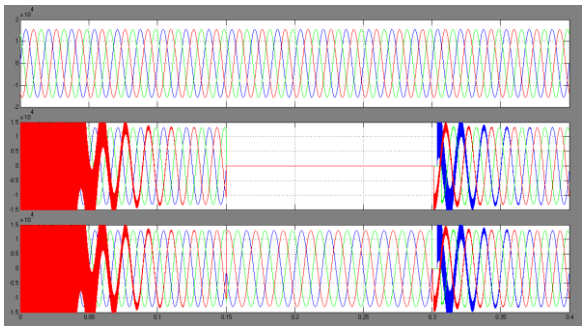


**(a)**

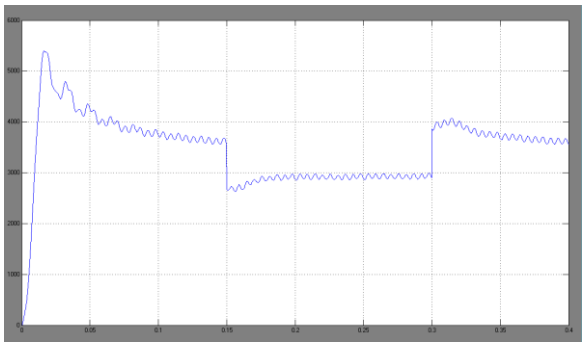


**(b)**

**Fig.22:** System response during L-L-G fault at bus B-2: **(a)**Feeder-2 source voltages($v_{s2}$), kv, B-2 bus voltages($v_{t2}$), kV, L-2 balanced load voltages ($v_{l2}$), kV, and **(b)** DC capacitor voltage($V_{dc}$), kv.

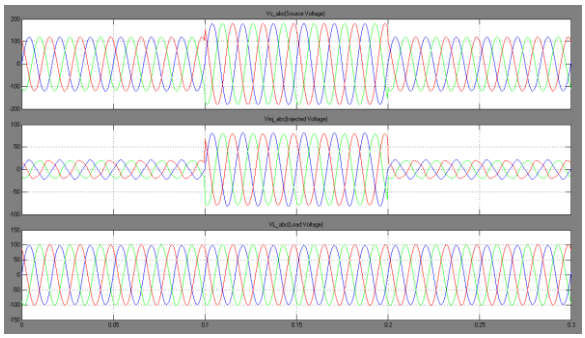


**(a)**

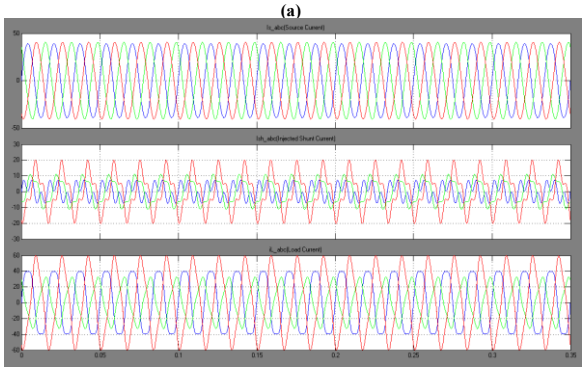


**(b)**

**Fig.23:** System response during three phase to ground fault at bus B-2 **(a)** Feeder-2 source voltages($v_{s2}$), kv, B-2 bus voltages($v_{t2}$), kV, L-2 balanced load voltages ($v_{l2}$), kV, and **(b)** DC capacitor voltage($V_{dc}$), kV.

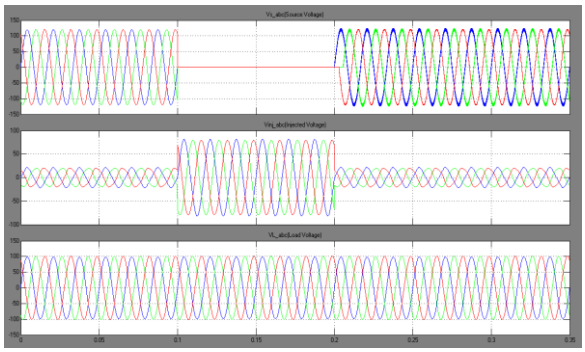


**(a)**

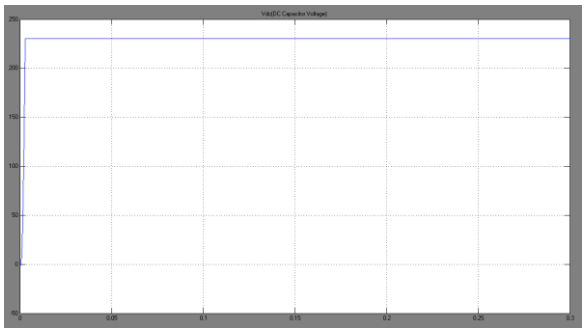


**(b)**

**Fig.24:** System performance with an IUPQC & Fuzzy Controller during voltage swells in Feeder-1 **(a)** B-1 bus voltages ($v_{t1}$), kV, Voltages injected ($V_{inj}$), kv, L1-Unbalanced & Non-linear Load Voltages ($V_{l1}$), kv, **(b)** Bus-1 currents(A), Currents injected ($I_{inj}$), (A), L1-Unbalanced & Non-linear Load currents ($I_{l1}$), A.



**(a)**



**(b)**

**Fig.25:** System performance with an IUPQC & Fuzzy Controller during three phase to ground fault at bus B-2
**(a)** B-2 bus voltages($v_{t2}$), kV, Voltages injected ($V_{inj}$), kv, L-2 Balanced load voltages ($v_{l2}$), kV
**(b)** DC capacitor voltage($V_{dc}$), kV.

## VIII. Conclusions

The paper illustrates the operation and control of an interline unified power quality conditioner (IUPQC). The device is connected between two feeders coming from different substations. An unbalanced and non-linear load L-1 is supplied by Feeder-1 while a sensitive load L-2 is supplied through Feeder-2. The main aim of the IUPQC is to regulate the voltage at the terminals of Feeder-1 and to protect the sensitive load from disturbances occurring upstream. The performance of the IUPQC has been evaluated under various disturbance conditions such as voltage sag in either feeder, fault in one of the feeders and load change. The IUPQC discussed in the paper is capable of handling system in which the loads are unbalanced and distorted. As far as the common dc link voltage is at the reasonable level, the device works satisfactorily. The angle controller ensures that the real power is drawn from Feeder-1 to hold the dc link voltage constant. Therefore, even for voltage sag or a fault in Feeder-2, VSC-1 passes real power through the dc capacitor onto VSC-2 to regulate the voltage $V_{t2}$. Finally when a fault occurs in Feeder-2 or Feeder-2 is lost, the power required by the Load L-2 is supplied through both the VSCs. This implies that the power semiconductor switches of the VSCs must be rated such that the total power transfer through them must be possible. In the IUPQC configuration discussed in this paper, the sensitive load is fully protected against sag/swell and interruption. In conclusion, the performance under some of the major concerns of both customer and utility e.g., harmonic contents in loads, unbalanced loads, supply voltage distortion, system disturbances such as voltage sag, swell and fault has been studied. The IUPQC has been shown to compensate for several of these events successfully.

## Appendix A
## Pole-Shift controller Design For VSC

The discrete-time input-output equation of VSCs given in (2) and (5) can be written in a general form as

$$A(z^{-1})y(k) = B(z^{-1})u_c(k) + C(z^{-1})\eta(k) \qquad (A.1)$$

The aim of the pole-shift controller is to track a reference value that is denoted by yref. The control law is given by [1],[12]

$$uc(k)=\frac{S(z^{-1})}{R(z^{-1})}\ \{yref(k) - y(k)\} \qquad (A.2)$$

Where S and R are controller ploynomials to be deteremined. From (A.1) and (A.2), the closed-loop system equation is then written as

$$y(k)= \frac{B(z^{-1})\,S(z^{-1})\,yref(k)+ C(z^{-1})\,R(z^{-1})\,\eta(k)}{A(z^{-1})\,R(z^{-1})+ B(z^{-1})\,S(z^{-1})} \qquad (A.3)$$

Let the closed-loop characteristic equation be defined by

$$T(z^{-1})= A(z^{-1})\,R(z^{-1}) + B(z^{-1})\,S(z^{-1})n \qquad (A.4)$$

The closed- loop system poles are obtained by radially shifting the open-loop system poles toward the origin by a pole-shift factor $\lambda(0< \lambda <1)$,i.e.,

$$T(z^{-1})= A(\lambda z^{-1})=1+\lambda a_1 z^{-1} +\ldots\ldots+ \lambda n a n z^{-n} \qquad (A.5)$$

The closer λ is to one, the smaller will be the control action. The controller parameters are obtained from the solution of the Aryabatta identify (A.4) and the control input uc(k) is obtained from (A.2). The switching action u is then obtained as

$$u=\begin{cases} +n \text{ for } uc > h \\ -n \text{ for } uc \leq -h \end{cases} \quad \text{(A.6)}$$

Where 2h is a hysteresis band and n is the turns ratio of the connecting transformer.

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