

Efficient Architecture for Image Compression for Lifting Based Discrete Wavelet Transform

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Abstract: *in this paper Efficient architecture for discrete wavelet transform is proposed by using lifting scheme. In arithmetic, a wavelet series is a representation of a square-integrable (real-or complex-valued) function by a certain orthonormal series generated by a wavelet. Lifting based Wavelet transform is mainly comprises of three steps that is split, predict and update, this algorithm allowed high compression ratios, preserving diagnostically important data features. For low-resolution images created with the necessity to keep predefined key diagnostic information (contractile function of the heart), high compression ratios up to 2000 could be achieved.*

Index Terms: *Discrete Wavelet transforms, square integrable function, lifting scheme.*

I. Introduction

The discrete wavelet transform (DWT) is widely used in many image compression techniques, and is used as an ingredient in many image compression standards, such as JPEG2000 etc. This is because the DWT can decompose the signals into different sub bands with both time and frequency information and facilitate to arrive a high compression ratio. The architecture of two-dimensional DWT is mainly composed of the multi rate filters. Because extensive computation is involved in practical applications. The parallel and embedded decimation techniques are employed to optimize the architecture, which is mainly comprise of two horizontal filter modules and one vertical filter module, working in parallel fashion and pipeline fashion. The architecture has been designed to generate two outputs at one working clock cycle, with every two sub bands coefficients alternately, and consuming approximately $2N^2(1-4^J)/3$ clock cycles for computing J levels of decomposition for NxN image. For simplicity but no losing generalization, we introduce the architecture by taking the bi-orthogonal 9/7 wavelet transform as an example.

II. Background

As computing power grows, 3D animation becomes one among the vital parts in communication. 3D animation compression naturally catches attention. There are 2 approaches in 3D animation compression. within the 1st approach, topology is assumed to be static, and there's no or chump change in property. within the second approach, topology might amendment indiscriminately between frames.

III. Proposed Compression Scheme

The data to be compressed is assumed to be regularly sampled, which is mainly used in scientific and medical visualization purpose. New scheme called Lifting Scheme is applied to compress the image and inverse discrete wavelet transform is applied to recover the original image. Because the compression technique is lossy technique, it is complex to recover back the original image. The process is divided into three steps which are split predict and update steps. Which is discussed below?

IV. Lifting Scheme For 2d Wavelet Transform

Lifting scheme is mainly based on spatial to construct wavelet, which comprises of three steps split, predict and update. Lifting wavelet is called the second generation wavelet, the basic principle of which is to break up the poly phase matrices for the wavelet filters into a sequence of upper and lower triangular matrices and convert the filter implementation into banded matrix multiplications. Every finite impulse response filter wavelet can be factored into lifting steps, and the lifting strategy is a highly non-unique process.

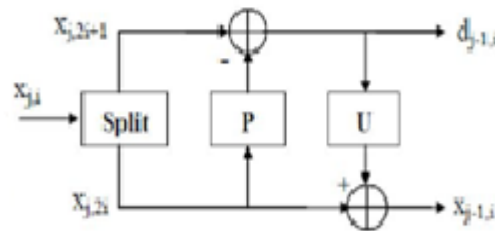


Fig: Lifting Scheme for Forward DWT

Split : First split the data into two steps i.e. even and odd samples. Because of the assumed smoothness of the data we have a tendency to predict that the odd samples have a worth that's closely connected therefore their neighboring even samples.

Predict : We use n even samples to predict the value of a neighboring odd value. With a good prediction method the change is high that the original odd sample and its prediction and replace the odd sample with its difference. As long as the signal is highly correlated, the newly calculated odd samples will be on the average smaller than the original one and can be represented with fewer bits. The odd half of the signal is transformed. To transform the other half samples, we will have to apply the predict step on the even half as well, because the even half is merely a sub-samples version of the original signal, it has lost some properties that we want to preserve. In the case of images we might keep the intensity (mean of samples) throughout different levels.

Update : The third step updates the even samples using the newly calculated odd samples such that the desired property is preserved. We apply these three steps repeatedly on even samples and transform each time half of the even samples. Up to all samples are transformed.

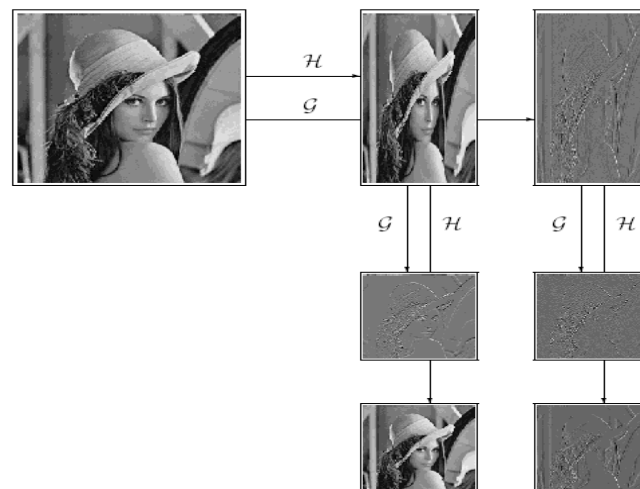


Figure: Wavelet Transform of an Image

A. Wavelet Realization and Implementation

Wavelet are the functions that satisfy certain requirements, wave is also referred to as the oscillating function of time and space. The name wavelet comes from the fact that they satisfy the requirement that they should integrate to zero, waiving above and below x-axis. A wavelet is a small wave which has finite energy, with its energy concentrated in time or space to give a tool for the analysis and way of comparison of transient, nonstationary, or time-varying development. The very small requirement of wavelet is that wavelet suggests the function has to be localized. There is many kinds of wavelets one of the most simple form of wavelet is Haar Wavelet. So we can say that wavelet is a wave like oscillation which starts out at zero, increases and then decreases back to zero.

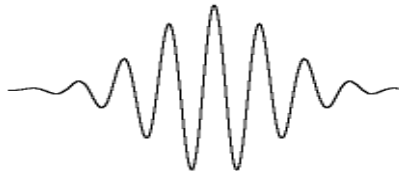


Figure: Wavelet with finite energy.

There are some difference between the Wavelet and Fourier transform. Fourier basis function is localized in frequency but not in time but wavelets are local to both time and frequency. Many class of functions are represented by wavelet in compact form , this makes the wavelet very efficient tool in data compression. Many data operation can be done by processing the corresponding wavelet. One can done data smoothing by thresholding the wavelet coefficient and then return the threshold code to time domain.



Figure: Data analysis by Wavelet

The wavelet transform are successfully applied to non stationary signals(audio, video and data) , and images Wavelet theory is based on analyzing signals to their parts by employing a set of basis functions. Wavelet basis functions is relate to each other by simple scaling and translation. The original or first wavelet function, known as mother wavelet, mother wavelet is mainly designed based on some desired characteristics associated to that function, is used to predict all basis functions. Wavelets are used to analyze signals in much the same way as complex exponentials (sine and cosine functions) employed in Fourier analysis of signals. The compactness and finite energy characteristic of wavelet functions totally differentiate wavelet decompositions from other Fourier like analysis in their applicability to different circumstances. Wavelet functions not solely can be used to analyze stationary signals however conjointly it can be used to decompose nonstationary, time-varying or transient signals.

B. Multirate Filter bank for DWT

The computations of DWT are inner products of the input signal and a family of wavelets. For a length N sequence of input signal, DWT will generate a length N sequence of output values. The value corresponds to the magnitude of the multi -resolution when decomposing the input signal. The expression of DWT can be written as

$$f(x) = \sum_{j=-\infty}^{\infty} \sum_{k=-\infty}^{\infty} c_{j,k} W(2^j x - k)$$

$$= \sum_{k=-\infty}^{\infty} c_{\phi,k} \Phi(x-k) + \sum_{j=0}^{\infty} \sum_{k=-\infty}^{\infty} c_{j,k} W(2^j x - k)$$

where $N(x)$ is the scaling function and $w(x)$ is the wavelet function[S]. DWT can be represented as multi-rate filter banks shown in Fig. 1

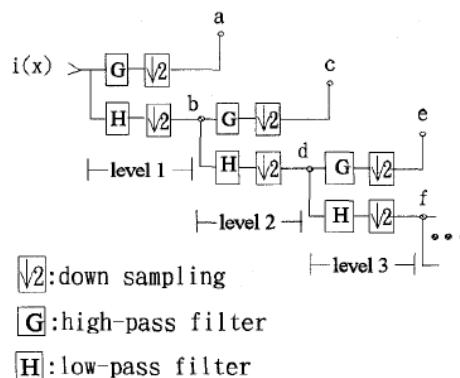


Figure: Multi-rate filter bank for DWT

The bi-orthogonal 5/3 wavelet transform is adopted in JPEG2000 standard to implement lossless compression of image, which can be factored into two stages of lifting. In this paper, we will take it for an example to introduce the proposed architecture for 2-D DWT for simplicity. The conventional lifting factorization for the forward transform of the 5/3 wavelet filters. Each level in figure above is composed of G, H, and down sampling to decompose the input data into two parts. G and H represent the high-pass filter and low-pass filter respectively. Down sampling is to directly output the data every two input data. For convenient description, the three-level DWT which consists of 4-tap G and H filters is used in the following architecture design

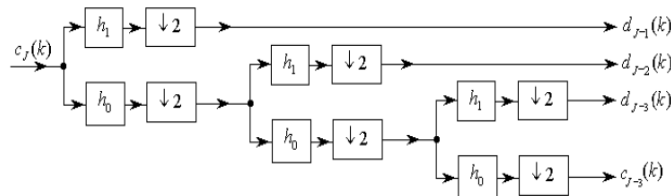


Figure: Three stage wavelet decomposition.

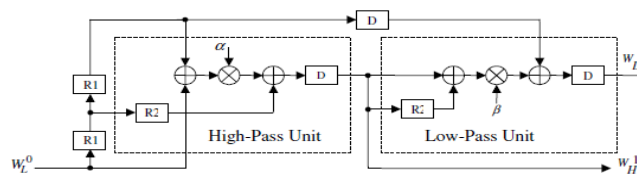
The filter coefficients are saved in shift registers. When the data sequentially inputs to the module, the first input data multiplies to go and g2, then the second input data multiplies to g1 and g3, and so forth. These resulted data is putted into two sets of shift registers. Next, the adders A, B and C are used to sum up the data in shift registers. The whole data flow for the G part is depicted in Fig.(2). If we use this hardware module to construct the entire three-level DWT, it can be found that the utilization for the hardware module in the higher level would become lower. From the above computation equations, the computing times of the level 2 and 3 are a half and a quarter of the level 1 respectively. Therefore, the second level module and third level module can be performed commonly on one module hardware by feeding the output to the input.

C. Methodology

The following equations can be used for computing the high-pass and low-pass coefficients of jth decomposition level of lifting DWT using filters. By using the lifting scheme and the embedded decimation technique, the numbers of adder and multiplier of the proposed architecture arc reduced significantly, which are 4 and 8 respectively.

$$W_H^j(i) = W_L^{j-1}(2i-1) + \alpha[W_L^{j-1}(2i) + W_L^{j-1}(2i-2)] \quad (1)$$

$$W_L^j(i) = W_L^{j-1}(2i-2) + \beta[W_H^j(i) + W_H^j(i-1)] \quad (2)$$



The proposed pipelined architecture for FU1.

TABLE I
DATA FLOW OF SINGLE LEVEL DECOMPOSITION STRUCTURE OF THE LIFTING DWT

Clock	HIGH-PASS UNIT			LOW-PASS UNIT		
	Input	Input	Output	Input	Input	Output
0	$W_L^0(0)$	$W_L^0(2)$	$W_L^0(1)$			
1	$W_L^0(2)$	$W_L^0(0)$	$W_L^0(1)$	$W_H^1(0) \rightarrow W_H^1(0)$	$W_H^1(-1)$	$W_L^0(2)$
2	$W_L^0(4)$	$W_L^0(2)$	$W_L^0(3)$	$W_H^1(1) \rightarrow W_H^1(1)$	$W_H^1(0)$	$W_L^0(0)$
3	$W_L^0(6)$	$W_L^0(4)$	$W_L^0(5)$	$W_H^1(2) \rightarrow W_H^1(2)$	$W_H^1(1)$	$W_L^0(1)$
4	$W_L^0(8)$	$W_L^0(6)$	$W_L^0(7)$	$W_H^1(3) \rightarrow W_H^1(3)$	$W_H^1(2)$	$W_L^0(2)$
5	$W_L^0(10)$	$W_L^0(8)$	$W_L^0(9)$	$W_H^1(4) \rightarrow W_H^1(4)$	$W_H^1(3)$	$W_L^0(3)$
6	$W_L^0(12)$	$W_L^0(10)$	$W_L^0(11)$	$W_H^1(5) \rightarrow W_H^1(5)$	$W_H^1(4)$	$W_L^0(4)$
7	$W_L^0(14)$	$W_L^0(12)$	$W_L^0(13)$	$W_H^1(6) \rightarrow W_H^1(6)$	$W_H^1(5)$	$W_L^0(5)$
8				$W_H^1(7) \rightarrow W_H^1(7)$	$W_H^1(5)$	$W_L^0(6)$
9					$W_H^1(12)$	$W_L^0(7)$

Typical performance comparison of the DWT architectures includes evaluation in terms of the number of multipliers, the number of adders, storage size, computing time, control complexity, latency and hardware utilization. Firstly, we will analysis the performance of the proposed architecture in theory. The computing time has been normalized to the same internal clock rate, and can be easily derived that is $T=2(1-4^J)N^2/3$ where N^2 is the image size, and J denotes the 2D DWT decomposition level.

V. Problem Formulation

Fast architecture for two-dimensional discrete wavelet transform by using lifting scheme, both parallel and embedded decimation techniques are proposed and employed to optimize the architecture, the architecture is mainly composed of two horizontal filter modules and one vertical filter module, works in parallel and pipeline fashion with 100% hardware utilization. The architecture is designed to produce two outputs at one working clock cycle, with every two sub bands coefficients alternately.

VI. Conclusion

A efficient architecture for discrete wavelet transform has been proposed, the architecture is based on lifting scheme of wavelet transform. The transform module of the proposed architecture includes two parallel working horizontal filters and one pipeline working vertical filter. Embedded decimation, parallel and pipeline techniques were adopted to optimize design, reducing significantly the internal memory size and the number of accessing storage, and increasing efficiently the throughput. Compared with the other devices, the proposed architecture has lower hardware cost and control completely, as well as short system latency. The architecture is fast as well as power and area efficient, and has 100% hardware utilization. The design is regular, simple, and well suited for VLSI implementation.

References

- [1] S. Mallat, "A theory for multiresolution signal decomposition: The wavelet representation," *IEEE Trans. Pattern Anal. Mach. Intell.*, vol. 11, no. 7, pp. 674–693, Jul. 1989.
- [2] M. Vishwanath, R. Owens, and M. J. Irwin, "VLSI architectures for the discrete wavelet transform," *IEEE Trans. Circuits Syst. II, Analog. Digit. Signal Process.*, vol. 42, no. 5, pp. 305–316, May 1995.
- [3] H. Y. Liao, M. K. Mandal, and B. F. Cockburn, "Efficient architectures for 1-D and 2-D lifting-based wavelet transforms," *IEEE Trans. Signal Process.*, vol. 52, no. 5, pp. 1315–1326, May 2004.
- [4] P. Wu and L. Chen, "An efficient architecture for two-dimensional discrete wavelet transform," *IEEE Trans. Circuits Syst. Video Technol.*, vol. 11, no. 4, pp. 536–545, Apr. 2001.
- [5] S. Masud and J. V. McCanny, "Reusable silicon IP cores for discrete wavelet transform applications," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 51, no. 6, pp. 1114–1124, Jun. 2004.
- [6] T. Huang, P. C. Tseng, and L. G. Chen, "Generic RAM-based architectures for two-dimensional discrete wavelet transform with line-based method," *IEEE Trans. Circuits Syst. Video Technol.*, vol. 15, no. 7, pp. 910–920, Jul. 2005.
- [7] P. K. Meher, B. K. Mohanty, and J. C. Patra, "Hardware-efficient systolic-like modular design for two-dimensional discrete wavelet transform," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 55, no. 2, pp. 151–155, Feb. 2008.
- [8] A. Benkrid, D. Crookes, and K. Benkrid, "Design and implementation of a generic 2-D orthogonal discrete wavelet transform on an FPGA," in *Proc. IEEE 9th Symp. Field-programming Custom Computing Machines (FCCM)*, Apr. 2001, pp. 190–198.
- [9] P. McCanny, S. Masud, and J. McCanny, "Design and implementation of the symmetrically extended 2-D wavelet transform," in *Proc. IEEE Int. Conf. Acoustic, Speech, Signal Process. (ICASSP)*, 2002, vol. 3, pp. 3108–3111.
- [10] S. Raghunath and S. M. Aziz, "High speed area efficient multi-resolution 2-D 9/7 filter DWT processor," in *Proc. Int. Conf. Very Large Scale Integration (IFIP)*, Oct. 2006, vol. 16–18, pp. 210–215.
- [11] M. Angelopoulou, K. Masselos, P. Cheung, and Y. Andreopoulos, "A comparison of 2-D discrete wavelet transform computation schedules on FPGAs," in *Proc. IEEE Int. Conf. Field Programmable Technology (FPT)*, Bangkok, Thailand, Dec. 2006, pp. 181–188.
- [12] C. Chrysytis and A. Ortega, "Line-based, reduced memory, wavelet image compression," *IEEE Trans. Circuits Syst. Video Technol.*, vol. 9, no. 3, pp. 378–389, Mar. 2000. ZHANG et al.: PIPELINE VLSI ARCHITECTURE FOR FAST COMPUTATION 1785
- [13] M. Ravasi, L. Tenze, and M. Mattavelli, "A scalable and programmable architecture for 2-D DWT decoding," *IEEE Trans. Circuits Syst. Video Technol.*, vol. 12, no. 8, pp. 671–677, Aug. 2002.
- [14] K. G. Oweiss, A. Mason, Y. Suhail, A. M. Kamboh, and K. E. Thomson, "A scalable wavelet transform VLSI architecture for real-time signal processing in high-density intra-cortical implants," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 54, no. 6, pp. 1266–1278, Jun. 2007.