Optimization and Simulation of humidity sensor readout circuitry using two stage op amp

Nidhi Kuriyal[1], Rajeev Kumar[2,] Vishal Ramola[3]
M.Tech. Student VLSI Design Department UTU, Dehradun[1],
Assist. Prof. Electronics Department UCST Dehradun[2],
HOD. ECE Department UTU, Dehradun[3]

Abstract: *In this paper a humidity sensor readout circuitry using two stage opamp is designed. This circuitry is realized in TSMC 0.18μm CMOS Technology. Designing of two-stage op-amps is a multi-dimensional-optimization problem where optimization of one or more parameters may easily result into degradation of others. The OPAMP circuit is designed to exhibit a unity gain frequency of 2.02GHz and exhibits a gain of 49.02dB with a 60.50 phase margin and CMRR 39dB, Slew Rate 154dB, UGB (Unity Gain Bandwidth) are in a higher unity gain frequency under the same load condition. Also presented humidity sensor can achieve good linearity over the relative humidity range from 20% to 80%. The total power dissipation of readout circuitry is 21.8 pW.*
***Terms*:** *CMOS humidity sensor, humidity sensor, Op-Amp.*

I. Introduction

Humidity sensors have a widely used in application areas, including agriculture, climate control, food storage, and domestic appliances. In order to satisfy the requirements of these applications, humidity sensors should provide high sensitivity over a wide range of humidity and temperature and linear response. Other important parameters of the humidity sensors can be listed as long-term stability, response time, and power consumption. A desirable feature of the humidity sensors is their compatibility with standard IC fabrication technologies. There are various types of humidity sensors based on the sensing principle they use, such as resistive, mechanical, gravimetric, capacitive, and thermal humidity sensors. This approach provides a number of advantages. The diodes can be heated up with a low power, and they provide high sensitivity. As the diodes are heated up, no water condensation can occur on the sensing elements.

In most of the electronics circuits the Operational Amplifiers is the most common building blocks. So as the transistor channel length and power supply is reduced then the design of Op amps face continuous challenge. Due to different aspect ratio (W/L), there is a tradeoff among speed, gain, power and the other parameters. The implementation of a CMOS OPAMPs that combines a considerable dc gain with higher unity gain frequency has been a most difficult problem. There has been several circuits design to evaluate this problem. The purpose of the design methodology in this paper is to design accurate equations for the design of high- gain 2 staged CMOS op-amp.

Outline of paper

This paper is organized as follows. Section II- presents the two stage amplifier. Section III- Differential transconductance amplifier and Modeling of sensor diode. Section IV- simulation result of two stage op amp and truth table. Section V- design and simulation of humidity sensor readout circuitry.

II. Two Stage Cmos Op-Amp

The various topologies of a new genus have evolved and been used in applications. Here, we chose a simple pair differential amplifier Immune input amplifier, common source amplifier (high gain) to the output amplifier, a current mirror circuit as bias circuit, and a buffer circuit compensation current as well as a Miller capacitance in series with one another.

For every iteration the entire design procedure above is carried on until the design is simulated for the specifications. For simplicity, only the W/L ratios of transistor in the if an iteration are presented. The value of the compensating capacitor Cc = 4pF to accommodate a variation of +/- 25%

and still give a phase margin greater than 60° since $Cc > 0.22 * C_L$

This topology of the circuit is that of a standard CMOS op-amp. It comprised of three subparts, namely differential gain stage, second gain stage and biasing network. It was found that this topology was able to successfully meet all of the design specifications.

II.1. Differential Gain Stage

The first subsection of interest is the differential gain stage which is comprised of transistor M1 to M4. In figure 1 transistor M1 and M2 are standard N channel MOSFET transistors which form the basic input stage of the amplifier. The gate of M1 is the inverting input and the gate of M2 is the non-inverting input. A differential input signal applied across the two input terminals will be amplified according to the gain of the differential stage. The transconductance of this stage is simply the transconductance of M1 or M2. M3 and M4 are the active load transistors of the differential amplifier. The current mirror active load used in this circuit has three distinct advantages. First, the use of active load devices creates a large output resistance in a relatively small amount of die area.

II.2 Second Gain Stage

The second stage is a current sink load inverter. The purpose of the second gain stage, as the name implies, is to provide additional gain, in the amplifier. Consisting of transistor M5 and M8, this stage takes the output from the drain of M2 and amplifies it through M5 which is in the standard common source configuration. Similar to the differential gain stage, this stage employs an active device, M8, to serve as the load resistance for M5. The gain of this stage is the transconductance of M5 times the effective load resistance comprised of the output resistance of M5 and M8. M8 is the driver while M7 acts as load.

II.3 Bias String

The biasing of the operational amplifier is achieved with only two transistors along with a current source. Transistor M6 and the current source supply a voltage between the gate and source of M7 and M8. Transistor M7 and M8 sink a certain amount of current based on their gate to source voltage which is controlled by the bias string. M6 is diode connected to ensure it operate in the saturation region. Proper biasing of the other transistors in the circuit is controlled by the node voltages present in the circuit itself shown in figure 1.
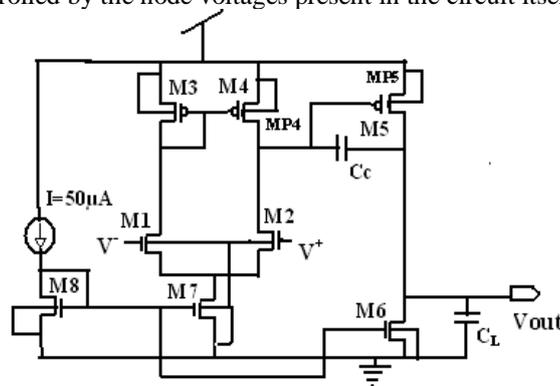
Figure.1. Two stage OPAMP with the compensation capacitor

Table-1: Transistor and size and the electrical parameters yielded of two stage op amp

Design parameters			The electrical parameters yielded	
Tran- sistors	Length	Width	gmI, gmII	806μ, 537μ
M1	0.2 μm	15 μm	Phase margin	60.5^0
M2	0.2 μm	15 μm	C_c	24.8fF
M3	0.4 μm	3.52 μm	DC Gain	53.40
M4	0.4 μm	3.2 μm	Slew rate (+ve, -ve)	154dB
M5	0.2 μm	6.2 μm	CMRR	39dB
M6	0.2 μm	1.6 μm	Noise	164μV/sqrt(Hz)
M7	0.2μm	0.8 μm	PSRR(+ve)	154dB
M8	0.2 μm	0.4 μm	Vdd	3V
Iref	50μA		C_L	10fF
			Power Consumption	0.17 pW

III.   Differential transconductance amplifier:

Differential transconductance amplifier is used for converting the input differential voltage into current output which is integrated by the switch capacitor. The design is shown in figure 2. The maximum differential voltage for which both the input transistor operate in active region is given by the following equation [4]
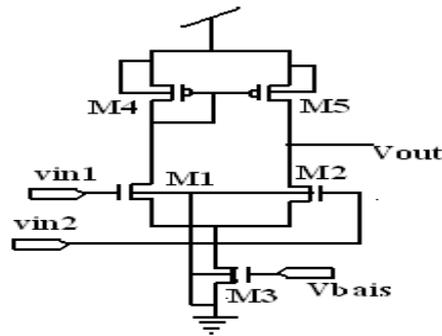
Figure 2. Differential amplifier circuit

III.1. Modeling of sensor diode

As given in [4] the thermal model of the sensor diode with the poly interconnects and air in between the diode and the substrate can be modeled as shown in the figure 3.

RT_{poly} is the thermal conductivity of poly connecting the diodes to the read out circuit, R_{Tair} is the thermal conductivity of air in between diode and the substrate, CT represents the thermal capacitance.
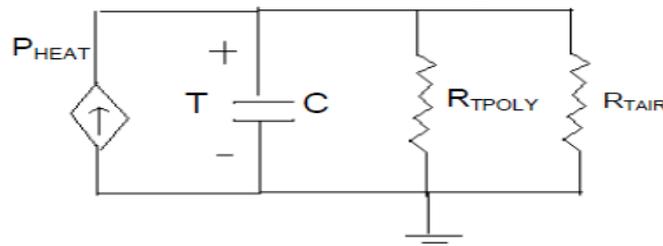
Fig 3: lumped element thermal circuit representing the self heating of a diode biased with constant current [4]

IV.   Switched Capacitor (SC) integrator circuit

The SC integrator correlated double sampling is used for offset compensation due to the finite gain effect of the operational amplifier [5, 6]. The schematic diagram of the switched capacitor (SC) integrator with the differential transconductance amplifier is as shown fig.6. The Sc integrator works in two non-overlapping phases' phi1 and phi2 as shown in fig 6. The switches of the SC integrator are implemented using NMOS. When the clock phase phi1 is high, switches transistor MN3, MN4, MN12, and MN13 are on. In phase phi1 the bottom plate of capacitor C1 is charged to a voltage depending upon the current output from the differential transconductance amplifier through switch MN4 and the top plate of the capacitor C1 forced to ground potential through switch MN3. In phase phi1 the op-amp acts as a voltage follower as the switch MN13 is on. During phi1 high the right plate of capacitor C3 is at ground potential through switch MN12 and the left plate of the capacitor C3 charged to Voffset which is due to the finite gain of the operational amplifier. When phi2 is high switches MN4, MN6, and MN14 are turned on. During this phase the bottom plate of capacitor C3 forced to ground potential through switch MN6, so the inverting input of the op-amp is forced to a negative voltage which was previously present in the bottom plate of the capacitor during phase phi1 let us say Vs. Thus this negative voltage at inverting input of the op-amp swings the output strongly positive. But the input of the op-amp must be at virtual ground due to high gain of op amp. So the capacitive coupling back to the inverting input through C_3 tends to pull the inverting input back towards zero. The circuit settles when the inverting node is once again at a virtual ground, which means that C_1 is now discharged. The positive charge C_1Vs which was on the bottom plate of C1 has flowed to ground while the negative charge ($-C_1$Vs) on the top plate of C_1 has shifted to the left hand plate of C_3. C_1Vs on the top plate of C_1 has shifted to the left-hand plate of C3. This requires that the right – hand plate of C_3 have a charge ($+C_1$Vs). However this charge must equal C_3Vout. Hence, we conclude that the output voltage swings to a value given by

$$Vout = (C_1 / C_3) \ Vs$$

Offset voltage is compensated during phi2 because the left plate of capacitor C_3 was initially charged to a voltage of Voffset.

V.   Simulation results of two stage op amp

The design compensation strategy, the two-stage OPAMP in the figure was designed using the model parameter of tsmc0.18 micron CMOS process. The design parameters along with the electrical parameters yielded are as given in the table 1. This circuit operates efficiently in a closed loop feedback system, while high bandwidth makes it suitable for high speed applications. The circuit operating conditions includes the room temperature as the operating temperature with a power supply of 3V and a load of 10fF.

For the frequency response plot, an ac signal of 1V is swept with 5 points per decade from a frequency of 10KHz to 4GHz. Figure.6 illustrates the frequency response which shows a dc gain in dB versus frequency in Hz(in log scale) and phase margin of OPAMP in open loop. The dc gain is found to be 49.02dB and phase margin 60.50 which is good enough for an OPAMP operating at a high frequency. A unity gain frequency of 2.02GHz is excellent for an OPAMP when all the other parameters are also set at an optimized value.
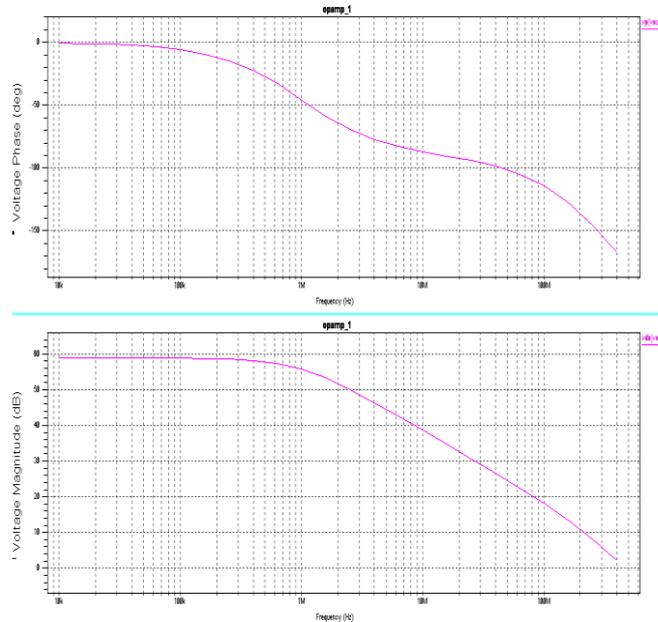
Figure.6: Frequency response of the OPAMP

The slew rate simulation is carried out performing a transient analysis using a pulse waveform of 1mV for a pulse period of 0.5nsec. Slew Rate waveform (V+ is input wave and V- is output) and the calculated Slew Rate is 1.0758 V/uS(+ve slew rate) and 1.13 V/uS(-ve slew rate) respectively, which is quite good as compared to other low power, low voltage OPAMPs. The slew rate response is as shown below---
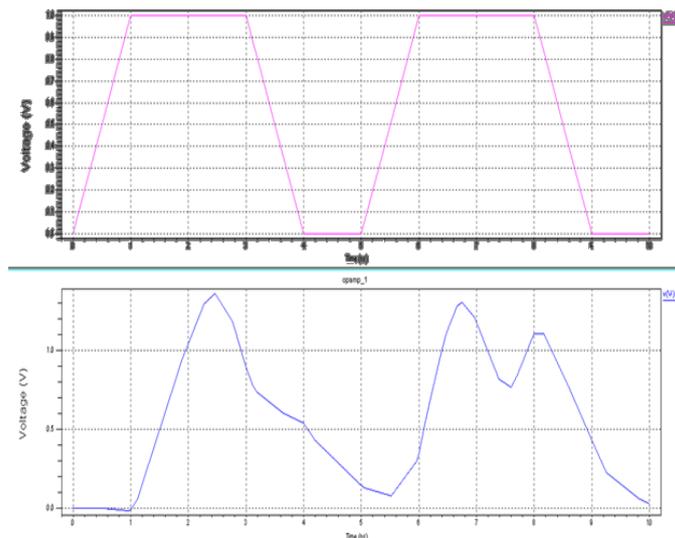
Figure.7. Slew Rate waveform

 The simulate result of CMRR= 39dB
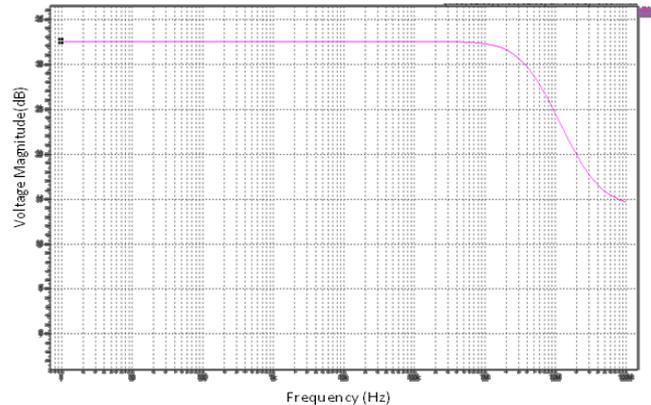
Figure.8. CMRR waveform

VI-1. Results of Differential transconductance amplifier

The operational amplifier and the differential transconductance amplifier are individually simulated using TSPICE in Tanner tool environment. The technology used for simulation is TSMC 180nm technology. The results are as shown in fig 6 &7.The final transistor sizes in the design of op-amp are obtained after many numerical iterations and simulations. For example the design started with a bias current of 50μA and this resulted in low-gain, low phase margin and excess of band width. Hence the bias current is gradually scaled down for meeting the specifications by employing a bias current of 20 +/- 3μa against PVT variations. The value of compensating capacitor Cc = 24.8fF has been taken to accommodate a variation of +/- 25 % and still give a phase margin greater than 60 deg. since Cc > 0.22 * C_L. The supply voltage has been taken as +/- 10% i.e. 4.5 V shown in table 2. The device length has been chosen as 180nm to reduce the short channel effects and keeping channel length modulation constant [6].

The op-amp with the following constraints
i. voltage variation +/- 10% i.e. 4.5V
ii. Bias current variation 20 +/- 3 μA
iii. Temperature variation 20°C to 60°C
iv. Compensating capacitor variation +/- 25%
v. all the process corners (SS, SF, FF, FS, typical)

Table:2

Worst Case Analysis	Bias Current (μA)	Compensating Capacitor(PF)	Temperature (°C)	Voltage (V)	Process Corner
ICMR (Input Common Mode Range) =0 to 2.85V	17	5f	20	4.5	Fast-slow
PM(Phase Margin)=60.5^0	17	5f	60	4.5	Slow-fast
DC Gain=60 db	17	5f	60	4.5	Slow-fast
SLEW RATE =1.078v/μsec	17	5f	60	4.5	Fast-slow
UGB(Unity Gain Bandwidth) =3.0970	17	5f	60	4.5	Slow-Fast
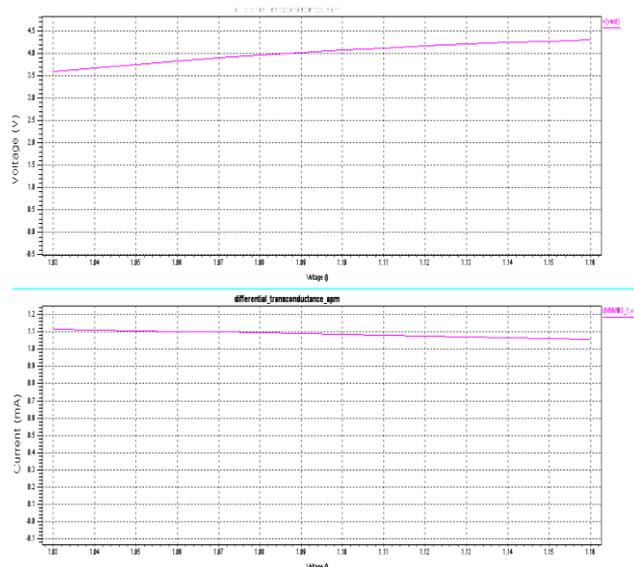
Figure 8: Waveform of Differential transconductance amplifier

VI.   Conclusions

In this paper, a humidity sensor read out circuitry using two stage opamp is designed. The results shows that the two stage operational amplifier optimized has successfully satisfied all the design specification given in advance. The Op-Amp specifications are met under all the process corners. The differential transconductance amplifier has also been designed for the required linear range of operation. The SC integrator and the differential transconductance amplifier are integrated and the output is verified by giving a constant voltage to the Non-inverting input and the sinusoidal voltage to the Inverting input. The design can be used for humidity sensor and can be adopted by the industries for its flexibility in design which would be beneficial from the point of view of production cost of industries.

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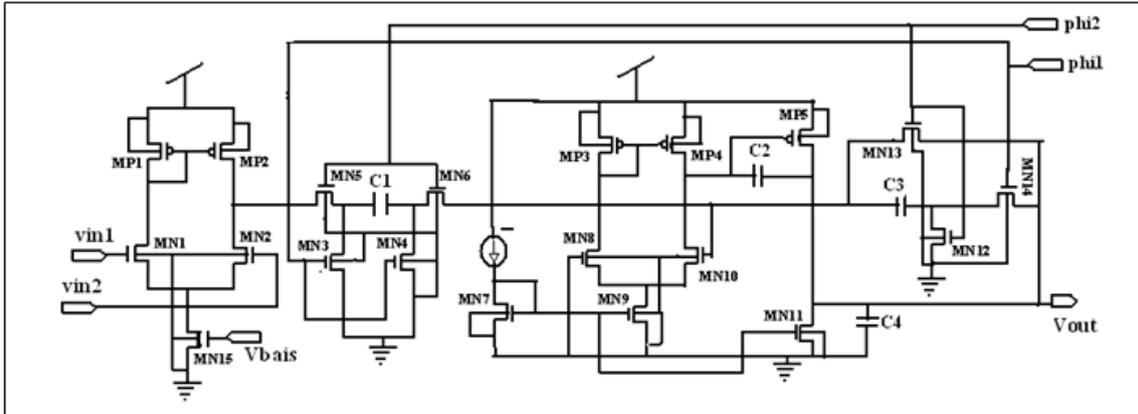
Figure 6: Schematic of humidity sensor with read out circuit
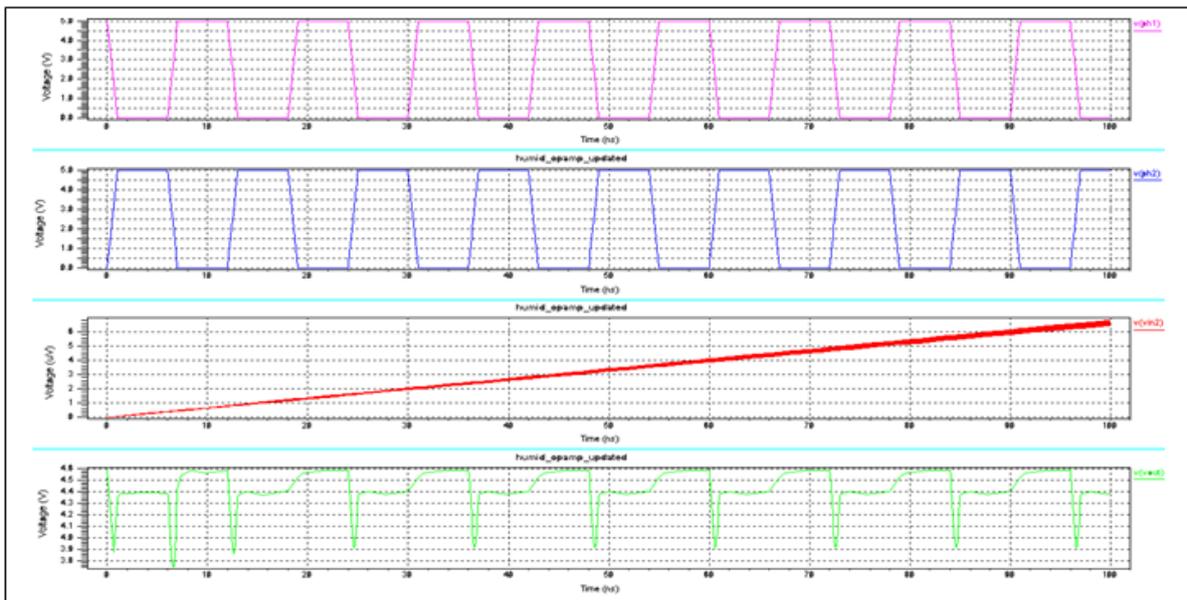
Figure 7: Waveform of humidity sensor with read out circuit