IOSR Journal of VLSI and Signal Processing (IOSR-JVSP)
ISSN: 2319 – 4200, ISBN No. : 2319 – 4197 Volume 1, Issue 2 (Sep-Oct. 2012), PP 35-40
www.iosrjournals.org

Design, Analysis and Simulation of High Performance Low Power 8-Bit ALU at Gate and Layout Levels

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Abstract : *In this work, the demand is to design an 8-bit ALU and perform analysis at gate and layout levels. The design makes use of n-Bit slice concept, the requirement is to design and develop low power high performance circuits. To achieve this, the design requires advanced styles to be employed. High level description language to be used to construct layout of 8-bit ALU and then different analyses will be carried out on this layout.*

Keywords - *ALU, Bit Slice, Low Leakage, Threshold Volatge.*

I. INTRODUCTION

An **Arithmetic and Logic Unit** (ALU) is a digital circuit that performs arithmetic and logic operations. The ALU is a fundamental building block of the central processing unit of a computer, and even the simplest microprocessors contain one. The processors found inside modern CPUs and graphics processing units (GPUs) accommodate very powerful and very complex ALUs, a single component may contain a number of ALUs. The ALU at one machine cycle executes a number of operations. During the process of operations it consumes a lot of power. Due to the power consumed by the ALU has a direct impact in the power dissipated from the processor.

Hence, a design is required to implement the ALU in a fashion where the performance of the processor is improved and also the power consumed is less. This paper provides a simple design of a 8 Bit ALU for a speedy performance.

This paper introduces a technique to design a ALU which consumes less power. Bit slice design is used for the construction of the 8-Bit ALU.

II. Design Of Alu

Arithmetic logic unit (ALU) is a universal combinational device capable of performing both arithmetic and logic operation. The number and complexity of the operations that a given ALU can perform is a designer's choice and varies from ALU to ALU. However the choice of operations is usually drawn from the table shown below:

Operations

Arithmetic operations	Logic operations
Negation	Transfer
Increment	Complementation
Decrement	AND
Addition	OR
Subtract	XOR

Other possible operations include sign complement, magnitude, parity generation, multiplication, division, indices etc. Multiplication, division, indices and related operations like arithmetic shifting are complex and found only in most sophisticated chips.

2.1 1-Bit Slice ALU

ALU accepts two n-bit input operands A_n and B_n and a carry-in bit, C_{in} and operates with them in some predetermined way to output an n-bit function, F_n and a carry out bit C_{out}. Here, the term n-bit SLICE indicates a partition of identical n-bit modules of stages that can be cascaded in parallel. The choice of operation between the two operands A & B is determined by 'm' mode/ select inputs, M, S_{M-2},……..S_1,S_0 is as shown in Figure 1. The mode input M sets the ALU for either arithmetic or logic operation and the functions select inputs S_{M-}

${}_{2}\ldots S_1,S_0$ determine which particular operation within arithmetic or logic mode is to be performed. Just a carry out bit is required for cascading standard R-C units. For designing ALU, the first step is to list the operations to be performed. Hence we write the operation table (Table 1 and Table 2) for a simple 1-bit slice ALU.

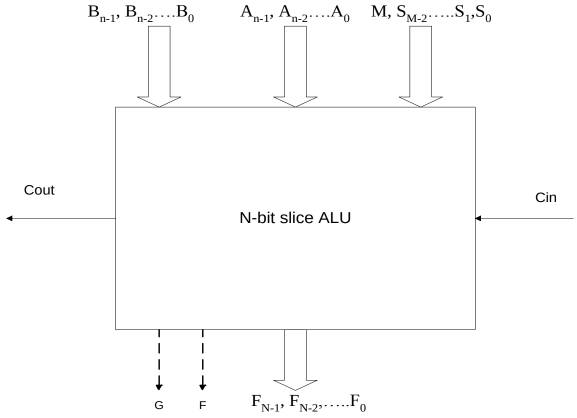

$B_{n-1}, B_{n-2}\ldots B_0$
$A_{n-1}, A_{n-2}\ldots A_0$
$M, S_{M-2}\ldots S_1,S_0$
Cout
Cin
N-bit slice ALU
G
F
$F_{N-1}, F_{N-2},\ldots F_0$

Figure 1: n-Bit Slice ALU

Table 1
Arithmetic Operations

M S1 S0	**F**	**Operation**		**C_{out}**
		C_{in}=0	**C_{in}=1**	
0 0 0	$A \oplus C_{in}$	Transfer A	Increment A	$A.\ C_{in}$
0 0 1	$\overline{A} \oplus C_{in}$	1's compliment of A	2's compliment of A	$\overline{A}\ .\ C_{in}$
0 1 0	$A \oplus B \oplus C_{in}$	A+B	A+B+1	$C_{in}\ (A \oplus B)+A.B$
0 1 1	$\overline{A} \oplus B \oplus C_{in}$	$\overline{A}$ +B	B-A	$C_{in}(\overline{A \oplus B})+\overline{A}.B$

Table 2
Logical Operations

M S1 S0	**F**	**Operation**	**C_{out}**
1 0 0	A	Transfer A	0
1 0 1	$\overline{A}$	Compliment A	0
1 1 0	A+B	A or B	0
1 1 1	$\overline{A}$ +B	$\overline{A}$ or B	0

2.2 CIRCUIT IMPLEMTATION OF LOW POWER HIGH PERFORMANCE 1 Bit ALU

The circuit implementation of high performance low power 1-Bit ALU is as shown in Figure 2. This 1-Bit circuit can be cascaded in parallel form to obtain 8-Bit ALU.

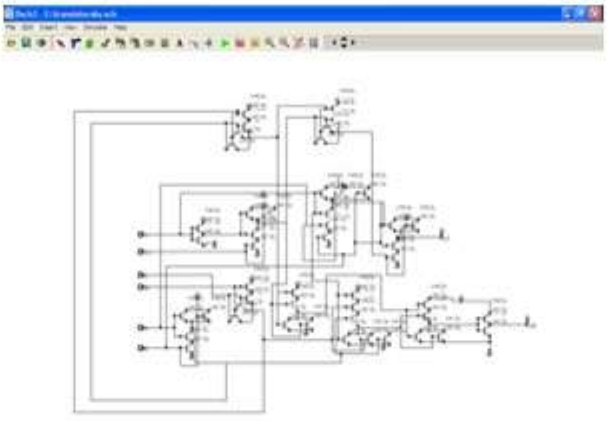


Figure 2: Circuit implementation of 1-Bit ALU

The MOS device used for designing the 1–Bit ALU are selected in such a manner that the power consumption of the whole circuit is less. Here low-leakage MOS devices are selected. Leakage current is the current that flows between the drain and source when the gate voltage is zero. Due to this leakage current the stand by current consumed by the processor is very high. Therefore, to avoid this stand by current, low leakage MOS devices are used. The ALU is also designed by choosing MOS devices that have a high threshold voltage. The Schematic view of the 8-Bit ALU is as shown in Figure 3 which is constructed by cascading 1 bit of ALU eight times.

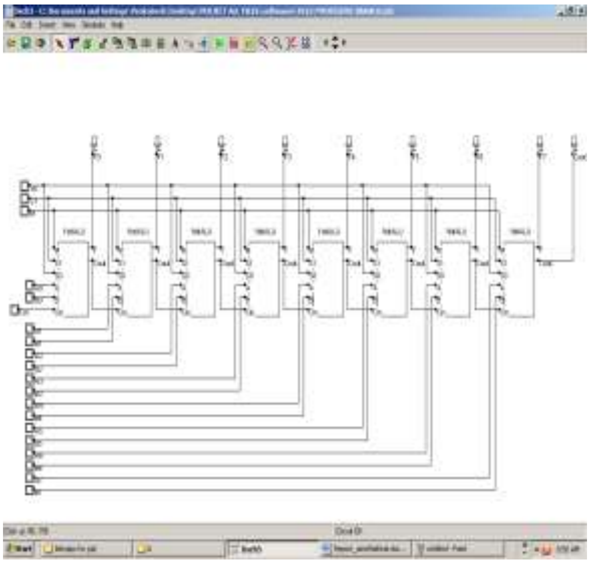


Figure 3: Schematic view of 8-Bit ALU

III. RESULTS And DISCUSSONS

In this section the physical implementation and simulation of the 1 Bit ALU/8 Bit ALU is shown. Analysis of global delay and analog simulation on the layout of the ALU is performed. Figure 4 shows the layout generated for 1-Bit ALU.

Delay calculation is performed of each interconnects in an ALU and the results are displayed in Figure 5. The navigator window represents each node in descending order of the delay and from the window it is clear that the worst case delay appears at node Y1, with a delay estimated to 0.412ns.

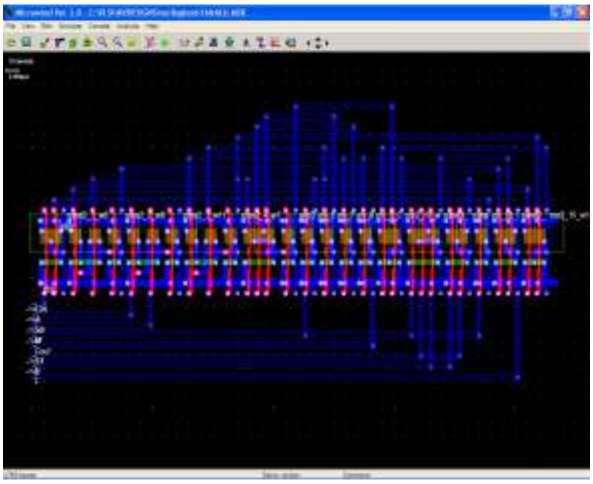
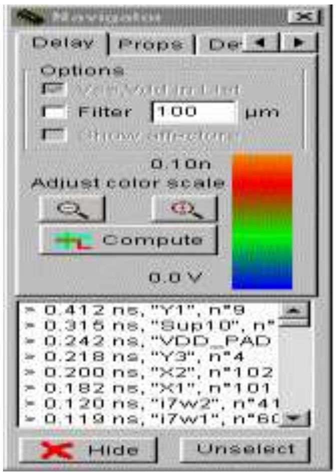


Figure 4: Layout of 1-Bit ALU



☐ Filter 100 µm

```
> 0.412 ns, "Y1", n°9
> 0.315 ns, "Sup10", n°
> 0.242 ns, "VDD_PAD
> 0.218 ns, "Y3", n°4
> 0.200 ns, "X2", n°102
> 0.182 ns, "X1", n°101
> 0.120 ns, "i7w2", n°41
> 0.119 ns, "i7w1", n°6(
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Figure 5: RC Delay Estimation at Chip Level

The leakage current is the current that flows between Drain and Source when no channel is present. No current is expected to flow between drain and source. However, a leakage current enables nA range current to flow although the gate voltage is 0.

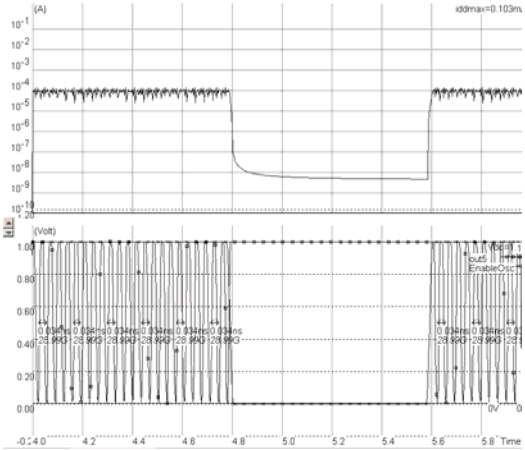

Figure 6: Low Leakage Mode

In the high speed mode, the circuit works fast (900 MHz) but consumes a significant standby current when off (around 200 nA). Once the option layer is set to “low leakage”, the simulation is performed again. The low- leakage mode show in Figure 6, features a little slower (100Mz that is approximately a 9 % speed reduction) and more than one decade less standby current when off (5 nA). In summary, low leakage MOS devices should be used as default devices whenever possible. High speed MOS should be used only when switching speed is critical. The analog simulation carried out on 1-bit ALU is shown in Figure 7.

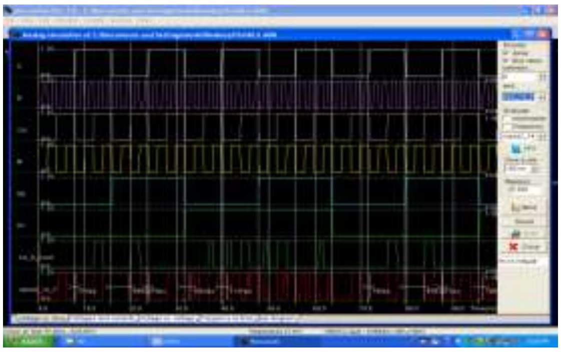

Figure 7: Analog simulation of 1-Bit ALU

The main objective of the low leakage MOS is to reduce the *Ioff* current significantly, that is the small current that flows between drain and source with a zero gate voltage. The price to pay is a reduced *Ion* current. The designer has the possibility to use high speed MOS devices, which have high *Ioff* leakages but large *Ion* drive currents. The size corresponds to the 0.12µm technology.

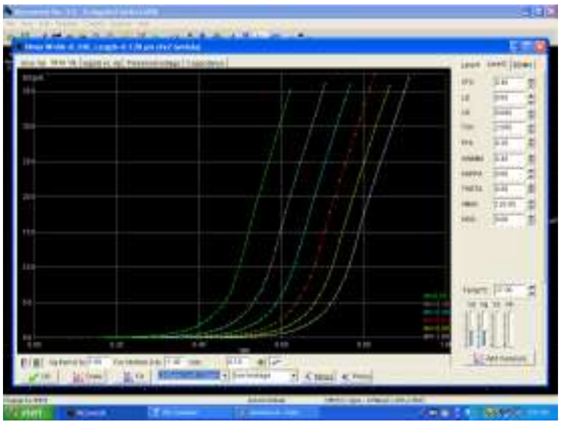

Figure 8: NMOS Device Characteristics

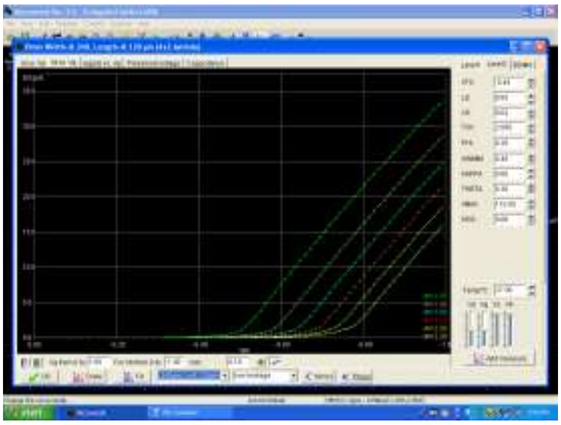

Figure 9: PMOS Device Characteristics

In Figure 8 and Figure 9, the characteristics of NMOS and PMOS is plotted. Both the low leakage MOS device has an negligible *Ioff* current. Thanks to a higher threshold voltage (0.4V rather than 0.3V) and larger effective channel length (120nm) compared to the high speed MOS. In the work, low leakage transistors are selected to encourage low power design. The *Ion* difference is around 33%. This means that a high speed MOS device is 33% faster than the low leakage MOS.

So, from the above analysis and results we can draw conclusion that a proper selection of transistors and designs move toward lower V_{DD} and lower V_{TH} reducing power dissipation. In this way it is evident from the above discussion that optimizing V_{DD} and V_{TH} is essential in low power, high speed designs.

The number of transistors for the design of 8- Bit ALU is 384. The maximum current drawn by the circuit during the operation is only 2mA, which can be seen from the Figure 10. The power dissipation calculated is only 0.0001mW while compared to Intel 8085 which dissipates power of 0.001mW.

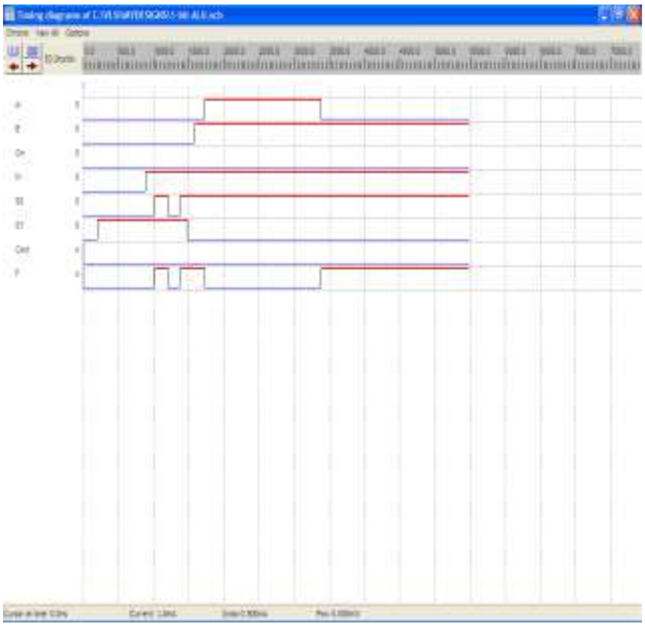

Figure 10: Simulation result of 1-Bit ALU

IV. Conclusions And Scope For Future Work

Design, analysis and simulation of an 8-bit ALU at gate and layout levels is presented. The ALU is designed for high performance and low power. The circuits are tested and simulated at transistor; gate and layout levels. The circuit is also tested by varying the threshold voltage. The ALU operates at a frequency range of 100MHz to 900MHz with a wide operating voltage of 1.2V to 5V. The technology employed is 120nm.

Leakage current can be reduced by adaptive body biasing and embedding dual threshold voltage in the proposed architecture. Power can be reduced by employing a technique of controlling threshold voltage through substrate bias.

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