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Design of Low Power Column bypass Multiplier using FPGA

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Abstract: It is well known that multipliers consume most of the power in DSP computations. Hence, it is very important for modern DSP systems to develop low-power multipliers to reduce the power dissipation.. In this paper, we presents low power Column bypass multiplier design methodology that inserts more number of zeros in the multiplicand thereby reducing the number of switching activities as well as power consumption. The switching activity of the component used in the design depends on the input bit coefficient. This means if the input bit coefficient is zero, corresponding row or column of adders need not be activated. If multiplicand contains more zeros, higher power reduction can be achieved. To reduce the switching activity is to shut down the idle part of the circuit, which is not in operating condition. Use of look up table is an added feature to this design. Further low power adder structure reduces the switching activity. Flexibility is another critical requirement that mandates the use of programmable components like FPGAs in such devices.
Keywords: Low Power, Multiplier, Reduced Switching,Column By passing

I. Introduction

As we get closer to the limits of scaling in Complementary metal. oxide. semiconductor (CMOS) circuits, power and heat dissipation issues are becoming more and more important. In recent years, the impact of pervasive computing and the internet have accelerated this trend. The applications for these domains are typically run on battery-powered embedded systems. The resultant constraints on the energy budget require design for power as well as design for performance at all layers of system design. Thus reducing power consumption is a key design goal for portable computing and communication devices that employ increasingly sophisticated and power hungry signal processing techniques. Flexibility is another critical requirement that mandates the use of programmable components like FPGAs in such devices.

The multiplication is an essential arithmetic operation for common DSP applications, such as filtering and fast Fourier Transform (FFT). To achieve high execution speed, parallel array multipliers are widely used. These multipliers tend to consume most of the power in DSP computations, and thus power-efficient multipliers are very important for the design of low-power DSP systems.

This paper presents a new multiplier design in which switching activities are reduced through architecture optimization. This paper is organized as follows. In the next section we give some preliminary information, including array multiplier architectures and previous works on low power multipliers. Our multiplier design is presented in Section 3, and some experimental results on the performance of various multipliers are shown in Section 4.

II. Preliminaries

A. Parallel Multiplier

Consider the multiplication of two unsigned n-bit numbers, where A = an–1an–2 …a0 is the multiplicand and B = bn–1bn–2 …b0 is the multiplier. The product P = p2n– 1, p2n–2 …p0 can be written as follows:

$$P=\sum_{i=0}^{n-1}\sum_{j=0}^{n-1}(a_i, bj)\,2^{i+j} \qquad (1)$$

A 4X4 unsigned multiplication example is shown in figure 1. The multiplicand Ai is added to the incoming partial product bit based on the value of the multiplier bit Bj. Each row adds the multiplicand to the incoming partial product, PPi to generate the outgoing partial product PP(i+1), if Yi =1. If Yi=0, PPi is passed vertically downward unchanged.

A - a3 a2 a1 a0

B - b3 b2 b1 b0

			a_3* b_0	a_2*b_0	a_1*b_0	a_0*b_0
		a_3* b_1	a_2 *b_1	a_1*b_1	a_0*b_1	
	a_3* b_2	a_2*b_2	a_1 *b_2	a_0*b_2		
a_3* b_3	a_2*b_3	a_1*b_3	a_0*b_3			

P_7 P_6 P_5 P_4 P_3 P_2 P_1 P_0

Figure 1. A 4×4 multiplication example

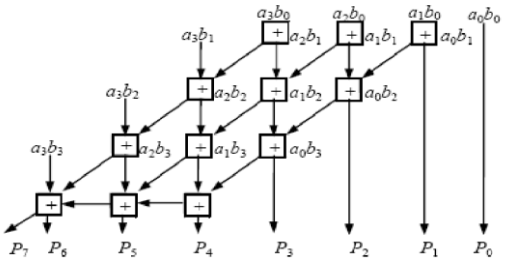


Figure 2. A 4×4 Braun multiplier.

An array implementation, known as the Braun multiplier , is shown in Figure 2. In the 4x4 Braun multiplier, the multiplier array consists of 3 rows of carry-save adders(CSAs), in which each row contains 3 full adders(FAs). Each FA has three inputs and two outputs: the sum bit and the carry bit. 3 FAs in the first CSA row that have only two valid inputs can be replaced by 3 half adders(HAs) and 3 FAs in the last row can be constructed as a 3-bit ripple-carry adder. On the other hand, the Baugh-Wooley multiplier uses the same array structure to handle 2's complement multiplication, with some of the partial products replaced by their complements. The multiplier array consists of (n–1) rows of carry-save adders (CSA), in which each rows contains (n–1) full adders (FA). The last row is a ripple adder for carry propagation. In this paper, we shall propose a low power design for this multiplier.

B. ***Related Research***

The power dissipation in CMOS circuit has several components that are usually estimated on the device parameters of the technology used. The total power in the circuit is given by the following equation,

Ptotal = Pswitching + Pshortcircuit + Pstatic +Pleakage (2)

where Pswitching is switching component of the power and it is a dominating component in these calculations. Pshortcircuit is the power dissipated due to the fact thatduring the circuit operation PMOS and NMOS transistors of CMOS gate become simultaneously during the transition at the input level, static consumption is from the leakage current For static power dissipation,the consumption is proportional to the number of the used transistors.

For dynamic power dissipation, the consumption is obtained from the charging and discharging of load capacitance. The average dynamic dissipation of a CMOS gate is given by equation 3.

$Pavg = 0.5 \times C_L \times VDD^2 \times fp \times N$ (3)

where CL is the load capacitance, fp is the clock frequency, VDD is the power supply voltage and N is the number of switching activity in a clock cycle.

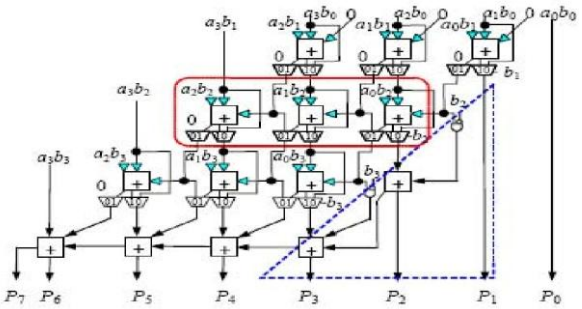


Figure 3. 4x4 Row bypassing Multiplier with reduced switching Activity

Thus, the power consumption can be reduced if one can reduce the switching activity of a given logic circuit without changing its function. An obvious method to reduce the switching activity is to shut down the idle part of the circuit, which is not in operating condition.

Figure 3 shows the 4 X 4 row bypassing architecture with reduced switching. The design included (n-1)(n-1) full adders, 2×(n-1)×(n-1) multiplexers, and 3×(n-1)×(n-1) three state gates.

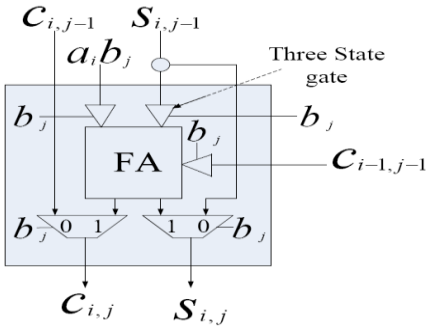


Figure 4. Row Bypassing Adder Cell (RA)

Figure 4 shows the Row Bypassing Adder Cell (RA) when the corresponding partial product is zero, the RA disabled unnecessary transitions and bypassed the inputs to outputs. The demerit of this technique is that it needs extra correction circuitry shown in triangle. Structure of the full adder is complex as well.

The Braun multiplier removes the extra correction circuitry needed. Also, number of adders is less. But, the limitation of this technique is that it cannot stop the switching activity even if the bit coefficient is zero that ultimately results in unnecessary power dissipation.

III. The Proposed Design

The switching activity of the component used in the design depends on the input bit coefficient. This means if the input bit coefficient is zero, corresponding row or column of adders need not be activated. If multiplicand contains more zeros, higher power reduction can be achieved.

Instead of bypassing rows of full adders, we propose a multiplier design in which columns of adders are bypassed. In this approach, the operations in a column can be disabled if the corresponding bit in the multiplicand is 0.

There are two advantages of this approach. First, it eliminates the extra correcting circuit as shown in Figure 3.Second, the modified FA is simpler than that used in the row-bypassing multiplier, as shown in Figure 7(a).Consider the multiplication shown in Figure 5, which executes 1010×1111. Note that, in the first and third diagonals (enclosed by dashed lines), two out of the three input bits are 0: the "carry" bit from its upper right FA, and the partial product aibj (note that a0 = a2 = 0).

As a result, the output carry bit of the FA is 0, and the output sum bit is simply equal to the third bit, which is the "sum" output of its upper FA. Now, consider another multiplication of 1111 x 1000. Since multiplicand contains no zero, all columns will get switched and consume more power. High power reduction

*A. **Basic Idea***

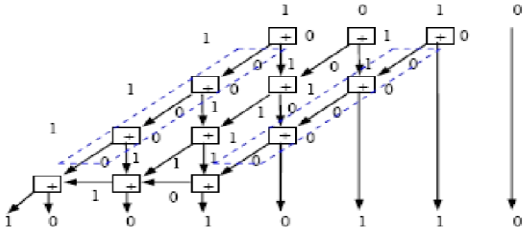


Figure 5. A column-bypassing example.

Can be achieved if the multiplicand contains more number of zeros than 1's.In this approach we propose Booth Recoding unit which will force multiplicand to have number of zeros,if does not have a single zero.The advantage here is that if multiplicand contains more successive number of ones then booth-recoding unit converts these ones in zeros.

B. Multiplier Design

The low power multiplier can be constructed as shown in figure 7. It is organized in three units as Detection of Zero Unit, Booth Recoding Unit and Multiplication Unit.

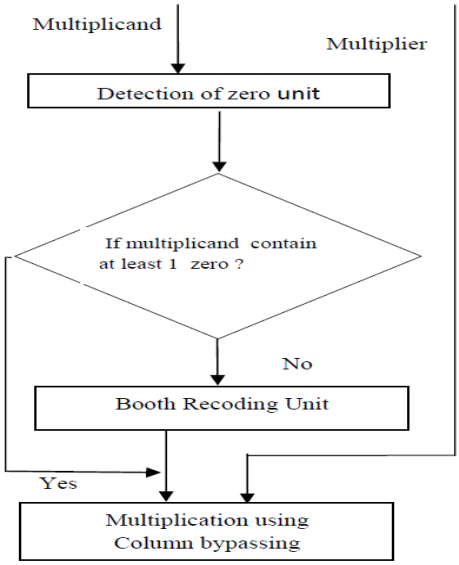


Figure 6. Proposed multiplier architecture

Detection of zero units:

This unit scan the number of zeros and their respective position in the multiplicand, so as to bypass the corresponding column. If multiplicand contain at least one zero then it will feed the column bypass multiplier and multiplication will be performed using column bypassing. If multiplicand does not contain zero, multiplicand will be given to the Booth Recoding Unit and after that multiplication will perform.

Booth Recoding Unit:

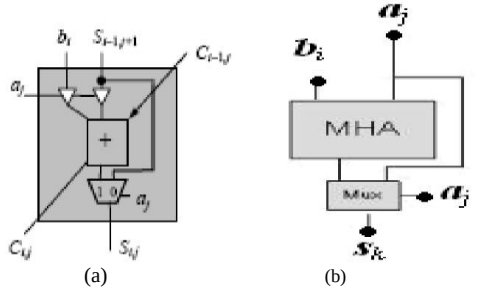
This unit chooses force the multiplicand to have greater number of zeros in case multiplicand does not have zero using Booth Table 1.

Table 1: - Booth Recoding Table

Multiplicand Bit i	Bit i-1	Version of multiplier selected by bit i
0	0	0 X M
0	1	+1 X M
1	0	-1 X M
1	1	0 X M

Column Bypassing Multiplier :

The column bypassing multiplier is constructed as follows. First, the modified HA cell is shown in Figure 7(b). Note that we only need two three-state gates and one multiplexor in this design. If aj = 0, the HA will be disabled. For a Braun multiplier, there are only two inputs for each FA in the first row (i.e., row 0). Therefore, when aj = 0, the two input of FA0,j are disabled, and thus it output carry bit will not be changed. Therefore, all three inputs of FA1,j are fixed, which prohibit its output from changing.



(a) (b)

Figure 7: (a) Modified FA cell for column bypassing multiplier.
(b) Modified HA cell for column bypassing multiplier.

The total number of full adders required to design column bypass multiplier are n*(n-2).The total number of half adders required to design column bypass multiplier are n.The total number of tristate buffers required to design column bypass multiplier are 2*n*(n-1).The total number of 2 TO 1 Multiplexers required to design column bypass multiplier are (n-1)*(n-1).

Figure 8 shows the 4×4 low power multiplier structure. This technique will be very useful as we go for higher width of the multiplicand specially when there are successive numbers of ones.if multiplicand contain at least one zero ,it does not uses the Booth recoding unit and if multiplicand is "11" then only it will use Booth recoding table shown in table 1.so we do not need sign bit circuitry.

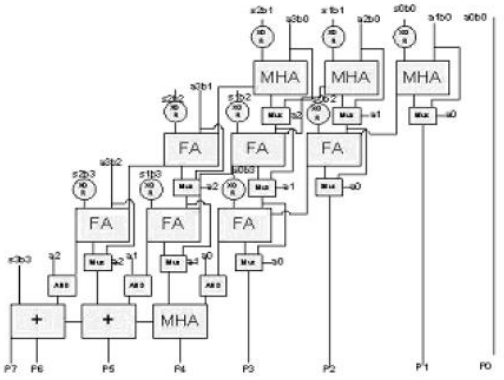


Figure 8. A 4×4 multiplier structure.

IV. Experimental Results

In order to evaluate the performance of 32-bit low power parallel multiplier, we implement all these designs on Spartan 3E FPGA. We compare the performance of this design with array multiplier and row bypassing multiplier. The design was synthesized on Xilinx 9.2i.Synthesized results on Xilinx XST are shown below in table 2 and 3 respectively. Simulation resultsfor the array multiplier are given in figure 9 and for proposed multiplier is given in figure 10.

Thus this method uses more number of slices compared to earlier methods. However, since number of logic elements available is large in most of the today.s FPGA this is not considered as a negative point, since power reduction is a prime goal. Theexperimental results show that the row-bypassing design and the array bypassing design actually consume more power due to the extra bypassing logic and our proposed design reduces the powerdissipation. Simulation results for the array multiplier and Row Bypassing multiplier are given in figure 9,10 and for proposed multiplier is given in figure 11.

Table 2:- Synthesis results on XPower Tool

Multiplier Type(32bit)	Array Multiplier	Row Bypass	Proposed
Vendor	Xilinx	Xilinx	Xilinx
Device and Family	Spartan 3E	Spartan 3E	Spartan 3E
Estimate Delay	87.636nsec	114.677nsec	80.870nsec
Total memory usage	299.736 MB	198.008MB	181.528MB
Power Dissipation	264 mW	184.77 mW	169.57mw

Table 3: - Synthesis results on Xilinx ST

Multiplier (32x32)	**Number of LUTs**
Without bypassing	2015
Row Bypassing	2960
Proposed	2014

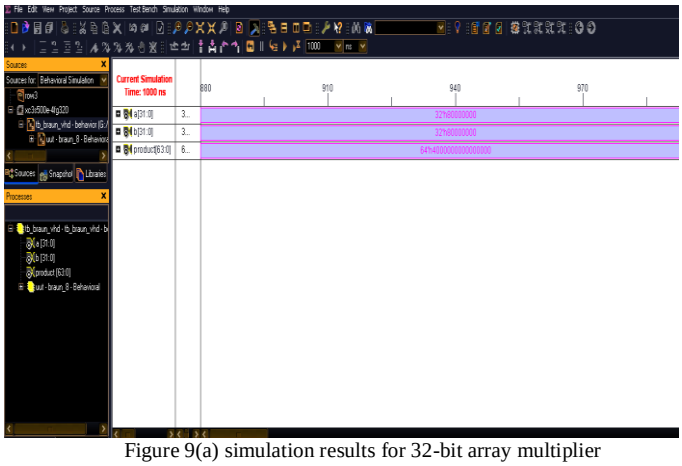


Figure 9(a) simulation results for 32-bit array multiplier

	Voltage (V	Current (m	Power (m
Quiescent		2.00	5.00
Total Pow			264.00
Startup Curr		0.00	
Battery Capacity (mA Hours)			0.00
Battery Life (Hours)			0.00

Figure 9(b) simulation results for 32-bit array multiplier

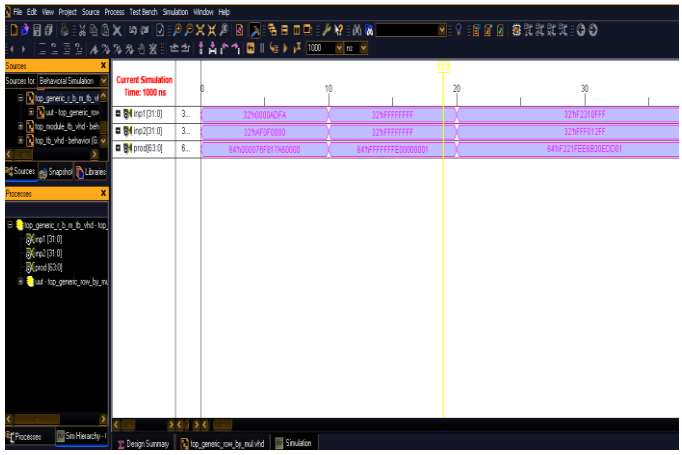


Figure 10(a) simulation results for 32-bit Row Bypassing multiplier

	Voltage (V)	Current (mA)	Power (mW)
Vccint	1.2		
Dynamic		17.60	21.12
Quiescent		26.91	32.29
Vccaux	2.5		
Dynamic		0.00	0.00
Quiescent		18.00	45.00
Vcco25	2.5		
Dynamic		32.54	81.36
Quiescent		2.00	5.00
Total Power			184.77
Startup Current (mA)		0.00	
Battery Capacity (mA Hours)			0.00
Battery Life (Hours)			0.00

Figure 10(b) simulation results for 32-bit Row Bypassing multiplier

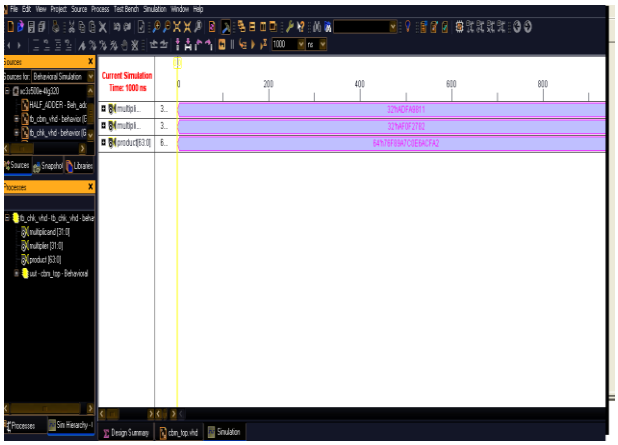


Figure 11(a) simulation results for 32-bit Column Bypassing multiplier

	Voltage (V	Current (m	Power (m
Quiescent		2.00	5.00
Total Pow			169.57
Startup Curr		0.00	
Battery Capacity (mA Hours)			0.00
Battery Life (Hours)			0.00

Figure 11(b) simulation results for 32-bit Column Bypassing multiplier

V. Conclusions

In this paper we have presented a new methodology for designing of low power parallel multiplier with reduced switching. Method for increasing number of zeros in the multiplicand is discussed with the help of Booth Recoding Unit. Based on the modification of the half adders instead of full adders in an array multiplier, a low-power design column bypassing using Booth recoding is proposed. Compared with the row bypassing or array-multipliers, the experimental results show that our proposed low-power multiplier achieves higher power reduction with lower hardware overhead.

VI. Future scope

The project can be implemented to 64 and 128 bit column bypassing multiplier. Less switching activity can be achieved in this multiplier. Low Power consumption can be achieved. In this multiplier, a low power multiplier design column bypassing using Booth recoding is proposed. Compared with other multipliers such as row bypassing array, the results achieve higher power reduction and hardware overhead.

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