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A Low Power Delay Buffer Using Gated Driver Tree

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Abstract : This project presents circuit design of a low-power delay buffer. The proposed delay buffer uses several new techniques to reduce its power consumption. Since delay buffers are accessed sequentially, it adopts a ring-counter addressing scheme. In the ring counter, double-edge-triggered (DET) flip-flops are utilized to reduce the operating frequency by half and the C-element gated-clock strategy is proposed. A novel gated-clock-driver tree is then applied to further reduce the activity along the clock distribution network. Moreover, the gated-driver-tree idea is also employed in the input and output ports of the memory block to decrease their loading, thus saving even more power.

The simplest way to implement a delay buffer is to use shift registers. If the buffer length N is and the word-length is b , then a total of Nb DFFs are required, and it can be quite large if a standard cell for DFF is used. In addition, this approach can consume huge amount of power since on the average Nb/2 binary signals make transitions in every clock cycle. As a result, this implementation is usually used in short delay buffers, where area and power are of less concern.

Although some power is indeed saved by gating the clock signal in inactive blocks, the extra R–S flip-flops still serve as loading of the clock signal and demand more than necessary clock power. We propose to replace the R–S flip-flop by a C-element and to use tree-structured clock drivers with gating so as to greatly reduce the loading on active clock drivers. Additionally, DET flip-flops are used to reduce the clock rate to half and thus also reduce the power consumption on the clock signal. The proposed ring counter with hierarchical clock gating and the control. Each block contains one C-element to control the delivery of the local clock signal "CLK" to the DET flip-flops, and only the "CKE signals along the path passing the global clock source to the local clock signal are active. The "gate" signal (CKE) can also be derived from the output of the DET flip-flops in the ring counter.

***Keywords* -** *C- element, delay buffer, first-in-first-out, gated clock, ring counter.*

I. INTRODUCTION

Portable multimedia and communication devices have experienced explosive growth recently. Longer battery life is one of the crucial factors in the wide spread success of these products. As such, low power circuit design for multimedia and wireless communication applications has become very important. In many such products, delay buffers (line buffers, delay lines) make up a significant portion of their circuits. Such serial access memory is needed in temporary storage of signals that are being processed, e.g., delay of one line of video signals, delay of signals within a fast Fourier transform (FFT) architectures and delay of signals in a delay correlate. Currently, most circuits adopt static random access memory (SRAM) plus some control/addressing logic to implement delay buffers. For smaller length delay buffers, shift register can be used instead. The former approach is convenient since SRAM compilers are readily available and they are optimized to generate memory modules with low power consumption and high operation speed with a compact cell size. The latter approach is also convenient since shift register can be easily synthesized, though it may consume much power due to unnecessary data movement. Previously, a simplified and thus lower-power sequential addressing scheme for SRAM application in delay buffers is proposed. A ring counter is used to point to the target words. Since the ring counter is made up of an array of D-type flip-flops (DFFs) triggered by a global clock signal. In this paper, we propose to use double-edge-triggered (DET) flip-flops instead of traditional DFFs in the ring counter to halve the operating clock frequency. A novel approach using the C-elements instead of the R–S flip-flops in the control logic for generating the clock-gating signals is adopted to avoid increasing the loading of the global clock signal. In addition to gating the clock signal going to the DET flip-flops in the ring counter, we also proposed to gate the drivers in the clock tree. The technique will greatly decrease the loading on distribution network of the clock signal for the ring counter and thus the overall power consumption. The same technique is applied to the input driver and output driver of the memory part in the delay buffer. In a delay buffer based on the SRAM cell array such as the one in, the read/write circuitry is through the bit lines that work as data buses. In the proposed new delay buffer, we use a tree hierarchy for the read/write circuitry of the memory module. For the write circuitry, in each level of the driver tree, only one driver along the path leading to the addressed memory word is activated. Similarly, a tree of multiplexers and gated drivers comprise the read circuitry for the proposed delay buffer. Simulation results show the effectiveness of the above techniques in power reduction.

II. CONVENTIONAL DELAY BUFFERS

The simplest way to implement a delay buffer is to use shift registers as shown in Fig. 1. If the buffer length is and the word-length is, then a total of DFFs are required, and it can be quite large if a standard cell for DFF is used. In addition, this approach can consume huge amount of power since on the average binary signals make transitions in every clock cycle. As a result, this implementation is usually used in short delay buffers, where area and power are of less concern. RAM-based delay buffers are more popular in long delay buffers because of the compact SRAM cell size and small total area. Also, the power consumption is much less than shift registers because only two words are accessed in each clock cycle: one for write-in and the other for read-out.A binary counter can be used for address generation since the memory words are accessed sequentially. The SRAM-based delay buffers do away with many data transitions, there still can be considerable power consumption. in the SRAM address decoder and the read/write circuits. In fact, since the memory words are accessed sequentially, we can use a ring counter with only one rotating active cell to point to the words for write-in and read-out. This method, known as the pointer-based scheme.This type flip-flops is initialized with only one“1” (the active cell) and all the other DFFs are kept at “0.” When a clock edge triggers the DFFs, this “1” signal is propagated forward. Consequently, the traditional binary address decoder can be replaced by this “unary-coded” ring counter. Compared to the shift register delay buffers, this approach propagates only one “1” in the ring counter instead of propagating-bit words. Obviously, with much less data transitions, the pointer-based delay buffers can save a lot of power.

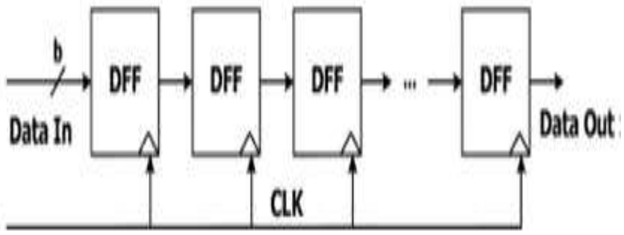


Figure 1 Delay Buffer implemented by Shift Register

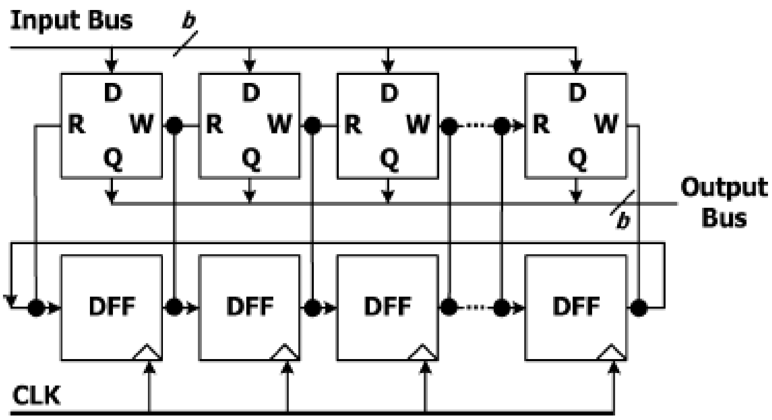


Figure 2 Pointer based Scheme

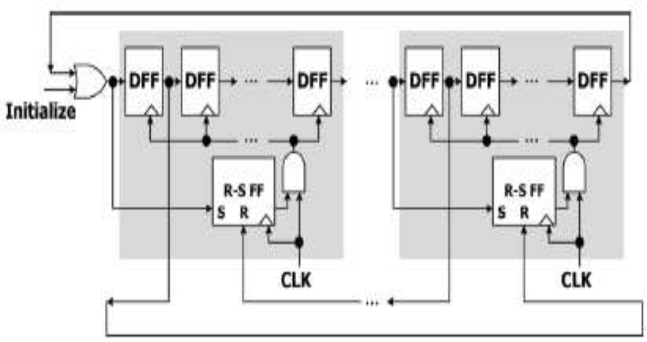


Figure 3 Ring counter with RS flip-flop

By observing the fact that only one of the DFFs in the ring counter is activated, the gated-clock technique has then been proposed to be applied to the DFFs. In their approach, every eight DFFs in the ring counter are grouped into one block. Then, a "gate" signal is computed for each block to gate the frequently toggled clock signal when the block can be inactive so that unnecessary power wasted in clock signal transitions is saved.

III. PROPOSED DELAY BUFFER

In the proposed delay buffer, several power reduction techniques are adopted. Mainly, these circuit techniques are designed with a view to decreasing the loading on high fan-out nets, e.g., clock and read/write ports.

A Gated-clock ring counter Although some power is indeed saved by gating the clock signal in inactive blocks, the extra R–S flip-flops still serve as loading of the clock signal and demand more than necessary clock power. We propose to replace the R–S flip flop by a C-element and to use tree-structured clock drivers with gating so as to greatly reduce the loading on active clock drivers. Additionally, DET flip-flops are used to reduce the clock rate to half and thus also reduce the power consumption on the clock signal.

The proposed ring counter with hierarchical clock is shown in figure. Each block contains one C-element to control the delivery of the local clock signal "CLK to the DET flip-flops, and only the "CKE signals along the path passing the global clock source to the local clock signal are active. The "gate" signal (CKE) can also be derived from the output of the DET flip-flops in the ring counter. The C-element is an essential element in asynchronous circuits for handshaking. The logic of the C-element is given by

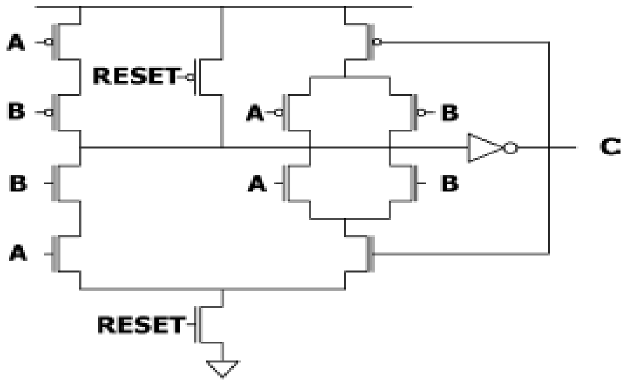


Figure 4 Logic Circuit of C-element

where A as well B are its two inputs and C+ as well as C are the next and current outputs. If A=B, then the next output will be the same as . Otherwise ,A#B and C+ remain unchanged. Since the output of C-element can only be changed when A=B , it can avoid the possibility of glitches, a crucial property for a clock gating signal. In order to reduce more power, we replace DFFs by double-edge-triggered flip-flops and operate the ring counter at half speed . With such changes, the clock gating control mechanism is different.

When the input of the last DET flip-flop in the previous block changes to "1" making both two inputs of the C-element the same, the clock signal in the current block will be turned on. When the output of the first DET flip-flop in the current block is asserted, then both inputs of the C-element in the previous block go to "0" and the clock for the previous block is disabled. In order to further diminish the loading on the global clock signal ("CLK"), we propose to use a driver tree distribution network for the global clock and activate only those drivers.

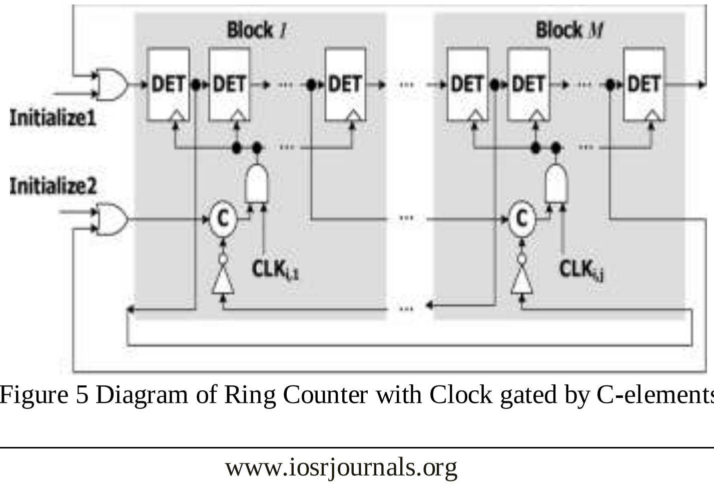
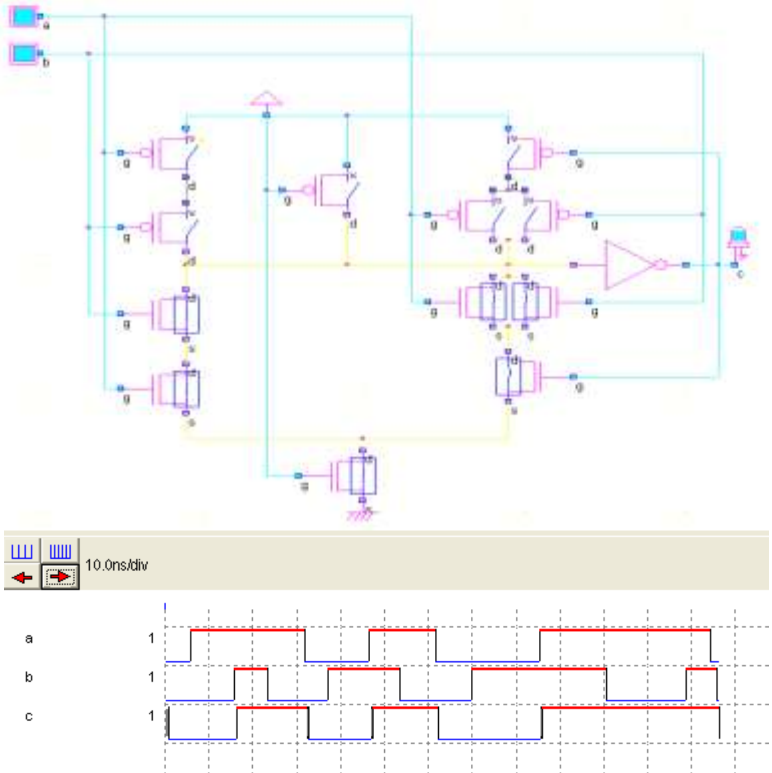


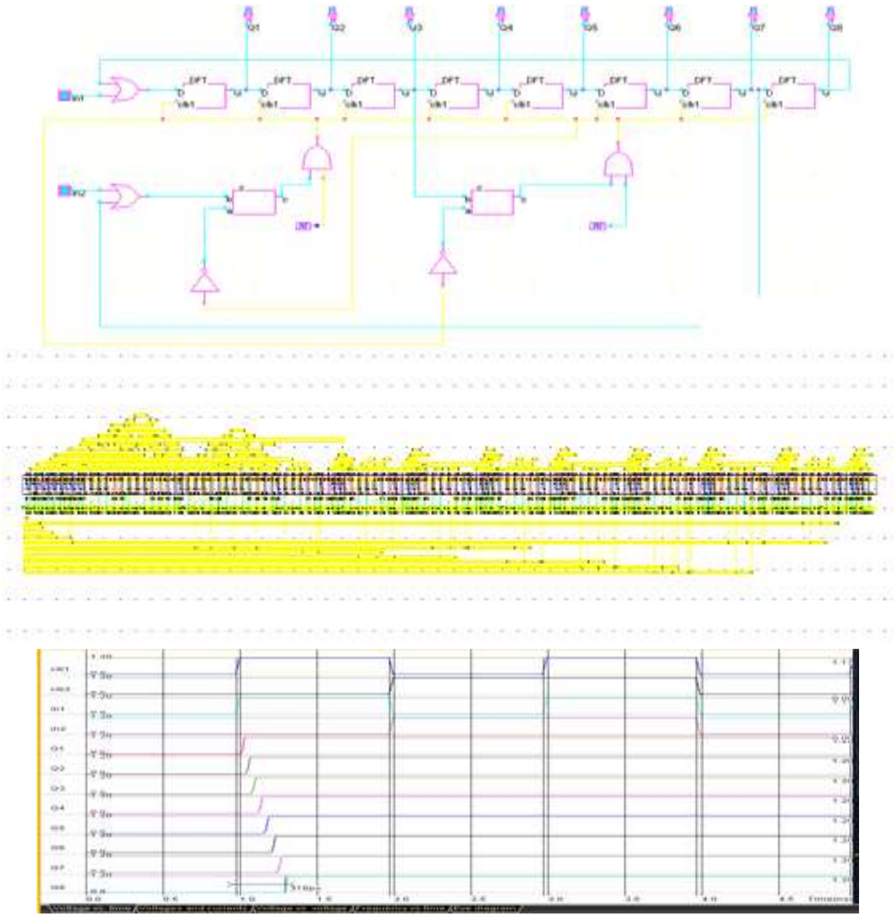
Figure 5 Diagram of Ring Counter with Clock gated by C-elements

IV. SIMULATION RESULTS

➢ Circuit Design and Simulation of C- Element



➢ Design and Simulation of Proposed Ring Counter of Double edge triggered Flip Flop with Clock Gated by C-Elements



V. ANALYSIS OF GATED DRIVER TREE USING D AND DET FLIP FLOP

Ring counter Structure (N=512,D=8,M=64)	Estimated Loading ratio by equations (3)-(5)
Traditional Ring Counter	1024
Gated clock ring counter with RS Flip Flop	208
Proposed Gated clock ring counter	31

Table 1 Estimated Loading Ratio of three different Ring Counters

Proposed Ring counter Structure Clock gated with C-element	Simulated Power @ 0.12um
Double Edge Triggered Flip flop	1.948mw
Pulse Triggered Flip Flop	0.767mw
Improved Pulse Triggered Flip Flop	0.582mw

Table 2 Comparison of Power by using different D Flip Flops in Delay Buffer Ring Counter

Input Driver Tree Structure (N=512,M=64,D=8)	Simulated Power @ 1.8v,50MHz,0.18µm	Estimated Loading Ratio by Eqs. (6)-(7)
Without Gated Driver Tree	520µW	512
With Gated Driver Tree	44.2µW	44

Table 3 Power of the Input Driver Tree with and Without the Gating Strategy

VI. Conclusion

In this project, we presented a low-power delay buffer architecture which adopts several novel techniques to reduce power consumption. The ring counter with clock gated by the C-elements can effectively eliminate the excessive data transition without increasing loading on the global clock signal. The gated-driver tree technique used for the clock distribution networks can eliminate the power wasted on drivers that need not be activated. Another gated-de multiplexer tree and a gated-multiplexer tree are used for the input and output driving circuitry to decrease the loading of the input and output data bus. All gating signals are easily generated by a C-element taking inputs from some DET flip-flop outputs of the ring counter.

We believe that with more experienced layout techniques the cell size of the proposed delay buffer can be further reduced, making it very useful in all kinds of multimedia/communication signal processing ICs.

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