IOSR Journal of VLSI and Signal Processing (IOSR-JVSP)
ISSN: 2319 – 4200, ISBN No. : 2319 – 4197 Volume 1, Issue 4 (Nov. - Dec. 2012), PP 42-46
www.iosrjournals.org

A Low Power, 8-Bit, 5MS/s Digital to Analog Converter for Successive Approximation ADC

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Abstract: *In this paper, a simple switched capacitor Digital to Analog Converter (DAC) is presented that exhibits monotonicity and occupies small area. The proposed DAC starts its conversion from the MSB instead of the traditional approach of starting from LSB making it suitable for use in cyclic or successive approximation analog-to-digital converters. The reference voltage is sampled once and appropriate charge is transferred to the output capacitor of the DAC. Some issues relevant to the design and their possible solutions are presented. The DAC is designed for a resolution of 8-bit. Sampling speed is chosen to be 5MS/s and the main emphasis is on low power. This DAC consumes power in the order of microwatt (μW), compare with previous DACs which consumes more power, generally in the order of milliwatts. The output 8-bits along with power dissipation of 493.8 μW has been achieved.*

Index Terms*—DAC, Folded Cascode, SAR ADC, Transmission gates.*

I. Introduction

Most of real world signals are continuous in time and value called analog signals. But, compared to analog signals, digital signals have many advantages. So, there is a flow to transfer signal processing from the analog domain to the digital one like digital signal processing, which not only allows for a higher level of accuracy but also provides savings in power consumption and silicon area. It increases robustness in the circuit, speeds up the design process, brings flexibility and programmability, and increases the number of chances for design reuse. Because of above benefits of working in digital domain, there is a need to convert the analog real world signals to digital discrete-time and discrete-value signals. DSP processors process digital signals, hence analog to digital converters (ADC) are required to convert the analog signals to digital signals. After processing of signals, the output needs to be converted back to its analog form, hence DAC is used. Here DAC is designed for Successive Approximation ADC which may be further used for bio-medical and video applications.

II. Background

Digital to analog converters operating at moderate speeds and their moderate resolutions are used in many applications. These DACs often consume low power. The classical DAC using two capacitors was proposed in [2] and is shown in Figure 1. The DAC starts its conversion from the LSB. This DAC can be used as a sub-DAC in an ADC, but the ADC will then required to convert the input completely before the LSB becomes available at DAC for processing. This usually slows down the operation of the ADC considerably.

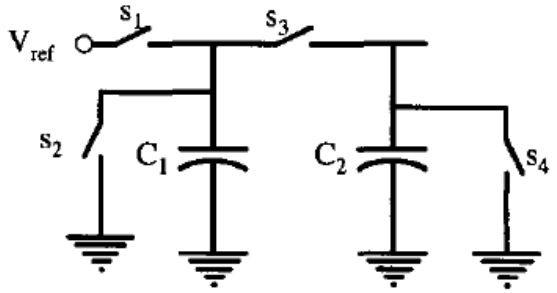


Figure 1: Conventional method of DAC implementation

So, a new method of designing DAC is proposed as shown in Figure 2. This low power 5MS/s switched capacitor DAC has been designed in 0.18μm CMOS n-well process. The resolution of DAC is taken to be 8-bit. Its practical implementation is shown in Figure 3.

III. Operation Of Dac

C_1 and C_2 are chosen to have the same size. φ_1 and φ_2 are non-overlapping clocks and get enabled only when φ_{start} is low. The conversion process begins with φ_{start} going high. This causes the capacitor C_1 to get charged

to the reference voltage,V_{ref}. Once φ_{start} goes low, φ_1 and φ_2 get enabled. Firstly, φ_1 turns on which results in charge sharing between C_1 and C_2 and hence C_2 gets charged to $\frac{V_{ref}}{2}$.

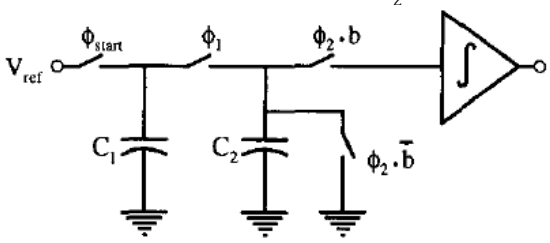


Figure 2: Proposed DAC structure

The incoming data stream is fed to the DAC with MSB facing first. If the current bit, d, is a 1, the charge which is hold by C_2 is transferred to the integrator. If the bit d is 0, then the capacitor C_2 is discharged to ground. This process continues until the LSB is reached. In each and every cycle, charge is transferred in quantities from the "master" capacitor C_1 to C_2 and hence either integrated with output or discarded to ground in exact correspondence with the bit under conversion. For an N-bit DAC, number of clock cycles required are N to finish the conversion, hence is widely used as an important component in Successive Approximation ADC. At the end of N cycles, the output is available at the output of op amp. All the switches are implemented by using transmission gate.

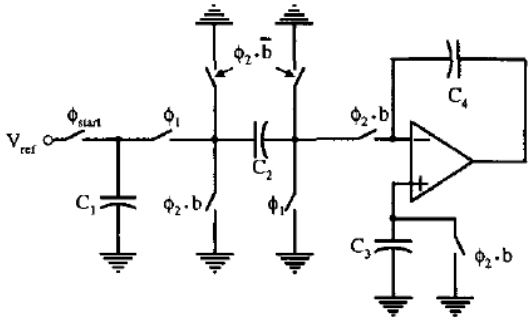


Figure 3: Practical implementation of DAC

IV. Dac Design Specifications

Table 1: Various design parameters of DAC

Parameters	**Values**
Technology	**Cadence UMC_180nm Technology**
Supply voltage	**1.8V**
Power	**< 500µW**
Resolution	**8-bits**
Sampling speed	**5MS/s**

V. Op-Amp For Dac

Out of various op amp architectures folded cascode op amp is best suited for switched capacitor applications. So, folded cascode op amp is designed keeping in view the total power consumption of DAC is less than 500µW. This power is distributed between op amp and switches, since folded cascode consume more power than the other op amp configurations, hence power budget is divided as 400 µW plus 100 µW.

Circuit diagram of folded cascode op amp is shown in Figure 4. With the given power constraint of op amp, the typical corner analysis of op amp gives power consumption of 306.5 µW. The op amp is made to run at all process corners. Gain and phase plot of op amp is shown in Figure 5 and Figure 6 respectively. The designed op amp meets all the desired specifications. Since resolution of DAC is 8-bit, hence the op amp should have minimum gain of 54.18 dB. Theoretical gain of folded cascode op amp is given by:

$|A_v| \approx \{[(g_{m1} + g_{mb3})r_{o3}(r_{o1} \parallel r_{o5})] \parallel [(g_{m7} + g_{mb7})r_{o7}r_{o9}]\}$.

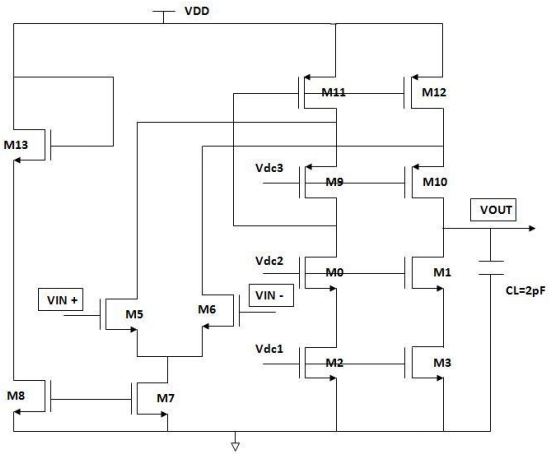


Figure 4: Folded Cascode op amp.

Designed op amp provides gain and phase of 62.61 dB and 82.7° respectively.

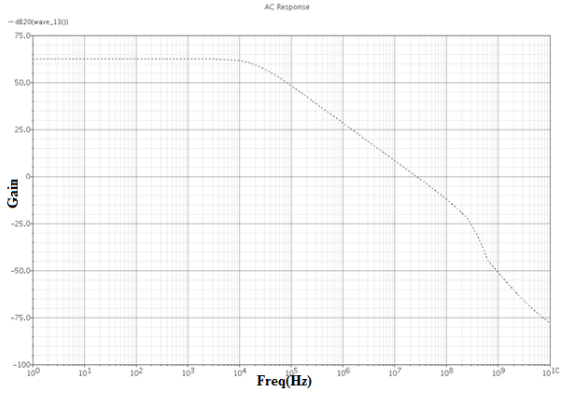


Figure 5: Gain plot of op amp.

VI. Switch For Dac

Given DAC uses transmission gate as a switch. The sampling speed of DAC is given by two factors: the on-resistance of the switch and the value of the sampling capacitor.

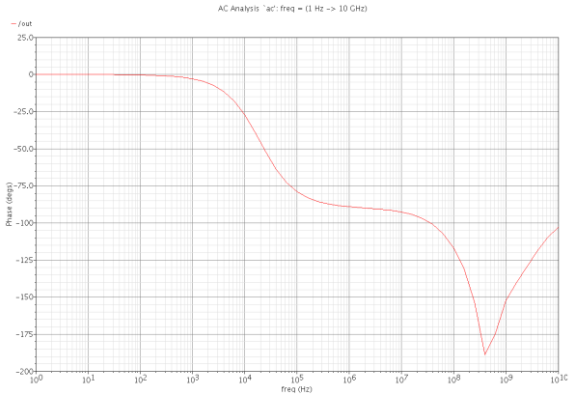


Figure 6: Phase plot of op amp.

Thus, to achieve a high speed, a switch with large aspect ratio and a small capacitor must be used. The value of R_{on} i.e. the on-resistance is given by

$R_{on} = \mu_n C_{ox} \frac{W}{L}(V_{DD} - V_{TH})^{-1}$. Plots of on-resistance of NMOS and PMOS device as a function of input voltage is shown in Figure 7.

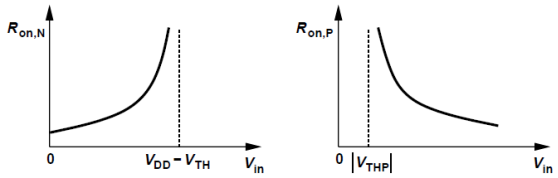
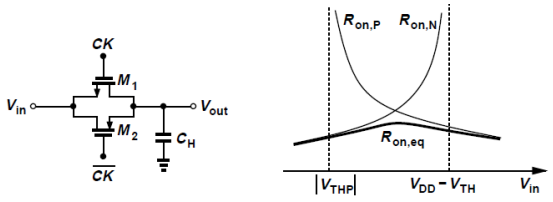


Figure. 7: On-resistance of (a) NMOS and (b) PMOS devices as a function of input voltage

In order to accommodate greater voltage swings in a sampling circuit, it is observed that a PMOS switch exhibits an on-resistance that decreases as the input voltage becomes more positive [Figure 7(b)]. It is then possible to employ "complementary" switches so as to allow rail-to-tail swings. Circuit implementation of transmission gate is shown in Figure 8.

VII. Switch Designing

The product of the ON-resistance and the capacitive load of the transistor determine the bandwidth. Using, the sampling frequency to be 5Ms/s, the values of R and C can be calculated and hence, the aspect ratio of MOSFET.



(a) (b)

Figure 8: (a) Complementary switch, (b) on-resistance of complementary switch.

Transmission gates are used as a switch which encounters two main problems: clock feed-through and charge injection. These problems are reduced to minimum by replacing capacitor C_1 in Figure 2 by the circuit shown in Figure 9. Now during φ_{start} the reference voltage V_{ref} is sampled as before. Again, the circuit looks the same during phase φ_1. However, in phase φ_2 at which the voltage on C_2 is being processed, the master capacitor C_1 is placed in the feedback loop of an op amp which forces the voltage across C_1 to remain constant and maintain its level. Any perturbations due to charge injection or charge loss from C_1 are compensated by the op amp. As a result of this, the charge corresponding to the reference voltage sampled across C_1 at the beginning of the conversion process can be hold more accurately. Output of DAC using this proposed method for reducing charge leakage is shown in Figure 10. The DAC is designed for low power consumption. Present work on DAC consumes the power in the order of milli-watts, but this DAC consumes very low power of 493.8 µW.

VIII. Performance Comparison

Table 2: Various performance parameters

	[6]	[7]	[8]	[9]	This work
Technology	0.35 μm	0.5 μm	0.35 μm	0.35 μm	0.18 μm
Resolution	10	10	10	14	8
Conversion speed	200 MS/s	400MS/s	25MS/s	5MS/s	5MS/s
Input range	-	0.5 V_{pp}	-	-	0.6-1.3
Supply voltage	3V	3.3V	3V	3V	1.8V
Power consumption	61mW	90mW	-	7mW	493.8 μW
Gain	65dB	-	-	90dB	62.61dB
Load capacitance	50pF	0.5pF	3.2pF	-	2pF

IX. Conclusion

The DAC is designed for resolution of 8-bit.

Sampling speed is taken to be 5MS/s and power dissipation achieved is 493.8 µW. The output of DAC converges to the final value without decreasing from its previous analog value. Simulation results shows that DAC dissipates power of 493.8 µW and output of DAC increases for input'1'. The conversion starts from MSB and the output voltage is obtained using a switched capacitor integrator.

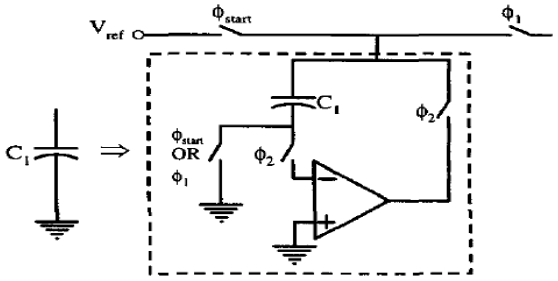


Figure 9: Proposed circuit for reducing charge leakage.

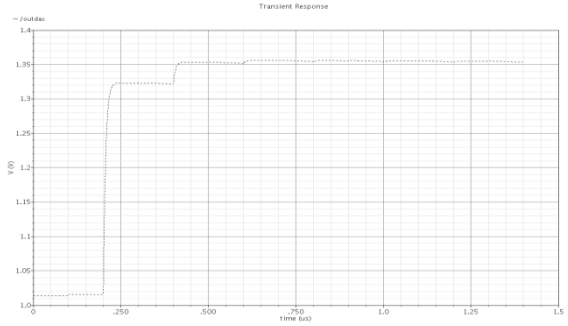


Figure 10: DAC output for all bits '1'.

Few of design issues that limit its performance have been discussed. Although no concern on linearity is specifically addressed, various techniques can be used for its improvement also. Such enhancements as well as the design of the improved DAC can be included in the future work. Since the designed DAC failed at SF corner and FS corner because the output of DAC decreases even for "1" input. This problem may be due to charge leakage through capacitor C_1 , hence improved charge storage circuit need to be designed to extend this work in future.

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