IOSR Journal of VLSI and Signal Processing (IOSR-JVSP)
Volume 10, Issue 3, Ser. I (May - June. 2020), PP 17-21
e-ISSN: 2319 – 4200, p-ISSN No. : 2319 – 4197
www.iosrjournals.org

An EDSP Estimation And Recalibration In FPGA Using Systematic Sampling

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Abstract: *In electronic applications, a synchronous relationship between the signals needs to be preserved for that phase measurement is required. In a Traditional electronic systems, the time measurement system is designed by using classical mixed signal approach. But it causes uncertainty in phase relationship between the recovered signals. To avoid this uncertainty, minute phase shift change register and phase measurement logic core is designed inside an FPGA with high resolution and precision in the range of few Pico seconds. The working principle present in the proposed system is systematic sampling, here subsamples are accumulated over the phase detector signal. The newly designed logic core can operate over a wide range of digital clock frequencies, ranging from a few kilohertz to the maximum frequency that is supported within the FPGA fabric. The Proposed System Implemented using Verilog HDL and Simulated by Model sim6.4 c and Synthesized by Xilinx tool. The proposed system implemented in FPGA Spartan 3 XC3S 200 TQ-144.*

Index Terms: *Field-programmable gate array (FPGA), jitter, phase calculator, phase polarity, subsampling, successive approximation, synchronization, systematic sampling, VLSI, XOR-based phase detector.*

I. Introduction

In recent trend for compact implementation of full digital architectures, reconfigurable hardware technologies such as field-programmable gate arrays (FPGAs) play a very dominant role. Popular latency critical communication link standards used in High Energy Physics experiments such as gigabit transceiver and timing-trigger and control system over passive optical network technology are implemented in FPGAs directly. These links carry trigger and timing information needed for timestamp generation and event building. It is essential that the latency critical protocols maintain constant phase differences in the recovered signals for the entire experiment's runtime.

High-speed serial transceivers of FPGA's do not maintain constant phase shift with each round of power cycle, reset cycle, loss of lock in the transceiver, firmware upgrade, or aging of clock circuitry in phase-locked loop (PLL). A logic design for phase monitoring capability to register phase shift changes in the range of 20–100ps is needed inside the FPGA circuitry. This would allow to extract the relative phase information and to recalibrate the system when needed, to maintain the constant phase relationships.

Several approaches for phase measurement have been discussed in the literature. The classical principle of using the over sampling technique is inadequate to measure a relative phase difference between the two high-frequency clocks inside an FPGA fabric, whose frequency exceeds the maximum limit supported by the fabric (<500 MHz). One of the solutions as mentioned in the works. This to sample it externally using an analog-to-digital converter (ADC) and then feed it back to the FPGA for computation. However, the technique needs an additional hardware to measure the phase difference of the internal digital clocks. Without the use of additional hardware, a phase measurement approach had been proposed using the dynamic phase alignment (DPA) features of the FPGA PLLs. The drawback of the method is the achieved resolution, which is limited to the 1/8th of the voltage controlled oscillator (VCO) frequency.

An accurate phase measurement in an FPGA using subsamples collected by the systematic sampling over XOR-based phase detector (PD) signal. The XOR-based PD introduces the least timing jitter because of the simplicity of its design. It is known that use of sub sampling technique causes spectral leakage. However, the use of averaging method for the phase measurement makes it less susceptible to interfere with the results. The proposed technique is suitable to construct a logic core for relative phase measurement between clocks having very low to very high frequencies with precision, accuracy, and resolution in the range of a few picoseconds.

In FPGA based phase detector [1] does not require any internal or external special components. It can be used on high speed clocks. Additional independent clock is used to scan the high speed clocks. It ensure good performance with high accuracy and have simplicity in its design.

In space borne systems [2] the important diagnostic information are provided by on-board rapid calculation of input signal phase differences. The high performance adaptive hardware provide an opportunity to efficiently evaluate signal phase and quickly identify phase drift.

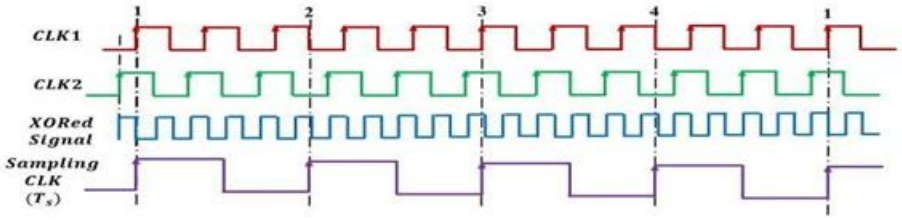

Fig. 1. Scanning of the XORed waveform using the sampling clock is illustrated for *Fs / F* = 4/10 or / = 2/5.

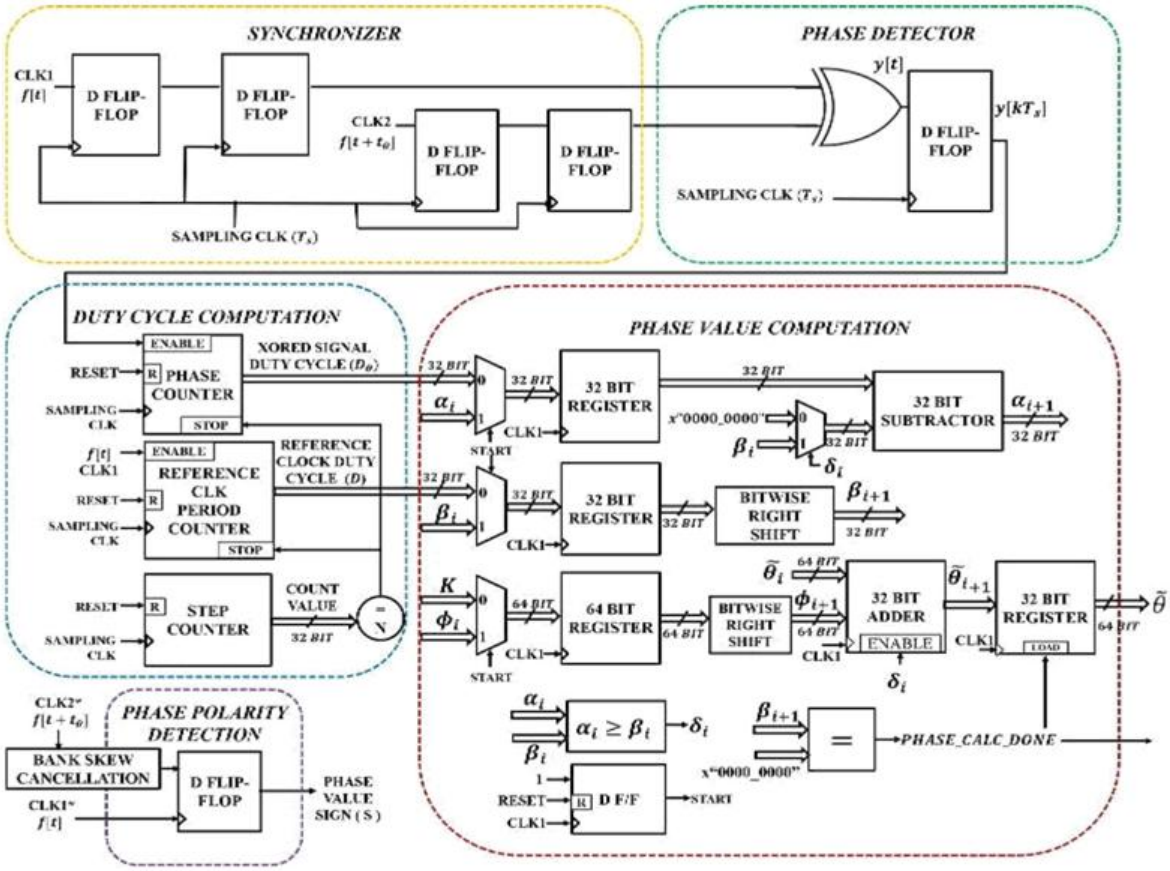

Fig.2 VLSI Architecture

II. Sampling Methodology

Commonly used stratified or random sampling for signal processing holds no synchronous relationship between the sampling clock and the reference clock used to drive the logic signal. In this paper, we have used the concept of systematic sampling method to sample the phase information signal or the XORed signal. The necessary condition for having systematic sampling is to maintain a synchronous relationship between the sampling clock (SAMPLE CLK) and the reference clock (CLK1). Since we are systematically registering only a part of the possible sample set, we refer to the collected samples as "subsamples." This systematic sampling approach is illustrated in Fig. 1. Here, the progression through the subsamples is cyclic, which means that the subsample starts repeating itself after every th element in the selected sample frame. The cyclic vector of subsamples **S** of order is represented as $\mathbf{S} = \{s^0, s^1, s^2, \ldots, s^{-1}\}$, then the relationship between $s = s^0$ holds. **S** forms a subset of the selected sampling frame or the sample population vector **P** of size *N*. To denote this mathematically, $\mathbf{S} \subset \mathbf{P}$ where $< N$. From the isometric property of systematic sampling on the XORed signal, the generated sample population vector (**P**) constitutes multiple sets of the cyclic vector of subsamples, **S**, that repeats itself and are isomorphic to one another.

III. FPGA Phase Measurement

General:

The notion of "phase" is usually associated with periodic or repeating signals. With these signals, the wave shape perfectly repeats itself every time the period of repetition elapses. For periodic signals one can think of the phase at a given time as the fractional portion of the period that has been completed. This is commonly expressed in degrees or radians, with full cycle completion corresponding to 360° or 2π radians. Thus, when the cycle is just beginning, the phase is zero. When the cycle is half completed, the phase is half of 360°, or 180°. It is important to note that if phase is defined as the portion of a cycle that is completed, the phase depends on where the beginning of the cycle is taken to be. There is no universal agreement on how to specify this beginning. For a sinusoidal signal, probably the two most common assumptions are that the start of the cycle is (1) the point at which the maximum value is achieved, and (2) the point at which the negative to positive zero-crossing occurs.

Assumption:

(1) Many theoretical treatments of phase, and for that reason is adopted in this chapter. It should be noted, however, that assumption (2) has some benefits from a measurement perspective, because the zero-crossing position is easier to measure +than the maximum.

(2) The measurement of phase is important in almost all applications where sinusoids proliferate. Many means have therefore been devised for this measurement. One of the most obvious measurement techniques is to directly measure the fractional part of the period that has been completed on a cathode-ray oscilloscope (CRO). Another approach, which is particularly useful when a significant amount of noise is present, is to take the Fourier transform of the signal. According to Fourier theory, for a sinusoidal signal, the energy in the Fourier transform is concentrated at the frequency of the signal; the initial phase of the signal (i.e., the phase at time, t = 0) is the phase of the Fourier transform at the point of this energy concentration. The measurements of initial phase and frequency obtained from the Fourier transform can then be used to deduce the phase of the signal for any value of time.

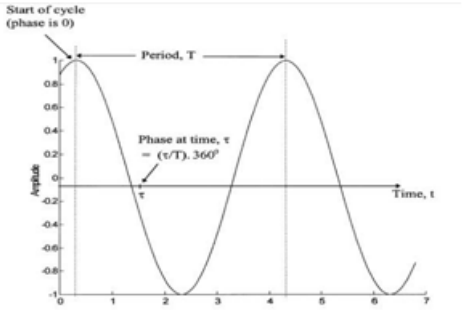

Fig.3 The phase of a periodic sinusoidal signal.

Frequently what is needed in practice is a measurement of the phase difference between two signals of the same frequency; that is, it is necessary to measure the relative phase between two signals rather than the absolute phase of either one. Often, in the measurement of the relative phase between two signals, both signals are derived from the same source. These signals might, for example, be the current and voltage of a power system; the relative phase, φ, between the current and voltage would then be useful for monitoring power usage, since the latter is proportional to the cosine of φ.

IV. Generating Subsamples

During systematic sampling, there are two main methods through which one can produce more subsamples to increase the resolution of the phase measurement. These two methods are discussed in the following sections.

A. Method of Cascaded PLL

When the multiplication factor exceeds the VCO maximum output frequency capability in PLL circuitry, then the PLL frequency synthesizer fails. In that scenario, PLL-to-PLL cascading is needed. Here, we can split the multiplication factor ( ) between the two PLLs. The cascaded PLL having the same bandwidth settings has jitter amplification effect [13]. To minimize jitter effect, Altera (now part of Intel) [14] recommends the use of a low-bandwidth setting for the source (upstream) PLL, and a high-bandwidth setting for the destination (downstream) PLL. The first (upstream) PLL acts as a jitter filter when configured as low bandwidth and transfers a very little jitter to the downstream PLL.

A High-bandwidth setting on the downstream PLL allows to track jitter from the first PLL.

To illustrate the implementation of this method, let us take, for example, a 120-MHz clock, whose phase shift of 1/100th of the total clock period is needed to be registered? Then according to (10), the number of subsamples required is 50 (= 50). However, the PLL multiplication factor of 50 requires VCO to operate at 6000-MHz frequency that exceeds the maximum VCO output frequency limit of 1300 MHz in PLL Circuitry for Intel Cyclone FPGAs. Hence, we split the multiplication factor

between two PLLs, as / |PLL1 = 5/7 and / |PLL2 = 10/17, respectively.

B. Sampling Frequency for Subsamples Generation

The phase measurement design works for both oversampling and under sampling clock frequency to generate a particular number of subsamples *( )*, by choosing lower or higher PLL division factor ( ). The preference is given to the under sampling frequency, because it improves the phase noise performance of the *Sampling C L K* significantly. According to the popular PLL manufacturers such as Texas Instruments and Silicon Labs, one of the cardinal principles is that the multiplication of frequency by *N* causes degradation in phase noise performance by 20 log *(N)* with reference to the input clock, while dividing it by the same improves by the same factor. In a classical PLL, due to the existence of the divide by *M* in the feedback path and the PD/CP, the divider noise amplification factor (in power) is M^2. However, the biasness toward under sampling can be avoided if subsampling technology-based PLL is used.

V. Simulation Results

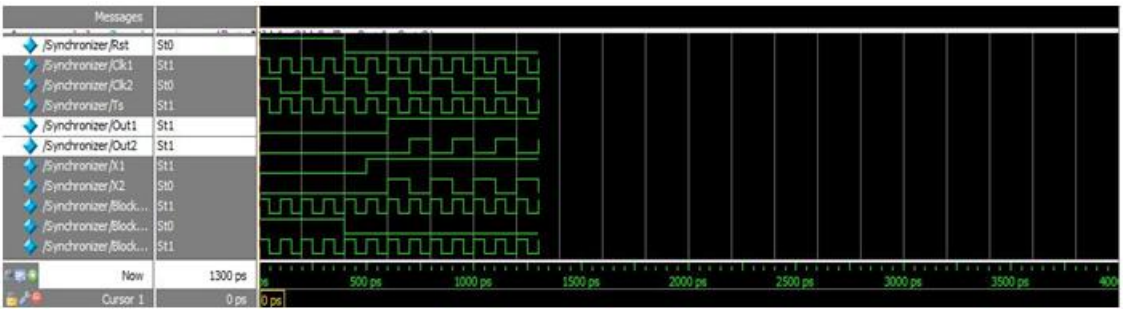

Fig.4 Synchronizer

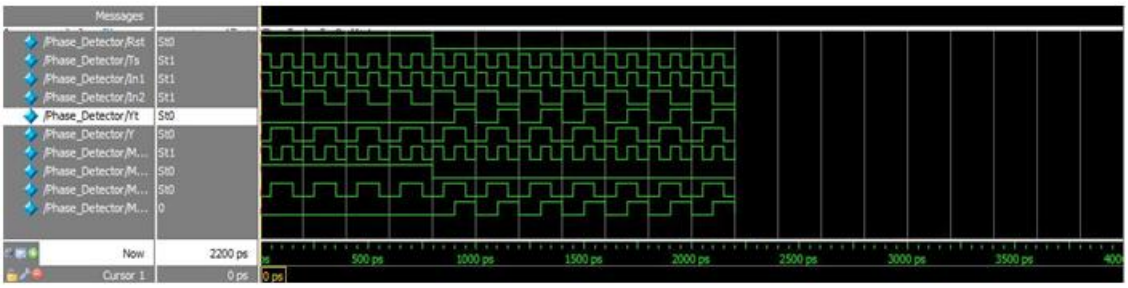

Fig.5 Phase detector

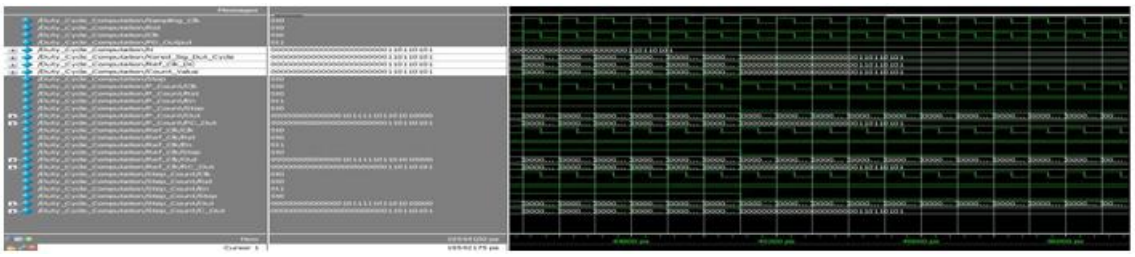

Fig.6 Duty cycle computation

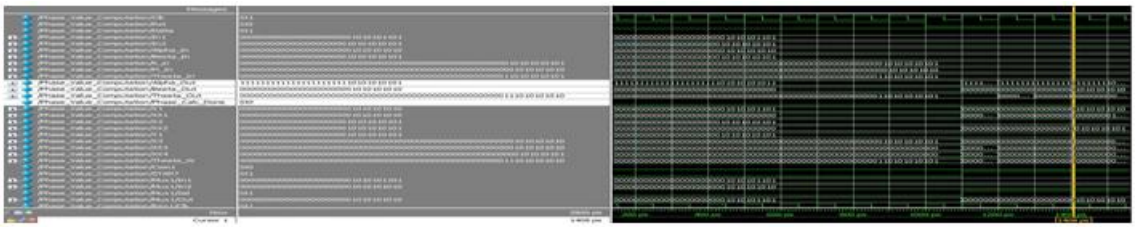

Fig.7 Phase value computation

VI. Conclusion

The development of a sensitive phase detection logic core for FPGA, having precision, accuracy, and resolution in the range of a few picoseconds. This can be used within FPGA as a monitoring device of phase relationship between digital clock pulses, without any additional circuitry. The design is modularized in a way that allows designers to modify different components for more robustness of the design, like replace XOR-based PD with other phase comparator. The concept of using systematic sampling for subsample collection can also be extended to map other complex analog domain problem to digital domain.

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