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# Quadruple Memory cell design with Complete protection against SEU and DNU

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***Abstract--****This paper presents novel quadruple cross-coupled memory cell designs, namely Proposed cell (BQCCM10T cell), with complete protection against single event upsets and double-node upsets. The proposed cell BQCCM10T consists of four cross-coupled input-split inverters and a buffer.Memory cell circuits are more sensitive to external radiation phenomena that are likely to cause the occurrence of soft errors SEU & DNU. Therefore, the tolerance of the circuit to the soft errors is a stern requirement in memory cell circuit designs. Since the traditional error-tolerant methods result in significant cost fines in terms of power, area, and performance, the development of low-cost hardened designs for storage cells(such as latches and memories)is of increasing importance. The Proposed cell achieves complete SEU and DNU tolerance through feedback and buffering mechanisms among its internal nodes.The proposed BQCCM10T cell has high robustness and high Read Access time and Write Access Time. With the help of T-Spice, simulation results of several SRAM cells and the BQCCM10T cell are compared.Hence the proposed cell BQCCM10T is used for highly terrestrial reliable low voltage applications.*

***Index Terms--****Single Event Upset, Double Node Upset, Memory Cell, Soft Error, Quadruple Cross coupled memory cell.*

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## I. Introduction

In the radiation condition, for example, space and atomic blasts, the radiation impact has been one of the fundamental unwavering quality issues of electronic frameworks.To guarantee the system, the dependability of the coordinated circuits that work in space must be solidified for radiation effect. Soft error in the memory cell is of two types. They are of Chip level and System level. Chip level error befalls due to cosmic rays whereas system-level ventures with noise phenomenon system. Higher capacitance and voltage are less likely to suffer an error. Errors can damage data but not the hardware. The cause of the error is Single EventUpset(SEU) [9] and Double Node Upset(DNU). It can be relieved by cold booting(restarting).In the combinational rationale circuit, when a molecule strikes a delicate node in a rationale door, the gathered charges may cause a transient heartbeat, i.e., a single event transient (SET), at the yield of the struck rationale entryway. In this manner, the SET heartbeat may spread through the downstream rationale entryways landing at a capacity component, and the beat might be caught, along these lines prompting invalid worth maintenance. For a capacity module, for example, a memory cell or a flip-flop, a molecule strike may bring about the state change of a single node, in this manner prompting a delicate blunder. This is known as a single event upset (SEU)[9]. In any case, in current progressed nano-scale CMOS innovations, the forceful contracting of transistor highlight sizes can make circuit joining higher and circuit hub dispersing littler.

Another critical problem is that the speed and stability of SRAM decrease with voltage scaling which has been widely used in ultra-low power (ULP) applications such as implantable medical devices, wireless sensor networks and smart grids [10]-[12]. The SRAMs, which are usually used in high speed cache, must cope with the voltage scaling trends to be compatible with the logic. The limitations of applying the near/subthresholdvoltage in SRAM designs are dominated by the following three reasons: 1) with the supply voltage decreasing, the delay of SRAM increases at a higher rate than does CMOS logic circuit delay, 2) low voltage read operations lead to destruction of stored data in SRAM bit-cells, and 3) write operation suffers from a higher rate of failure at low supply voltage [13], [14]. Therefore, due to the possibility of SRAM being affected by SEU at ground level and the three limitations mentioned above of applying the near/subthreshold voltage, there is a trend to propose soft error tolerant SRAM cells for highly reliable terrestrial low-voltage applications.

The development of radiation-hardened technologies in digital circuits is extremely crucial [15]. Due to the larger sensitive volume per bit and lower node capacitance than the dynamic counterpart, SRAM is more prone to soft errors. Therefore, the soft error rate (SER) [16] in SRAM is increased with the technology scaled

in the nano-meter regime. To reduce the SER, numerous alternatives have been proposed to the standard 6T SRAM cell [17]-[25]. The main reinforcementmethod is throughconstructing special topology of transistor connections inside cells to achieve circuit-level protection. The soft error robust Quatro-10T SRAM cell, offering differential read operation with large noise margin was proposed in [17]. However, it can only recover from "1" to "0"; thus, it cannot immune SEU completely. Due to the feedback of the dual node, the dual interlocked storage cell (DICE) [18] can fully immune against single-event transient (SET) occurring on any of its single nodes

Therefore, because of charge-sharing, the strike of one molecule may all the while change the conditions of two hubs in a capacity component, which is known as a double node upset (DNU).There are several varieties of SRAM cell designs. They are Non-volatile, Pseudo, By transistor, Function, Feature, Flip Flop. Non-volatile SRAM is the same as SRAM but saves data when power is off. Pseudo SRAM has a DRAM core, slower than SRAM, has separate refreshing circuits. By transistor type, cells are designed using Bipolar and MOSFETs. By function type, they are asynchronous and synchronous. By feature, they are DDRSRAM (Double Data Rate I/O SRAM) and QDR SRAM (Quad Data Rate I/O SRAM). DDR SRAM is synchronous, has a single write and read port. QDR SRAM has a separate read and write port. Most technologies prefer QDRSRAM since it has quadrate I/O and has separate read and write port.

The proposed Cell completely hardens DNU whereas the existing cell systems partially hardens DNU. The proposed cell has higher compilation time than the existing cell system. The remainder of this paper is composed as follows. section II portrays the existing SEU, as well as partially DNU, hardened cells. Section III portrays the schematics and working standards of the proposed memory cell structures. section IV presents test results and examination results. section V concludes the paper.

## II. Existing Memory Designs

The below sections deal with the existing memory designs. First, it has a standard 6T cell. Then following up on the hardened measurement we deal with NASA13T, LIN12T, RHD12T, QUCCE10T, QUCCM10T. All the memory cell above has a complete SEU hardened cell but a partially DNU hardened cell.

### *A. 6T Cell*

The schematic of the 6T cell is shown in Figure 1. The storage module of the 6T cell consists of a couple of cross-coupled inverters. The 6T cell is widely used because of its simple construction and small area. However, the 6T cell cannot tolerate an SEU. Therefore, many radiation-hardened cells have been proposed for reliability improvement.

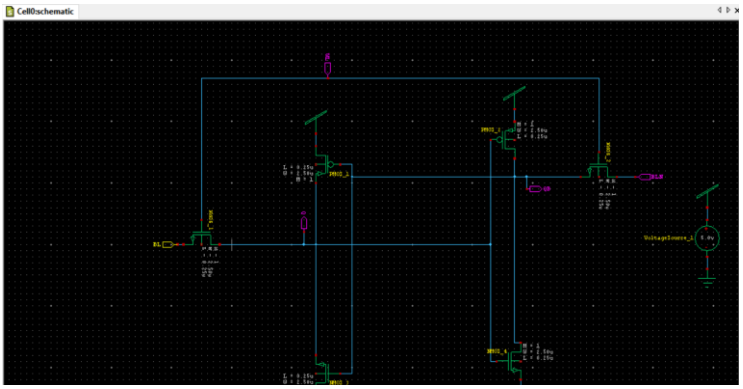


**Figure 1:** 6T cell

The classic design for a SRAM memory cell is thesix transistors design, 6T, shown in Fig. 1. The 6T memory cell uses a feedback loop between two cross-coupled inverters formed by four transistors: N1 − N2 – the pull down NMOS transistors and P3 − P4 – the pull up PMOS transistors. The cross-coupled inverters retain the stored data value. The 6T memory cell has three modes of operation: write mode − data is deposited into the cell, read mode − data is read from the cell, standby mode − the cell is idle and is not being read or written to[2].

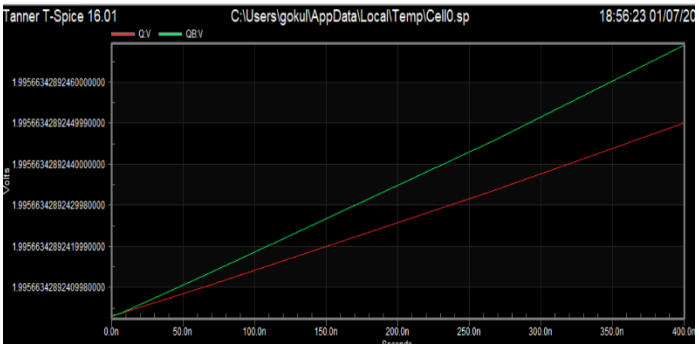


**Figure 2:** Simulation Result of 6T cell Design

*B. NASA13T Cell*

The schematic of the NASA13T [2] cell is shown in Figure3. The module is an improvised version of the 6T cell. It suffers from a large area and power dissipation and cannot tolerate SEU for large energy particles. The module is of two parts, the upper part is the storage module and the lower part is for protecting values. It has a high read and write access time.

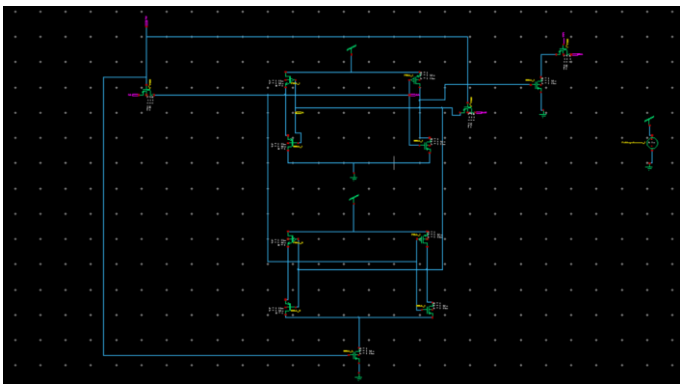

Figure 3: NASA13T

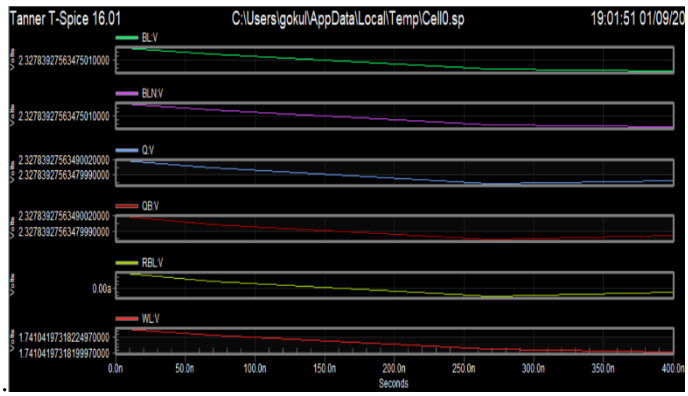


**Figure 4:** Simulation Results of NASA13T cell Design

The design offers low power consumption, high level of soft error tolerance, high read cell stability and fast write time performance. The design was optimized to achieve maximum advantages in comparison with other hardened SRAM designs. Temperature dependence and voltage scaling have been analysed for design performance [2].

*C. LIN12T*

The Schematic of LIN12T[1] cell is shown in Figure 5.

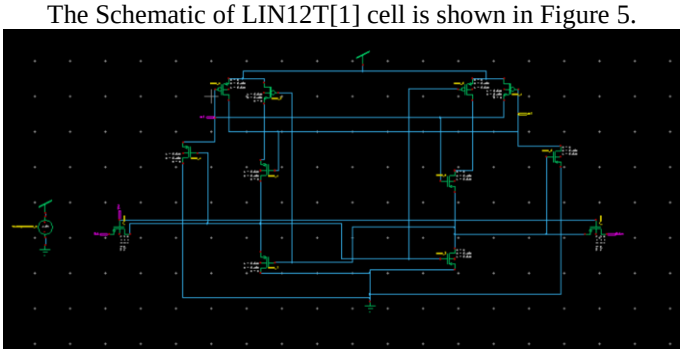

**Figure 5**: LIN12T

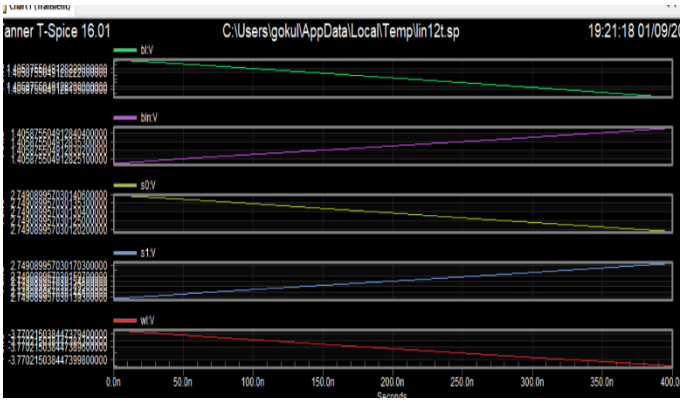


**Figure 6:** Simulation Results of LIN12T cell Design

The module is an improvised version of the NASA13Tcell. It suffers from a large area and power dissipation and can completely tolerate SEU. It uses two storage nodes (Q, Qn) and (S0, S1). Only one pair of the module is DNU hardened.The source and drain terminals of access transistors N5 and N6 connect bit lines (BL and BLN) and storage nodes (Q and QN). Moreover, gate terminals (S0 and S1) of cross-coupled transistors P1 and P4 are also storage nodes, which increase the redundancy of nodes for SEU tolerance.

*D. RHD12T*

The Schematic of RHD12T[4] cell is shown in Figure 7. The module is an improvised version of the LIN12Tcell. It has less area and power consumption and can completely tolerate SEU. It uses two storage nodes (Q, Qn) and (S0, S1). Only one pair of the module is DNU hardened. SEU is completely hardened using feedback loops.

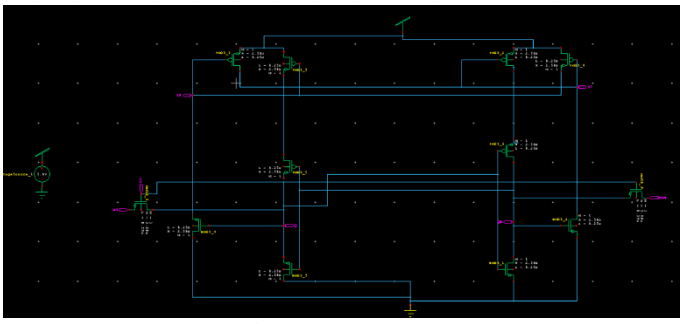

**Figure 7:** RHD12T

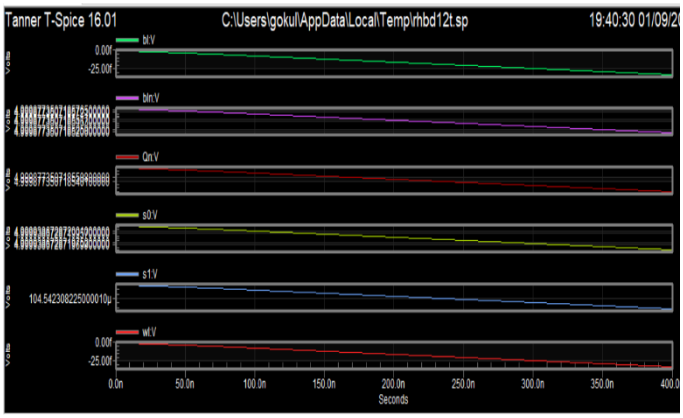


**Figure 8**: Simulation Results of RHD12T cell Design

SEU recovery behaviour analysis at circuit level under the assumption of QN = 0, Q = 1, S0 = 0, and S1 = 1 are given without considering layout information. By analysing the off/on states of all transistors in Fig. 4 when the corresponding nodes were hit, it can be concluded that if an upset occurs on node S0, S1, Q or even node pairs S0–S1, RHD12T [7]memorycell can holdits originalvalue.For example, if an upset occurs on node S0, the state of node S0 will be changed from 0 to 1 which temporarily turns off transistors P1 andP2, but this changecannot furtheraffectthe off/onstates of other transistors. In

other words, nodes S1, Q, and QN hold its originalstate,whichconfirmsthatRHD12TSRAMcellcan hold its correct value after encountering particle strike. However, if an upset occurs on node QN, at circuit level analysis, node QN changes its state to 1 (in layout level design, it has been made very difficult to change to 1 shown in next section). Analysing the off/on states of all transistors in RHD12, we can see that all transistors have a chance to change its off/on state, which finally makes RHD12 upset [4][8].

*E. QUCCE10T*

The Schematic of QUCCE10T[6] cell is shown in Figure 9.

The module is an improvised version of the RHD12Tcell. It has less area and power consumption and can completely tolerate SEU. It has four storage nodes(A, Q, Qn, B). It acts as a feedback loop (A->Q->Qn->B->A). DNU is not hardened. It has a high read and write access time.

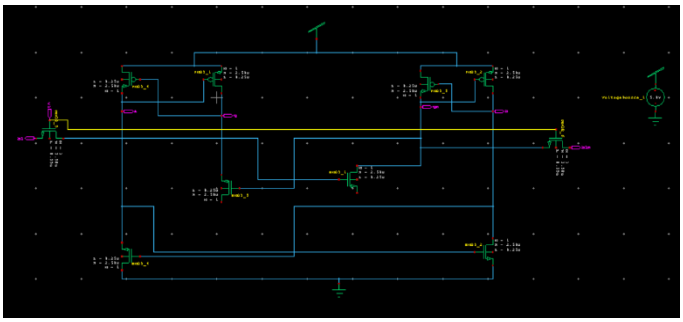

**Figure 9**: QUCCE10T

The QUCCE 10T memory cell has four storage nodes A, Q, QN and B. The output nodes, Q and QN, are connected to the bit lines BL and BLB through pass gates N5 and N6, respectively. The two access transistors N5 and N6 are controlled by word line WL and will be enabled when WL is at high logic state. The stored ‘0’ state for the proposed QUCCE 10T cell is taken into consideration [6].

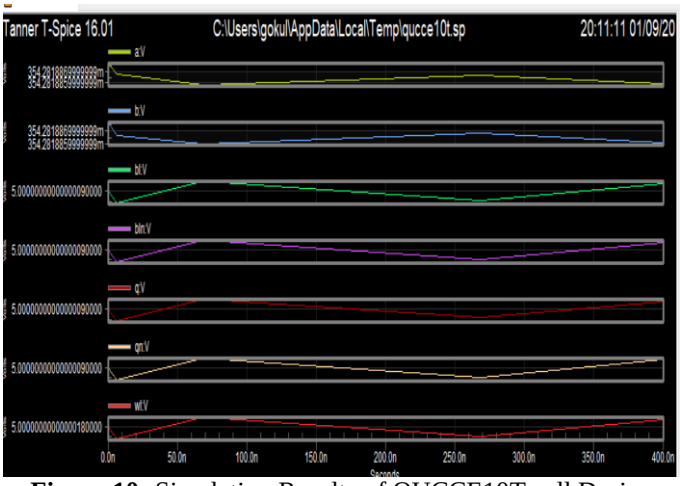


**Figure 10:** Simulation Results of QUCCE10T cell Design

*F. QUCCM10T*

The Schematic ofQUCCM10T[1] cell is shown in Figure11.

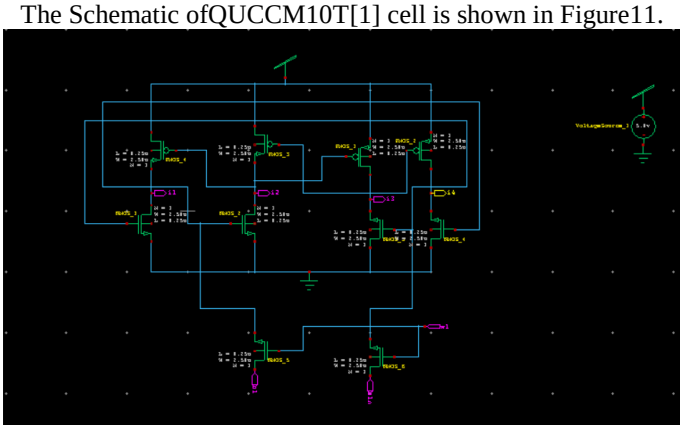

**Figure 11:** QUCCM10T

The module is an improvised version of the QUCCE10Tcell. It has less area and power consumption and can completely tolerate SEU. It has four interlocked input split-inverters and nodes namely I1, I2, I3, I4. It has a high read and write access time. Based on RHBD(Radiation hardening by design) it reduces SEU & DNU. DNU is hardened for non- adjacent nodes and one adjacent node (I2, I3).

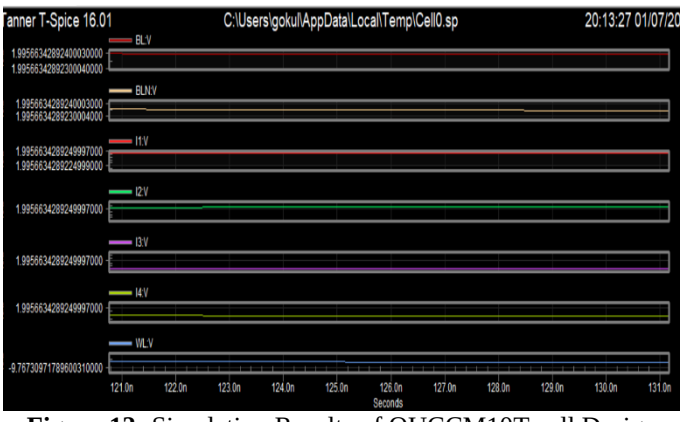


**Figure 12:** Simulation Results of QUCCM10T cell Design

The normal operations of the proposed QCCM10T cell are described as follows. Let us first consider the case of writing 1. Before the normal write operation, owing to the writing circuitry, BL = 1 and BLN = 0. When WL = 1, the operation of writing 1 is executed. Transistors P1, N2, P3, and N4 are ON. Meanwhile, transistors N1, P2, N3, and P4 are OFF, so that the stored value is rightly changed to 1, and the operation of writing 1 is completed. Next, let us consider the case of reading 1. Before the normal read operation, owing to a

pre-charge circuitry, the voltages of bit-lines BL and BLN will be set to 1. During the read operation, WL = 1, and access transistors N5 and N6 become ON immediately. Nodes I1, I2, I3, and I4 are keeping the stored values, and the voltage of BL does not change. However, the voltage of BLN decreases due to the discharge operation through N4. BL and BLN are directly connected to a differential sense amplifier, and once the voltage difference between BL and BLN becomes a constant value, the read operation is completed and 1 is read out.
Note that, similar scenarios can be observed when writing/reading 0. The simulation results of normal operations of the proposed QCCM10T cell are shown in FIGURE 5. It can be seen that "write 0, read 0, write 1, and read 1" operations are correctly executed. Next, the fault tolerance principle of the proposed QCCM10T cell is described. To illustration, we consider the case of a 1 being stored in the cell (i.e., I1 = I3 = 1 and I2 = I4 = 0). In the next section, we discuss the SEU-tolerance principle and the DNU-tolerance principle, respectively [1].

## III. Proposed Memory Design

The below diagram represents the schematic view of proposed cell design. It is an improvised version of QUCCM10T cell with the introduction of buffer in the I1 & I4 nodes which completely hardens DNU.

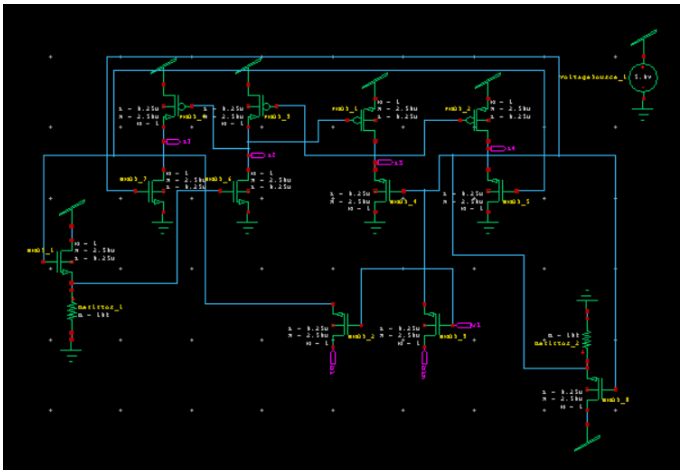

**Figure 13:** BQCCM10T cell design

Transistors N5 and N6 are used for access operations and their gate terminals are connected to word-line(WL). BL and BLN are bit-lines. I1, I2, I3, and I4 are storage nodes for keeping values. FIGURE 7 shows the schematic of the proposed cell. When WL is high (WL = 1), the access transistors are ON, allowing read/write operations to be executed. When WL is low (WL = 0), the cell keeps the stored values.

The normal operations of the BQCCM10T cell are described as follows. Let us first consider the case of writing 1. Before the normal write operation, owing to the writing circuitry, BL = 1 and BLN = 0. When WL = 1, the operation of writing 1 is executed. Transistors P1, N2, P3, and N4 are ON. Meanwhile, transistors N1, P2, N3, and P4 are OFF, so that the stored value is rightly changed to 1, and the operation of writing 1 is completed. Next, let us consider the case of reading 1. Before the normal read operation, owing to a pre-charge circuitry, the voltages of bit lines BL and BLN will be set to 1. During the read operation, WL = 1, and access transistors N5 and N6 become ON immediately.

Nodes I1, I2, I3, and I4 are keeping the stored values, and the voltage of BL does not change. However, the voltage of BLN decreases due to the discharge operation through N4. BL and BLN are directly connected to a differential sense amplifier, and once the voltage difference between BL and BLN becomes a constant value, the read operation is completed and 1 is readout. Note that, similar scenarios can be observed when writing/reading 0. The simulation results of normal operations of the proposed cell are shown in FIGURE 8. It can be seen that "write 0, read 0, write 1, and read 1" operations are correctly executed. Next, the tolerance principle of the proposed cell is described. For illustration, we consider the case of a 1 being stored in the cell (i.e., I1 = I3 = 1 and I2 = I4 = 0). In the next section, we discuss the SEU-tolerance principle and the DNU-tolerance principle, respectively.

A. SEU Tolerance Principle

Case 1: I1 is affected,since it is affected it changes from one to zero, hence Transistor terminals N2 & N4 are OFF. I3 is not affected since P2 & P4 are still OFF. P1 is still ON & N1 is still OFF so a strong 1 can neutralize a weak 0 in I1. Thus, it automatically recovers from SEU.

Similarly, in case, I3 is affected, Transistor terminals P2 & P4 changes from OFF to ON. I1 is not affected since N2 is ON. I4 is temporarily put to 1 (weak 1) as P4 is ON since I1 is not affected N2 is ON. I2 is not affected too since weak 1 from P2 does not affect strong zero. Henceforth N3 changes to one. Thus, self-recovery of SEU is done.

B. DNU Tolerance Principle

It can be applied to six nodes of pairs (I1, I2), (I1, I3), (I1, I4), (I2, I3), (I2, I4), (I3, I4). The proposed design can completely harden DNU. It hardens DNU even in adjacent nodes with the help of buffer circuits.

When I2 & I3 is affected. P1 & P3 are OFF and P2 & P4 are ON. So N1, N2, N3, N4 are not affected. Therefore I1, I2 is determined. I1 is still ON which makes N4 ON. Here P4 is temporarily ON (weak one), once N4 is ON and I4 is determined, strong Zero of I4 overcomes weak one of P4 and makes P4 OFF. Similarly, I1 is One and N2 is ON which has a strong zero. So strong Zero neutralizes weak 1 of P2 and P2 is made OFF. Thus, I2 is put to zero. I3 self recovers from DNU with the help of RHBD design.

| CELL | DISADVANTAGES |
|---|---|
| NASA13T Cell | Cannot tolerate SEU for large energy particles. |
| LIN12T Cell | Largearea and power consumption. |
| RHD12T Cell | DNU is partially hardened. |
| QUCCE10T Cell | DNU is nothardened. |
| QUCCM10T Cell | DNU is partially hardened. |
| BQCCM10T Cell | High compilation time. |

**Figure 14:** Disadvantage Table

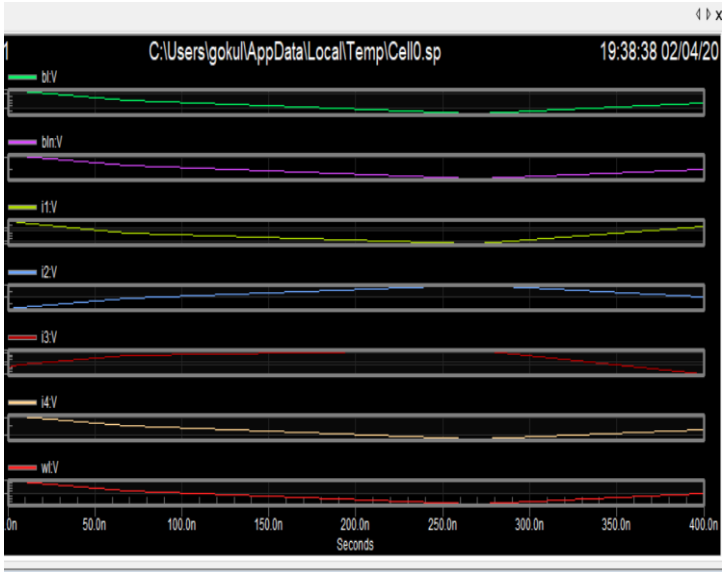


**Figure 15:** Simulation result for BQCCM10T cell design

Similarly, in the case of I1 & I2. I1 & I2 is affected, so the transistor terminals P1, P3, N2, N4 changes from ON to OFF. With the help of separate buffer circuits connected to I1 & I4 node. Buffer connected to Node I1 has strong One which flows to N2 terminals that can neutralize weak zero and thus make N2 ON. Similarly, Buffer connected to the I4 node has a strong Zero that can neutralize the weak one of the P3 terminal and thus makes P3 ON. Thus, I1 and I2 are determined. With the help of Strong One from N2 terminal I1 is recovered, thus P1 is ON. I2 is self-recovered from DNU with the help of RHBD design.

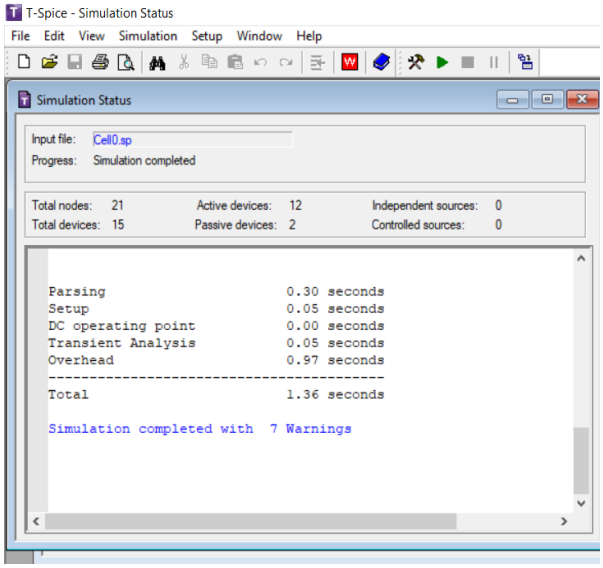


**Figure 16:** Result of BQCCM10T cell Design

## IV. Result

The following is the compilation results of ProposedMemory cell Design QUCCM10T, QUCCE10T, RHD12T, LIN12T, NASA13T, 6Tcell designs. Though the proposed cell BQCCM10T has higher compilation time, it completely hardens Double-Node Upset(DNU) and Single Event Upset (SEU).

| Memory cell Design | Compilation Time |
|---|---|
| 6T | 0.79sec |
| NASA13T | 0.61sec |
| LIN12T | 0.69sec |
| RHD12T | 1.12sec |
| QUCCE10T | 0.68sec |
| QUCCM10T | 0.45sec |
| Proposed Cell | 1.36sec |

**Figure 17:** Compilation Result Table

## V. Conclusion

In this paper, a novel quadruple memory cell design namely BQCCM10T has been proposed. It completely hardens SEU and DNU with the help of buffering mechanisms. It has high reliability and can be much effectively used for applications such as nuclear, aerospace, and high reliable appliance.

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## VII.DECLARATION

- **AVAILABILITY OF DATA AND MATERIAL**

Not applicable in this section.

- **COMPETING INTERESTS**

The author Gokul Somasundaram declares that they are no competing interests.

- **FUNDING**

Not applicable in this section.

- **AUTHOR CONTRIBUTIONS**

Gokul Somasundaramconceived the idea, designed, simulated the experiment, analyzed the data and wrote the manuscript**.**

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