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Design of CMOS VCO for Implementation of Phase Locked Loop

Alpana A. Deshmukh*[1], Radheshyam Gamad[2], Deepak Kumar Mishra[3]
[1] Ph.D. Scholar , [2]Professor and Head , [3] Professor of Electronics & Instrumentation Engineering Department, SGSITS, Indore
Madhya Pradesh India

Abstract— *Paper presents a new design approach of voltage-controlled ring oscillator for PLL based applications in a communication system for low voltage and power range. This approach reports a 1.8 GHz to 2.8 GHz five stages VCO design using current starved method for CMOS technology. Paper also reports comparative analysis of five stages VCO with three stages VCO. Five stage design analysis shows 3.07 µW power consumption for 22 nm @ 0.4 GHz to 26.04 GHz and three stages design represents 15 mW for 180 nm @15 MHz to 5 GHz.*

Keywords*- CMOS, VCO, PLL, FFT, PMOS, NMOS*

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I. Introduction

Due to latest technologies in the field of CMOS design is topped down in order to lower cost, higher speed and compact design at higher level. Now a day these technologies are growing up for wireless communication system. Design based on these devices is very useful for chip fabrication. This paper proposes VCO design for mixed signal processing system design. This circuit plays vital role in electronics devices, whose frequency is linearly varied by input control voltage. It is perhaps the integral part of the phase locked loop. It can be design using various configurations like ring and LC based resonant devices. It is mostly useful in communication, radio frequency integrated areas like transponder, clock generation and in medical based devices. In this design approach CMOS based VCO are implemented for high frequency range [1] [2]. It provides enhanced speed, larger bandwidth and lower power because it produces in multiple phases.

Odd numbers of inverters are requiring in ring oscillator based VCO circuit. Feedback of last stage inverter is connected to the first stage inverter. Its connections are shown in fig. 1 with amplifier or inverter circuits. Here single ended inverter circuit requires odd number of inverting stages, which is a circuit having advantages of easier design and integration of multiple devices. Due to these properties, it requires very small area and wide tuning ranges.

Here frequency of oscillation can be determined by no. of stages and each stage having delay which is very less for inverter. VCO output can be achieved, with various range of frequency, if the delay is voltage controllable. The proposed VCO is used for the PLL based applications in communication circuits. Here inverter based diagram of VCO shown in fig. 1 & schematics diagram of current starved VCO is shown in fig. 2 [3][4][5].

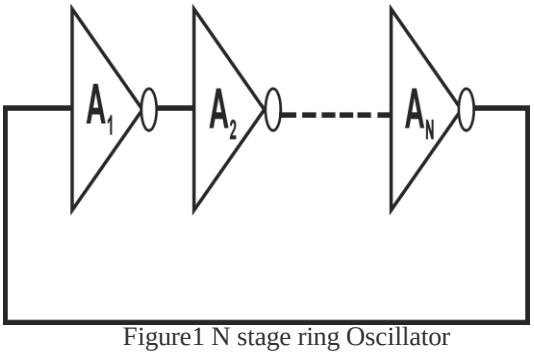

Figure1 N stage ring Oscillator

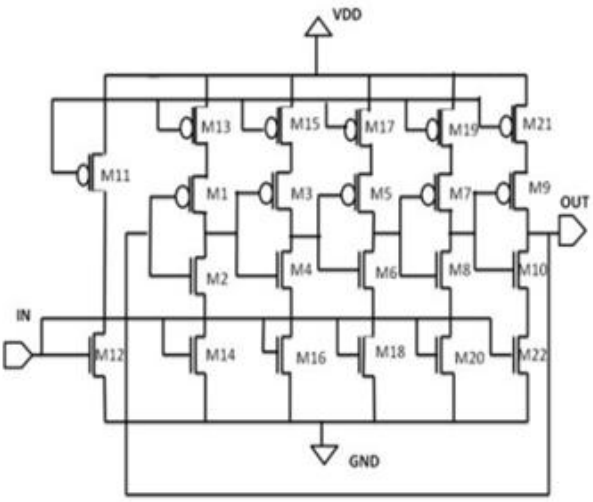

Figure 2 Schematic of 5 stage Current Starved Method

Fig. 2 represents five stage current starved methods is shown, which is same as ring oscillator and functionality of it is also consistent to that in circuit PMOS13 and PMOS14 act as current source. In this circuit drain current of PMOS11 and PMOS12 are resembles and are set by the input control voltage. Each inverter stage is current mirrored stage just like in M11 and M12. The Oscillation frequency of current starved VCO (5 Stage) is given in (1) [6].

$$Fout = F_0 + K_{VCO} V_{ctrl} \qquad (3)$$

F_0 = Frequency of oscillation of VCO. K_{VCO} is the gain of VCO which checks variation over control voltage V_{ctrl} which is input to the VCO determining its operating frequency. Power can be consumed in two different ways: Dynamic & Static. In case of single stage device power can be calculated as given in (4).

$$P = P_D + P_S \qquad (4)$$

Previously in electronics based devices, static power was very less. But this approach is based on nanometer technologies which require static power. This power is playing very vital role in advance technologies. Today in most advance technologies, static power consumption exceeds dynamic power consumption. Now a day's CMOS gates are consuming dynamic power because load capacitance are going to be charge & discharge by them. Power consumption is also based on rate at which the inverter's output switches and the size of the capacitive load, which is held on output of the circuit. Inverter current and voltage output can be calculated in (5), (6) [7][8][9][10].

$$I_{CL}(t) = \frac{V_{DD} - V_{ss}}{R_p} e^{-(t/R_p C_l)} \qquad (5)$$

$$V_{CL}(t) = (V_{DD} - V_{ss}) \qquad (6)$$

Where C_L is load capacitor & R_p is effective resistance. The gain of the amplifier from small signal model in fig. 3 is $A = g_m r_d$.

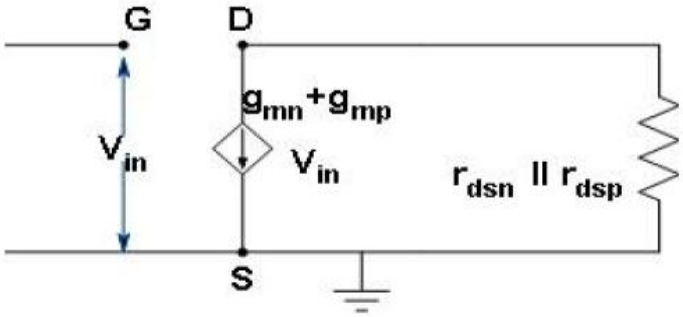

Figure 3 Small Scale Model of inverter

II. Proposed Methodology

Phase locked loop has become a widespread circuit in latest electronics based systems especially in the wireless area. Due to low cost, low power consumption and stability in frequency generation, it finds application in the various areas like frequency synthesizers, modulation and demodulation of FM signals, FSK decoders, two-tone decoders, motor-speed control, frequency multiplications etc. This paper presents applications of PLL in frequency synthesizer. It is a feedback control system. Error signals are being produced by computing phase of two input signals of PLL which is proportional to the phase difference of the given input signals. Error signals are driving VCO which generate output frequency & passed through the low pass filter which creates output frequency. It is served to a frequency divider back to the input of the system, which will generate negative feedback loop. Phase error signal will increase by output frequency drifts & to reduce the error drives the frequency in opposite direction. Thus the output is locked to the frequency at the other input. Crystal oscillator will derive reference input which coming from the locked output signal with stable frequency. This method shows design of VCO for getting different-different frequency ranges in various applications of electronics system. Circuit generates clock with a controlled frequency. It is basically generating clock in PLL circuits. Clock may be approximately by +/- 50% of its control frequency [11][12][13]14]. Fig. 4 shows layout of VCO using ring oscillator which is useful in PLL based frequency Synthesizer. Fig. 5 shows PLL based frequency Synthesizer which having two broad categories; Direct method and indirect method. This paper presents indirect frequency synthesis method which is based on phase locked loop. It is generated by an oscillator that is controlled by other signal as shown this here.

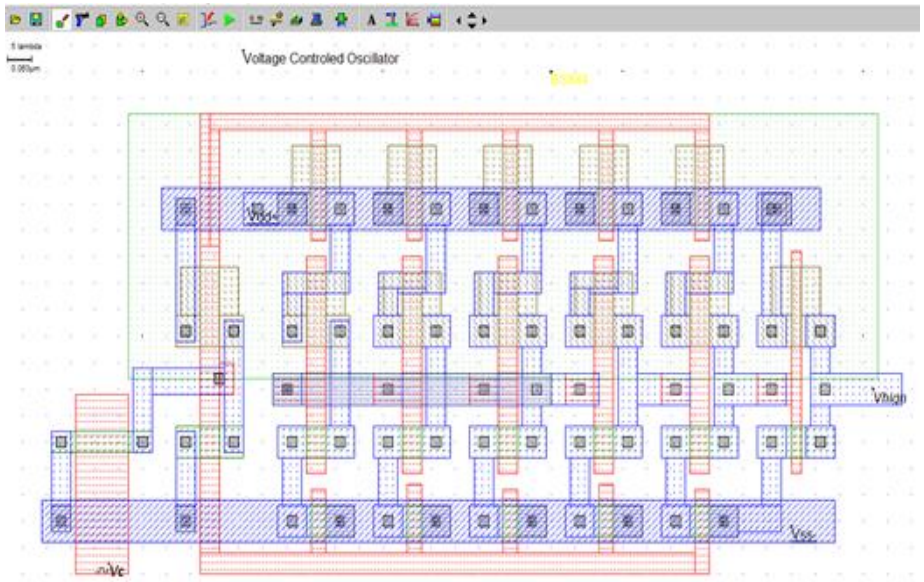

Figure 4 Five stage VCO Layout for 22 nm

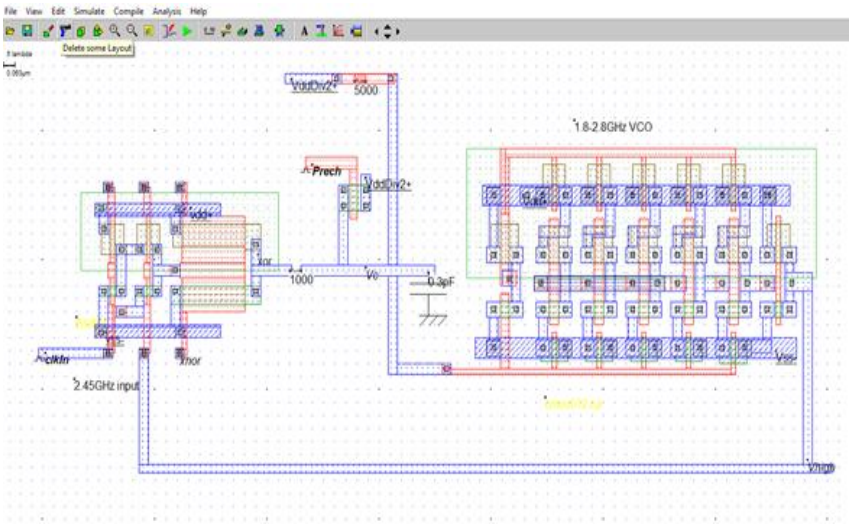

Figure 5 Layout of PLL Circuit

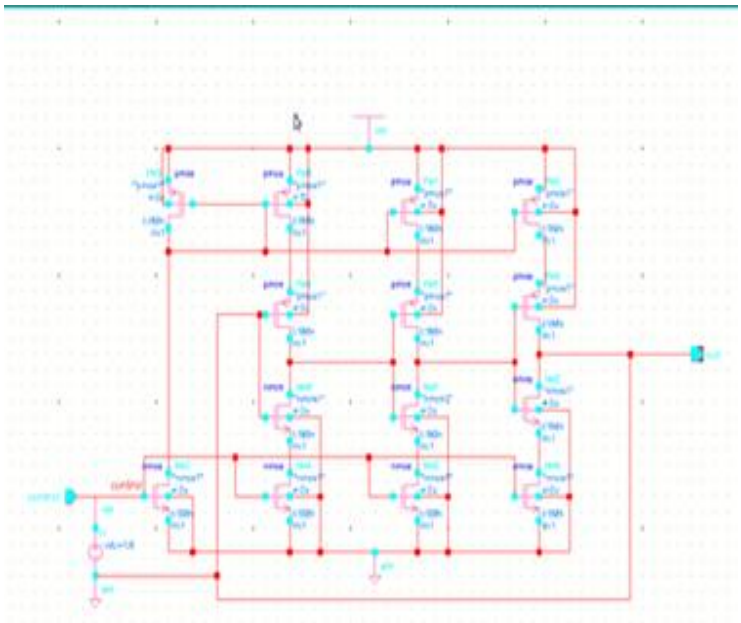

Figure 6 Three Stage VCO Layout for PLL design on cadence tool

III. Results and Discussions

VCO design approach has represented in fig. 6 whereas fig. 7 shows voltage versus time plot at 18.175 µw power for the given design. One line represents V_{high}, which is varying according to the time period, whereas another one line shows pretch signal, 3rd line is clock time period in nanoseconds. Each period shows 0.18 ns difference and rest line is for input control voltage which is varying from 0 to 1volt. Fig. 8 shows frequency versus time response in which time is started from 2.0 ns to 2.8 ns range and frequency range would be start from 4.65 GHz to 6.96 GHz for W=1 µm & L= 0.025 µm. Whereas FFT response of PLL circuit shown in fig. 9. In this response minimum voltage is 0.2 mv @ MHz frequency. From 1302 MHz frequency and 10 mv voltage, graph of frequency and voltage will constantly increasing. FFT response from 1000 MHz@ 0.001 mv to 9000 MHz @ 0.33 mv also shown in table 2. Fig. 10 shows drain current versus gate voltage at constant base voltage V_b, where values of V_b are varying from 0 volt to 0.20 volts. Whereas in fig. 10, 1st line is for low leakage current, 2nd for high speed & 3rd line is for high voltage 0.75µm speed at high voltage range & 1.25 µm speed found for low leakage current. Gate to source voltage versus drain current in the range of 10 mA to 75 mA is represented in fig. 11. It means internal design of VCO using MOSFET requires very low level of voltage and current for executing the design of the circuit. While this approach shows gate to source voltage versus drain current in range of 0 to -100 mv voltage to 10 mA to 75 mA current in fig. 12. Whereas fig. 13 shows (ON Current) I_{on} current versus I_{off} (OFF current).

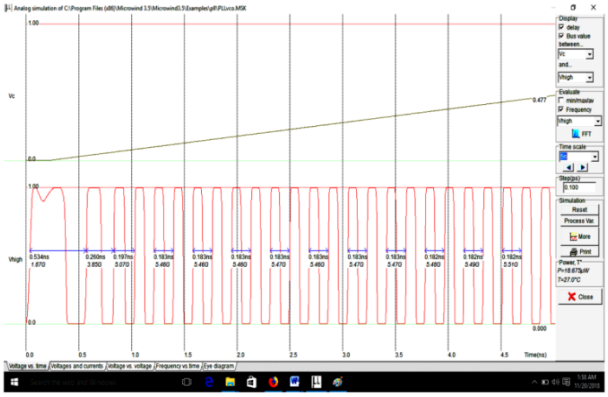

Figure 7 Voltage versus time

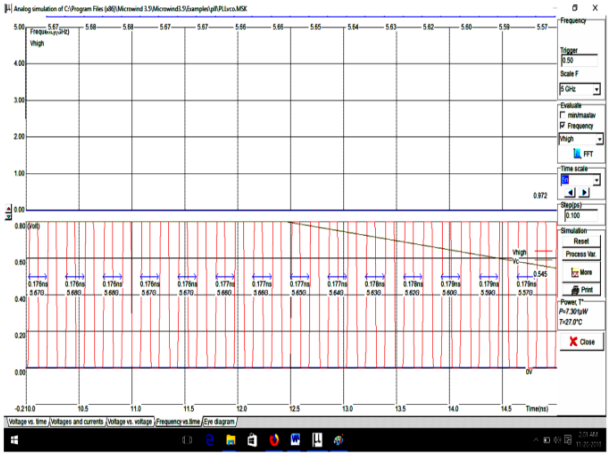

Figure 8 Frequency versus Time (W = 0.175µm, L = 0.025µm)

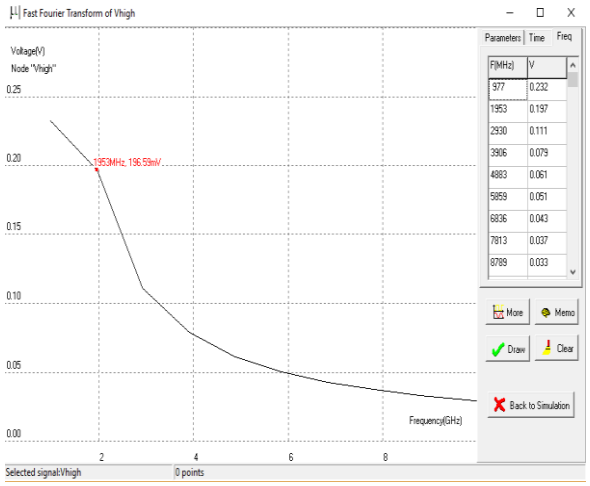

Figure 9 FFT Response of PLL

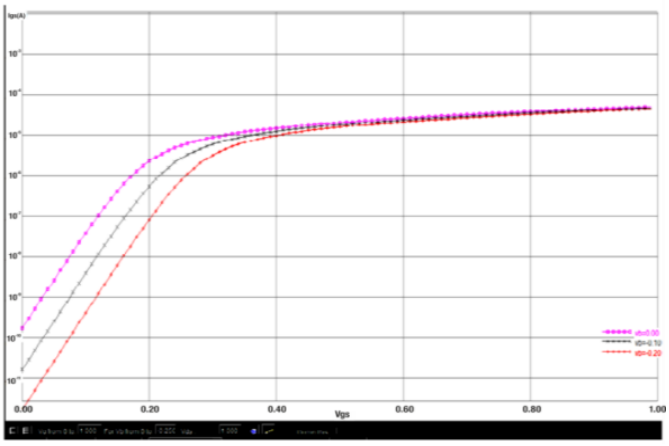

Figure 10 V_{gs} versus I_{gs}

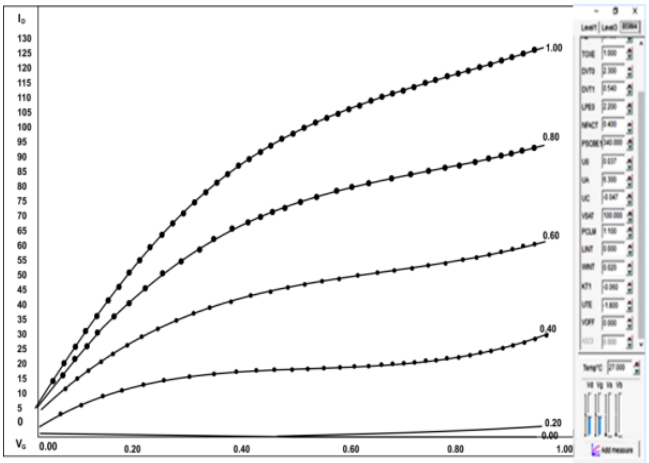

Figure 11 Voltage versus current graph (I_D Versus V_G) for NMOS

In this graph voltage levels varies with respect to the change in ON and OFF current. Here, Red dots are for high voltage level and pink dots are for low leakage current and black dots are for high speed of current. So these dots show the different levels of voltages. While Fig. 14 represents drain current versus drain voltage for W = 0.072 µm & L = 0.35 µm. Values of W and L can change the value of current and voltage in the design. All mentioned plots represent output response of 3 Stage VCO in Microwind 3.5 tool. Same layout has been design in cadence virtuoso tool. Its output response is shown in fig. 15. Values of time are varying from 0 to 4.4 nsec and voltage range would be 0.4 volts to 1.8 volts. Time period is in very low level means frequency of oscillation will be in GHz range. Output of this layout is based on 180 nm design technology. Comparative analysis based on this layout is discussed in fig. 16. Analysis of these graph are also mentioned in the form of tables.

Table 1 represents comparative analysis of 180 nm and 22 nm technology. In which 3 stage VCO circuit works on 180 nm technology and 5 stage VCO circuit represent 22 nm technology. Design of 5 stage circuit is complex than 3 stage circuit but design technology of this circuit is comparatively advance than 3 stage design that's why power consumption in this technology is very low in microwatt range with gigahertz frequency but in 180 nm technology power consumption is in milli watt range with same frequency range. Analysis of this table also showed in fig. 16 and 17. In fig. 16, blue color represents 180 nm and red represents 22 nm technologies. In Y-axis 0 to 5 numbers represent different ranges of control voltage, frequency range and power consumption in used design.

Similarly fig. 17 shows Y-axis range from 0 to 8 with reference to design technologies. In fig. 18, different colors of plot shows comparative analysis of various versions of design with this work with respect to

CMOS based technology, VDD, Power dissipation and operating frequency range. Red color is for 32 nm, blue color is for 22 nm, green is for 45 nm and violet color is for 180 nm. This work shows blue and violet color plot which represents almost similar values of VDD and operating frequency, whereas power dissipation is increasing slightly.

Table 1 Comparative of VCO design for CMOS Technologies

S. No.	3 stage	5 stage
Technology	***180nm***	***22nm***
Control Voltage	1.8v	1.8v
Power Consumption	15 mW	3.07µw
Frequency Range	15MHz to 5GHz	0.4GHz to 26.04GHz

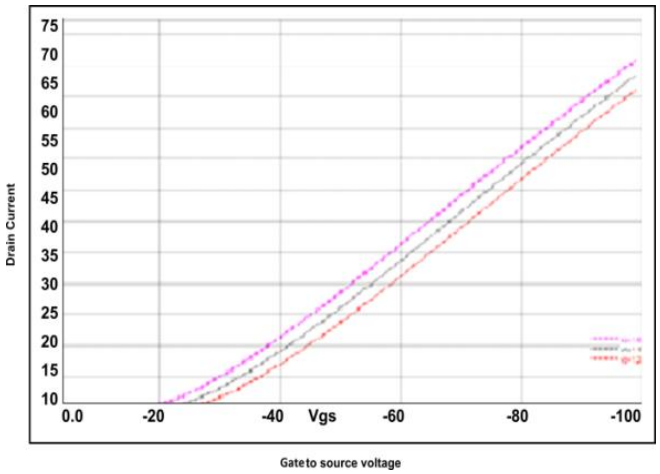

Figure 12 I_d Versus V_{gs}

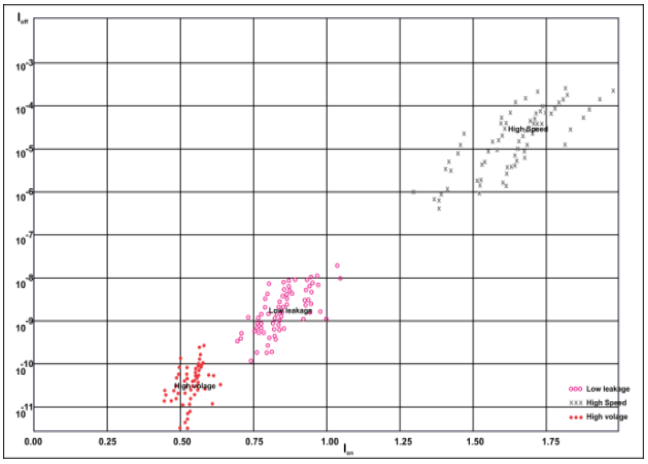

Figure 13 I_{off} Versus I_{ON}

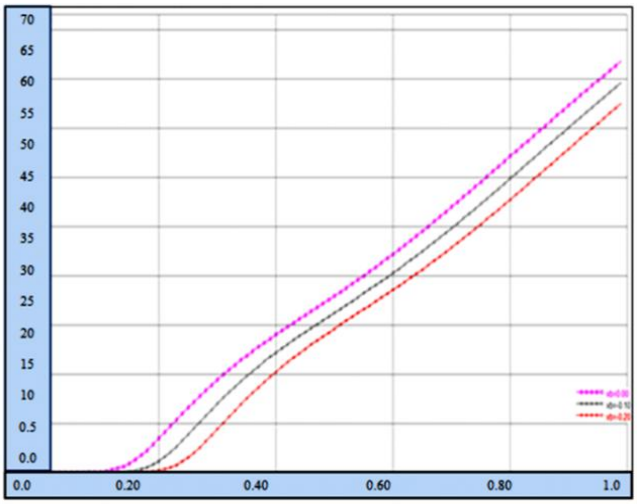

Figure 14 Drain current versus drain voltage (W=0.072µm and L=0.35µm)

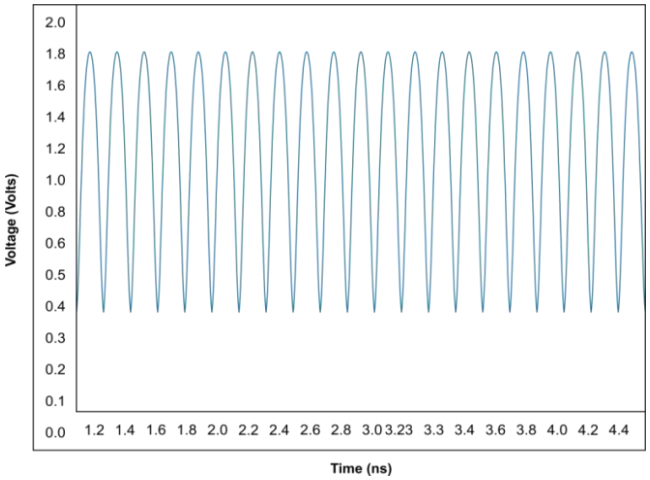

Figure 15 Output waveform of 3 stage VCO

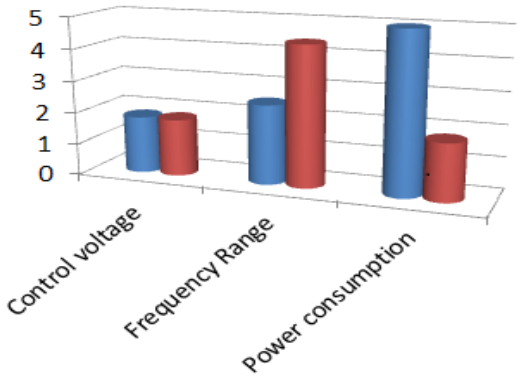

Figure 16 Analysis of design technologies

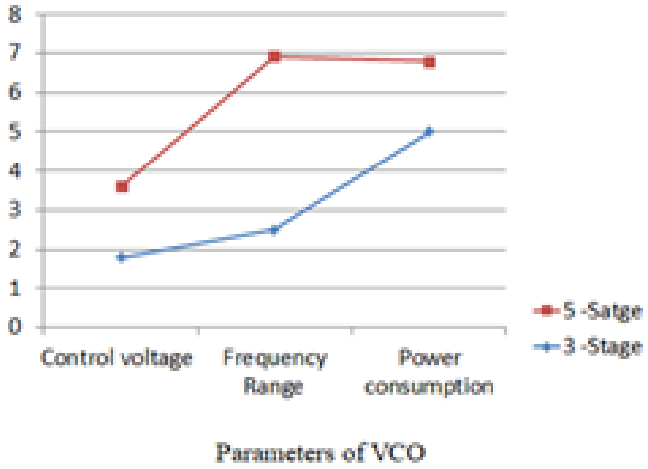

Figure 17 Comparative analyses of 5 stage and 3 stage design

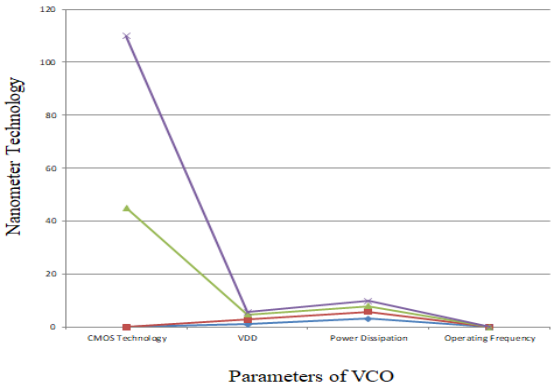

Figure 18 Comparative of VCO design with various nanometer technology

IV. Conclusion

Current starved VCO have been designed in this paper for wide tuning range of frequency with various design parameters. Hence paper reported this design for PLL based applications like frequency synthesizer in the field of communication engineering. The proposed 1.8 to 2.8 GHz VCO is implemented in 22 nm CMOS technology with comparative analysis of other CMOS technologies. Response of this work has been found better than previous reported work. VCO circuit for 3 stage ring oscillator implemented in cadence tool in 180 nm technologies and compared with 5 stages design based on 22 nm technologies. The proposed result provides possibility of achieving low power consumption with low voltage and current parameters and therefore less circuit design efforts. In the future, a complete design may use for advance CMOS technologies with less complexity.

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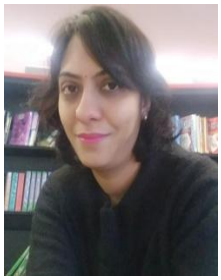
Biographies



Mrs. Alpana A. Deshmukh is a Research Scholar in E & I Engineering Department at SGSITS Indore MP and she has received the BE in Electronic & Telecommunication Engineering from the SGSITS Indore, R.G.P.V. Bhopal University Madhya Pradesh India in 2004 and M.E. in Digital Instrumentation Engineering from the IET, DAVV University Madhya Pradesh, Indore, India, in 2007. She is currently pursuing PhD from SGSITS, Indore in optimum way to implement and test analog and mixed signal circuits. Her current research interests include mixed signal circuit design and testing, embedded processor, circuit theory and devices, Image processing. She is a life member of the ISTE.

Dr. Radheshyam Gamad is a HOD in the E & I Engineering Department at SGSITS Indore MP and he has received the BE in Electronics and communication Engineering from Govt. Engineering college Ujjain, Madhya Pradesh, India, in 1995 and the Master of Engineering in Digital Techniques and Instrumentation from Shri Govindram Sakseria Institute of Technology and Science, Indore, Madhya Pradesh, India, in 2003 and PhD in Dynamic testing of an A/D converter in 2010 from RGPV Bhopal, Technical university of M. P., India. His fields of interest are data converter, ADC design- testing and mixed signal VLSI design.

Dr. Deepak Kumar Mishra is a Professor in the E & I Engineering Department at SGSITS, Indore, Madhya Pradesh, India. He has completed his BE in Electronics Engineering in 1979, ME in Applied Electronics and Servo Mechanism in 1984 and PhD in Electronics and Telecommunication Engineering with title 'Some methods for dynamic testing of A/D converters' in May 2000. His areas of interest are Electronics and Instrumentation, VLSI technology and low power analogue and mixed signal VLSI design and dynamic testing of A/D converters.

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