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Design and Implementation of 8-bit Vedic-Wallace Multiplier

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Abstract:
The processors used in the electronic devices spend more time on multiplication operation compared to other arithmetic operations like addition and subtraction. Generally, multiplying two numbers includes basic shift and add operations which are used in Array multipliers. To speed up the multiplication process Conventional Wallace Tree Multiplier (WTM) is used, which is pipelined process and uses carry save adders to decrease the delay. To further increase the speed of the WTM, higher order compressors like 3-2, 4-2, 5-2, 7-2 etc., are used. In this paper we are designing an 8-bit Wallace Multiplier which uses an optimized 4-2 compressor circuit to decrease the power and delay of the multiplier. The design and simulation of the multiplier circuit is done on Tanner EDA tool version 16.0

Key Words: *WTM, Compressor, PPG, PPR, DSP's, HA, FA*

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I. Introduction

Multiplication is one of the fundamental arithmetic operations used in Digital Signal Processors (DSP's) and is also the time-consuming operation. The speed of the DSP's is majorly determined by the speed of multiplication. The multiplier architecture can be divided into three stages, Partial Product Generation (PPG), Partial Product Reduction (PPR) and final stage where we are left with two rows [1].

In recent years, extensive research has been conducted to reduce the multiplier circuit's delay and complexity. The partial products are divided into two rows using the well-known Wallace multiplier's carry save adders, and each column in these two rows is fed to a carry propagate adder to generate the final product [2]. The complexity of the circuit can be reduced by reducing the number of half adders used in the traditional Wallace multiplier, but the number of full adders will be slightly increased [3].

Binary counters using Symmetric stacking are used to decrease power and increase the speed of adding the partial products [4]. Higher-order compressors, such as 4-2, are used to speed up partial product reduction by compressing four inputs into two outputs and at the final stage Sklansky adder is used to produce the product [5]. In each step, the required number of half adders can be used to reduce the width of the carry propagate adder used in the final stage which reduces the multiplier's are [6]. To decrease the delay of the multiplier full adder is realized using mux and XOR gate [7] and to increase the speed of partial product reduction 7-2, 8-2 compressors are used [8, 9].

A new XOR-XNOR logic is used to decrease the critical path delay of 4-2 compressor thus reducing the delay of the multiplier [10], Pass Transistor Logic is used to design the full adder and mux thus reducing the delay and number of transistors used [11] and to decrease the delay and power Gate Diffused Input (GDI) full adder is used for the reduction of partial product [12].

A new multiplier architecture radix-4 Booth Wallace algorithm is used along GDI technique to reduce area, power, and delay [13] and NAND based compressors which uses stacking approach are used to decrease usage of XOR gates thus reducing the critical path delay [14]. To minimize the use of XOR gates and reduce the critical path delay in the 4-2 compressor a logically optimized 4-2 compressor is introduced [15] and use of prefix adder at the final stage instead of ripple carry adder decreases the latency of the multiplier by 66%[1]. A novel hybrid 3-2 counter is designed which uses GDI technique to decrease the power [16].

Wallace multiplier with optimised compressor is simulated in this document. The compressor and its operation are discussed in Section II. In Section III, the 4-2 compressor's Boolean equations and function are discussed. Section IV shows a simulated Wallace multiplier with an optimised compressor circuit. In Section V, the simulation results are compared. The paper comes to an end in Section VI.

II. Compressor

Once you have generated the partial products using AND gates, you must add them in such a way that the addition is faster. One way to make the addition faster is to have the minimal carry propagation, to achieve this we use compressor circuits to compress all the columns in parallel without relying on the result of previous column compressor. The sum and carry can be recombined in the next stage to form the correct result. In the last stage where we are left with two rows, we use carry propagate adder to recombine the sum and carry to generate the result. 3-2 compressor which is nothing, but a full adder is the commonly used compressor which takes three inputs from one column and generate two outputs namely 'sum' and 'Carry'. In the next stage, the sum will be written in the same column, while the carry will be written in the next column. To speed up the reduction process, we use higher order compressors such as 4-2, 5-2, and so on, so that we can compress more bits in each column at the same time.

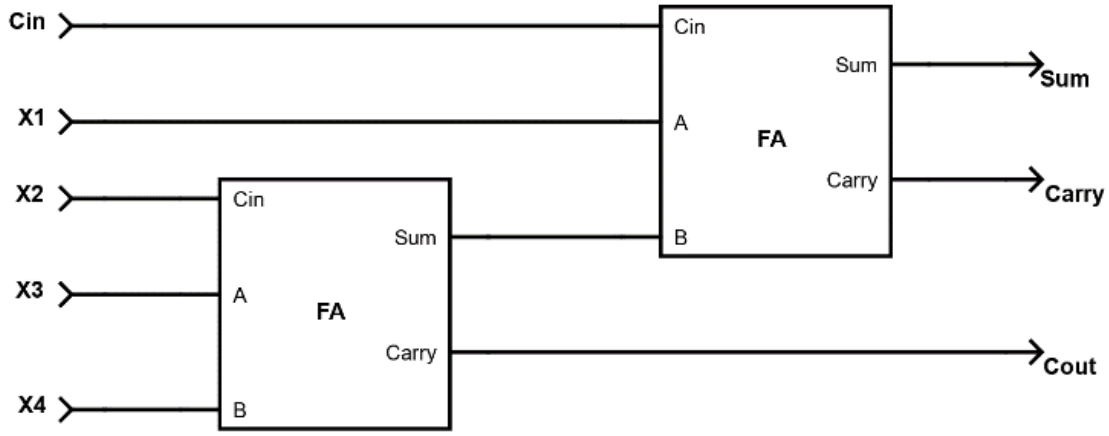

Figure 1. 4-2 Compressor using full adders.

4-2 Compressor

Combinations of full adders may be used to build a traditional 4-2 compressor circuit. Fig. 1 illustrates the data flow from input to output. A 4-2 compressor compresses four inputs plus one carry bit 'Cin' from the previous column into two outputs 'Sum' and 'Carry' plus one intermediate carry bit 'Cout' that is provided as Cin to the next column, as the name implies. The 4-2 compressor's input and output relationship can be expressed mathematically as

$$C_{in}+X_4+X_3+X_2+X_1 = Sum+2(Carry+C_{out})$$

As shown in Fig. 1, implementing a 4-2 compressor using basic cascading of full adders introduces a critical path delay of four XOR gates. As shown in Fig. 2, logical optimization reduces the critical path delay to three XOR gates, and this 4-2 compressor is considered a traditional model. The traditional 4-2 compressor's Boolean equations are as follows:

$$Sum = C_{in}\ X_4\ X_3\ X_2\ X_1$$
$$Carry = (X_4\ X_3\ X_2\ X_1)C_{in} + (X_4\ X_3\ X_2\ X_1)X_4$$
$$C_{out} = (X_2\ X_1)X_3 + (X_2\ X_1)X_1$$

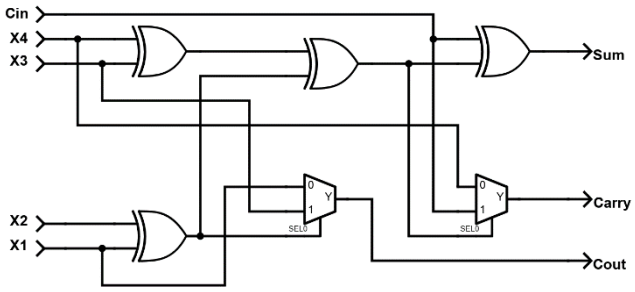

Figure 2. 4-2 Compressor using three XOR gates.

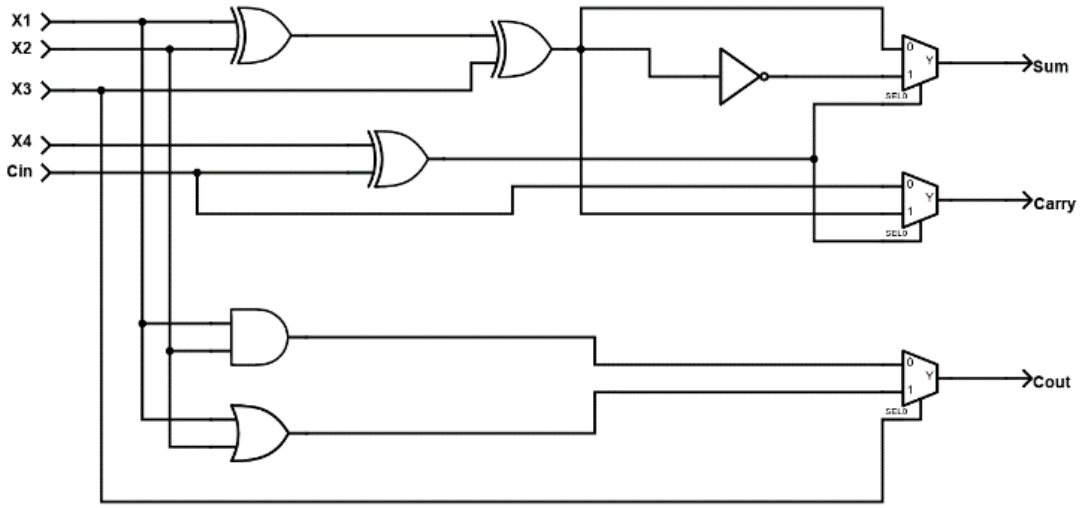

Figure 3. 4-2 Compressor used in this paper.

From the above Boolean equations, as Cout is independent of Cin parallelism among each column in compressor can be ensured. From the truth table deriving new Boolean equations or rearranging the existing equations plays primary role in the design of any digital circuit. The XOR gates of the 'Sum' generation specify the critical path delay of a traditional 4-2 compressor. Since it is provided to the next adjacent compressor, 'Cout' should be produced faster because it is independent of 'Cin.' The critical path delay is often characterized by 'Cout' in most multiplier architectures that use compressors. So, faster generation of 'Sum' and 'Carry' is crucial for faster multiplication operation.

The compressor used in this paper uses the fewest XOR gates possible since XOR gates cause more delay and using MUX logic over XOR logic reduces delay. The following are the Boolean equations obtained from the 4-2 compressor's truth table [17]:

$$Sum = (X_4C_{in})(X_1X_2X_3) + (X_4C_{in})\,(X_1X_2X_3)$$
$$Carry = (X_4C_{in})\,(X_1X_2X_3) + (X_4C_{in})\,C_{in}$$
$$C_{out} = X_3(X_1+X_2) + X_3(X_1.X_2)$$

From the above equations we can observe that 'C_{out}' is independent of 'C_{in}' which is crucial and we have used MUX logic over XOR logic to decrease the delay.

III. Wallace Multiplier

The multiplier designed using Wallace algorithm is called Wallace multiplier. The switching speeds of Wallace multiplier is faster compared to other multipliers. As researchers are interested in this multiplier better designs of Wallace multiplier are introduced one such is the use of higher order compressors. Wallace multiplier algorithm is the fastest column compression technique used in multiplication of unsigned number as the delay of this multiplier varies logarithmically with the size of the input. In this algorithm mainly three steps are involved:

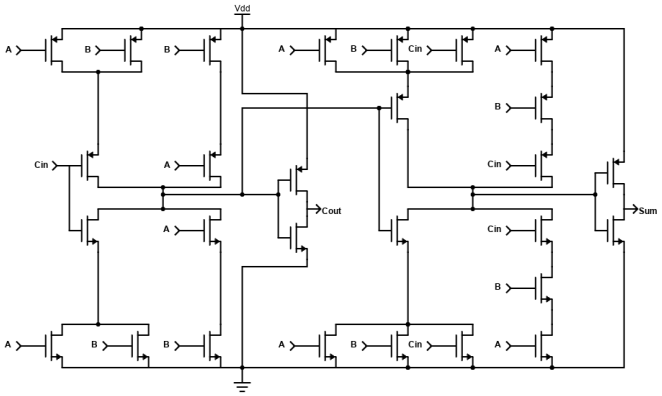

Figure 4. 28 Transistor Full Adder.

- Partial Product Generation (PPG)
- Partial Product Reduction (PPR)
- Partial Product Addition (PPA)

An AND gate array is used to create partial products. The reduction of partial products in a traditional Wallace multiplier is accomplished by connecting a group of "Half Adders" and "Full Adders" using the carry-save technique. At the end of the process, partial products are reduced until there are just two rows remaining. To get the product, these two rows are fed into a carry-propagate adder. The cascading of 'Full Adders' is used to create the carry-propagate adder used in the final step.

The multiplication process is carried as follows:

- The binary representation of the two unsigned numbers is given to the AND gate array which will then generate the partial products.
- For simplicity, the generated partial products are arranged in a tree like structure. Now the eight rows are divided into two stages each stage having four rows.
- Half adders, full adders, and 4-2 compressors are used to reduce partial products. The generated 'sum' is written in the same column, while 'carry' is written in the next column down.
- In the latter stages the 'sum' and 'carry' are also grouped using 'HA', 'FA' and '4-2 Compressor'.
- The reduction continued until we are left with two rows. When we are left with two rows, we use a simple carry-propagate adder to produce the result.

The sub-circuits we have used to design multiplier are 'AND', 'NAND', 'OR' and 'XOR' gates, 'FA', 'HA', 'MUX', and 'COMPRESSOR' circuits. The simulated multiplier circuit is shown in the Fig. 5.

IV. Simulation Results

The multiplier is simulated in Tanner EDA tool using 65nm BPTM technology model file. We have used A=0000_1111 and B=0000_0111 as inputs to the multiplier circuit and V_{dd} = 1V. The corresponding outputs are shown in Fig. 6a to 6d.

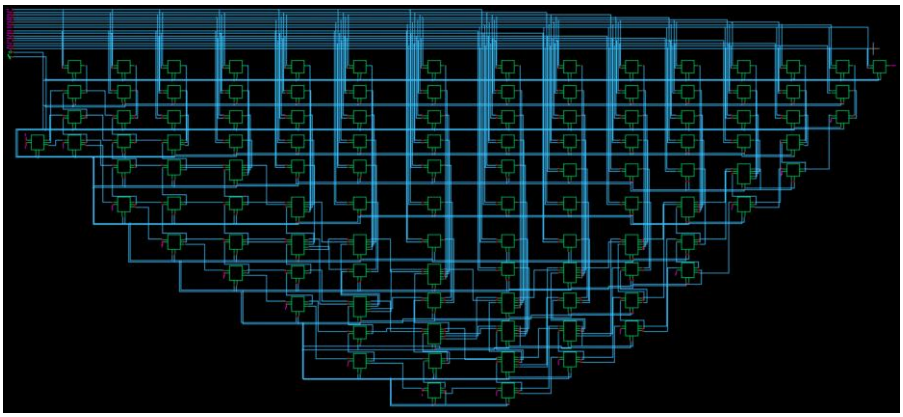

Figure 5. Simulated multiplier circuit.

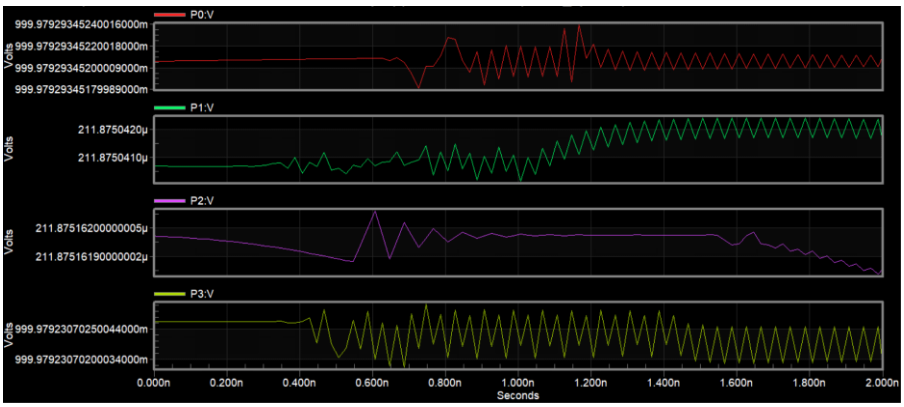

Figure 6a. Output P0-P3

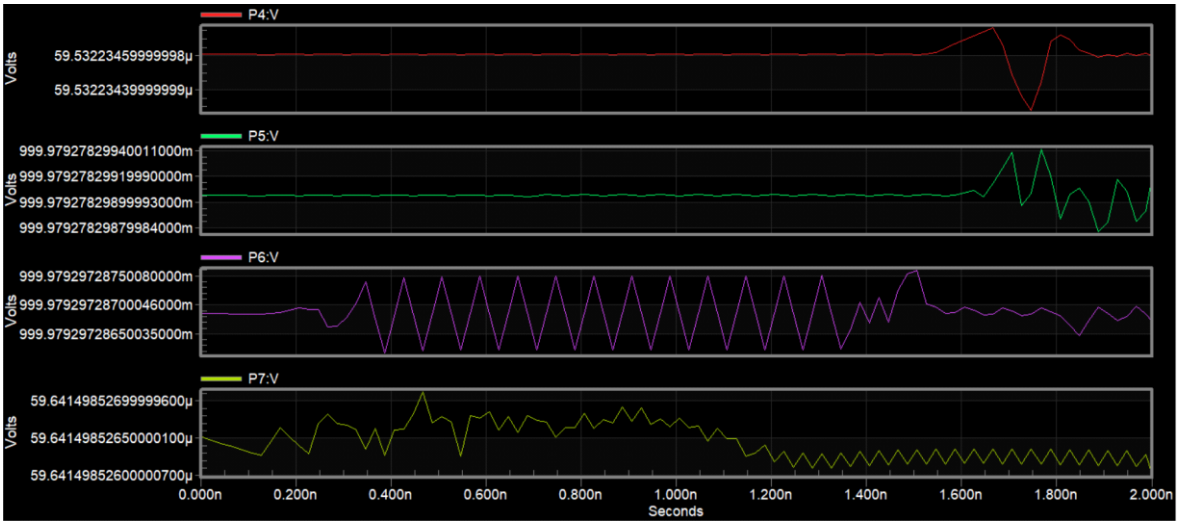

Figure 6b. Output P4-P7

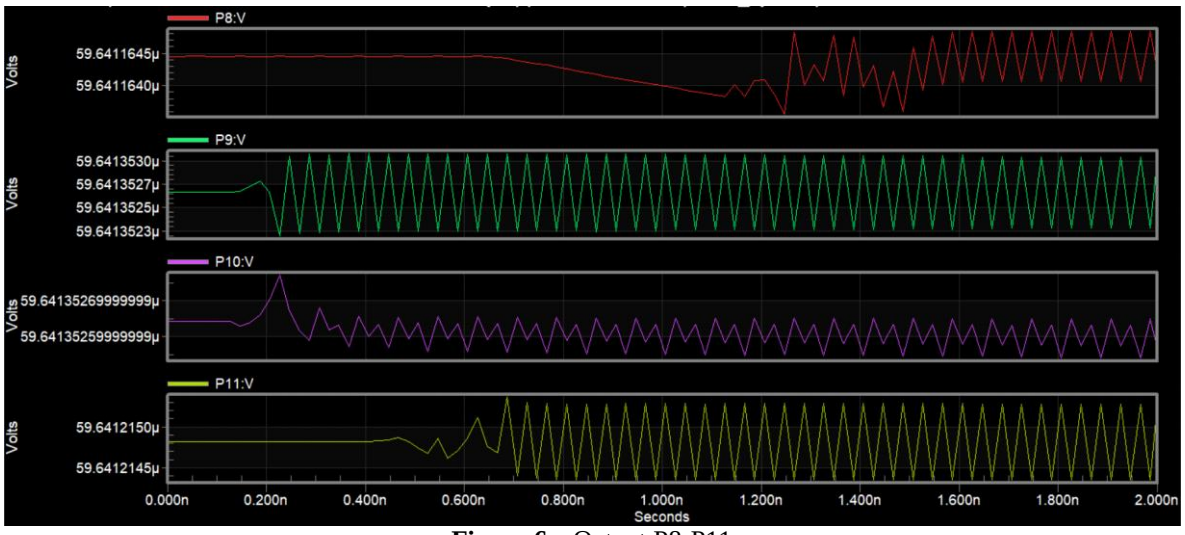

Figure 6c. Output P8-P11

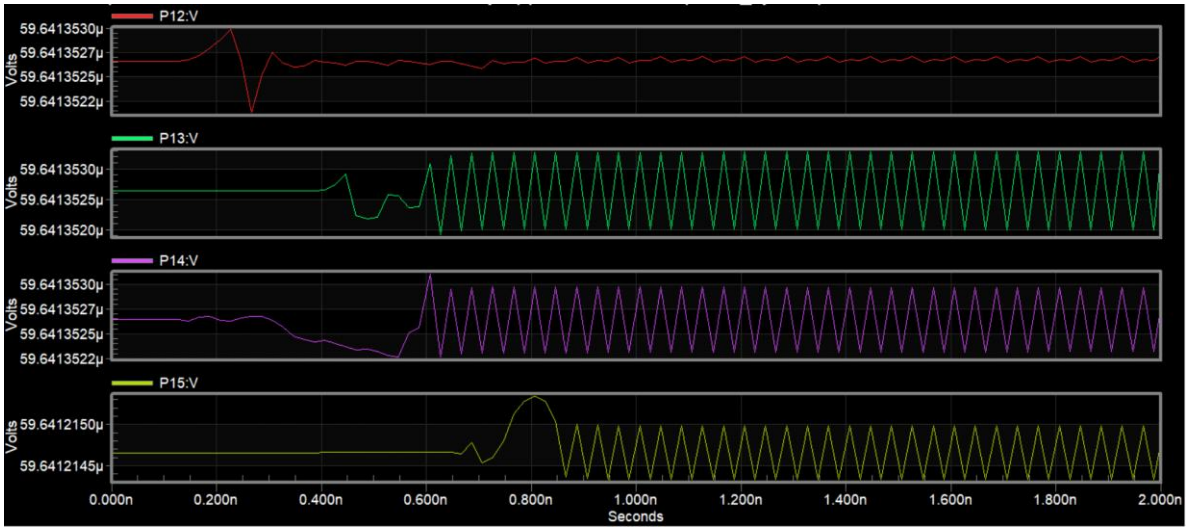

Figure 6d. Output P12-P15

Table no 1: Comparison of performance.

Multipliers	Power (µW)	Delay (ns)	Power Delay Product (fJ)
Proposed Wallace Multiplier	I) 10.5	I) 2.367	I) 0.02485
Vedic Multiplication algorithm [17]	69.1	100.1	6.91691
Vedic Multiplier using compressors [18]	521.38	2.962	1.54432
4-bit Wallace Multiplier hybrid 3-2 counter [19]	21.81	0.244	0.00517

V. Conclusion

The simulation results of the multiplier show decrease in both average power consumption and PDP which means that the proposed multiplier is energy efficient. As for the future work one can write switch-level Verilog code for the circuits and synthesize it or can burn the netlist on the FPGA for prototype implementation. We can also develop layout of the multiplier circuit using MTCMOS technique to decrease the OFF current in Cadence or Synopsys IC compiler.

References

[1]. U. Kumar and A. Fam, "Enhanced Wallace Tree Multiplier via a Prefix Adder," 2020 IEEE Student Conference on Research and Development (SCOReD), Batu Pahat, Malaysia, 2020, pp. 211-216.

[2]. C. S. Wallace, "A Suggestion for a Fast Multiplier," in IEEE Transactions on Electronic Computers, vol. EC-13, no. 1, pp. 14-17, Feb. 1964.

[3]. R. S. Waters and E. E. Swartzlander, "A Reduced Complexity Wallace Multiplier Reduction," in IEEE Transactions on Computers, vol. 59, no. 8, pp. 1134-1137, Aug. 2010.

[4]. C. Fritz and A. T. Fam, "Fast Binary Counters Based on Symmetric Stacking," in IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol. 25, no. 10, pp. 2971-2975, Oct. 2017.

[5]. K. Gopi Krishna, B. Santhosh, and V. Sridhar, "Design of Wallace Tree Multiplier using Compressors," in International Journal of Engineering Sciences & Research Technology, vol. 2, no. 9, pp. 2249-2254, Sept. 2013.

[6]. Shahzad Asif and Yinan Kong, "Low-Area Wallace Multiplier," in Hindawi Publishing Corporation, VLSI Design, Australia, vol. 2014, pp. 1-6.

[7]. K. B. Jaiswal, Nithish Kumar V, P. Seshadri and Lakshminarayanan G, "Low power Wallace tree multiplier using modified full adder," 2015 3rd International Conference on Signal Processing, Communication and Networking (ICSCN), Chennai, India, 2015, pp. 1-4.

[8]. Jinimol P George and Ramesh P, "Wallace Tree Multiplier using Compressor," in International Journal of Current Engineering and Technology, vol. 5, no. 3, pp. 1934-1938, 2015.

[9]. Rao, E & Kondapalli, Jayaram Kumar & Prasad, "Design of high speed Wallace tree multiplier using 8-2 and 4-2 adder compressors," in International Journal of Engineering & Technology, vol. 7, no. 4, pp. 2386-2390, 2018.

[10]. Kumar, Manish & Nath, Jonali, "Design of an Energy Efficient 4-2 Compressor," in IOP Conference Series: Materials Science and Engineering, pp. 1-8, 2017.

[11]. Janveja, Meenali & Niranjan, Vandana, "High Performance Wallace Tree Multiplier Using Improved Adder," in ICTACT Journal on Microelectronics, vol. 3, no. 1, pp. 370-374, Apr. 2017.

[12]. K. R. Kumar, "A Novel Approach to Design Area Optimized, Energy Efficient and High Speed Wallace-Tree Multiplier Using GDI Based Full Adder," 2017 IEEE International Conference on Computational Intelligence and Computing Research (ICCIC), Coimbatore, India, 2017, pp. 1-4.

[13]. B. Mukherjee and A. Ghosal, "Design and Analysis of a Low Power High-Performance GDI based Radix 4 Multiplier Using Modified Booth Wallace Algorithm," 2018 IEEE Electron Devices Kolkata Conference (EDKCON), Kolkata, India, 2018, pp. 247-251.

[14]. T. Satish and K. S. Pande, "Multiplier Using NAND Based Compressors," 2019 3rd International Conference on Electronics, Materials Engineering & Nano-Technology (IEMENTech), Kolkata, India, 2019, pp. 1-6.

[15]. M. Priyadharshni, Anishchandran Chathalingathu, S. Kumaravel, Arun Manoharan, Sreehari Veeramachaneni, Sk Noor Mahammad, "Logically Optimal Novel 4-2 Compressor Architectures for High-Performance Applications" 2019 Arabian Journal for Science and Engineering (AJSE), pp. 6199-6209.

[16]. Senthilkumar, V.M & Sowmiya, S & Stella. K, "Design and analysis of 4-2 compressor for arithmetic application," 2017, vol. 1, no. 1, pp. 106-109.

[17]. K. Dey and S. Chattopadhyay, "Design of high performance 8 bit binary multiplier using Vedic multiplication algorithm with 16 nm technology," 2017 1st International Conference on Electronics, Materials Engineering and Nano-Technology (IEMENTech), Kolkata, 2017, pp. 1-5, doi: 10.1109/IEMENTECH.2017.8076956.

[18]. H. Kaur and N. R. Prakash, "Area-efficient low PDP 8-bit Vedic multiplier design using compressors," 2015 2nd International Conference on Recent Advances in Engineering & Computational Sciences (RAECS), Chandigarh, India, 2015, pp. 1-4, doi: 10.1109/RAECS.2015.7453395.

[19]. B. C. Devnath, S. N. Biswas and M. R. Datta, "4-bit Wallace and Dadda Multiplier design using novel hybrid 3-2 Counter," 2020 2nd International Conference on Advanced Information and Communication Technology (ICAICT), Dhaka, Bangladesh, 2020, pp. 189-194.