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Design, Simulation, and Analysis of Different Operational Factors of a 4-bit Carry Look-Ahead Adder Circuit in Microwind at Several CMOS Technology Nodes

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Abstract:
In Very Large Scale Integration (VLSI) technology, the main objective is to shrink the area and thereby to raise the packing density for performance improvement in terms of power consumption, noise, delay, operating frequency, etc. A carry look-ahead adder circuit is an important block in any digital circuit. It improves the parallel addition process. Since the number of bits in various digital circuits is being increased, as such, we need millions of transistors to perform several functions in parallel. But it increases the need for surface area, power consumption, noise, and other factors. Therefore, we need to reduce the transistor size to alleviate these problems. In this research article, we designed a 4-bit carry look ahead full adder circuit at several technology nodes using Proteus and then simulated it in Microwind. The designed circuit and layout are presented here. Besides, various operational factors are obtained to observe the benefits of the transistors' size decrement. The layouts are converted and simulated at130 nm, 90nm, 65nm, and45nm CMOS technology nodes. From the comparative analysis, we observed that the reduction of CMOS technology node increases the performance factors of the designed carry look-ahead adder circuit.

Key Words*: CMOS; Carry Look Ahead (CLA)Full Adder; Technology Node; VLSI; Area; Power Consumption; Noise; Delay.*

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I. Introduction

Various types of binary logic circuits are used in various integrated chips in many applications as electronic computing and portable devices [1]. In the VLSI circuits, to perform the arithmetic operations, we need the binary adder circuit [2]. A single-bit full adder circuit is the elementary building block [3] from which we can have multi-bit adder circuits. The multi-bit circuits increase the surface area, power consumption, and propagation delay, noises, etc.[4-9]. However, the circuit designers want to retain these parameters constant or reduce them to augment the circuit performance eventually. Therefore, we need to shorten the transistor's size further to have a higher packing density as well [10].

In an adder circuit, two numbers are added, one is termed as augend and the other one is known as an addend. After the addition, they produce two more numbers that are called sum and carry. The number of bits of the sum is equal to that of either augend or addend though the carry has only one bit. It is to be ensured that the current bit position of an augend must be added with the current bit position of an addend and the output carry of that position must be added as the input carry of the next bit position. That is for a multi-bit adder circuit the addition of a particular bit position of the augend and addend yields a sum bit and a carry bit for their next bit positions [11].

Binary adder circuits are designed and implemented based on diverse logic families, such as Transistor-Transistor Logic (TTL), Complementary Metal Oxide Semiconductor (CMOS) logic [12], High Threshold Logic (HTL), Gate Diffusion Input (GDI) logic, Transmission Gate Logic (TGL), Bipolar CMOS (BiCMOS) logic [13-14], CMOS/BiCMOS logic [15], Emitter Coupled Logic (ECL) circuit [16] and so on. In each logic family, there are various architectures of such circuits.CMOS is a commonly used technology due to its high speed, low power consumption, and compactness [12, 17]. This technology facilitates the scaling down of its node for performance improvement [10]. As such, we have chosen CMOS based logic circuit and want to study comparatively various performance factors mentioned earlier as the technology node is scaled down from 130 nm to 32 nm.

Currently, the available technology nodes are 130, 90 nm, 65 nm, 45 nm, 32 nm, 22 nm, 14 nm, and so on due to continuous scaling down of the MOS transistor dimensions and other parameters [10, 18]. Most of

these technology nodes are available in Microwind software [19-20]. CMOS-based full adders are employed in manufacturing communication circuits and multi-media processors [21]. In this article, we designed a 4-bit carry look-ahead adder circuit at various technology nodes and then simulated the circuit to get various outputs. We found out the various operational and design parameters of the circuit at these various nodes.

II. Literature Review and Problem Statement

All the semiconductor industries around the globe want the semiconductor designers to improve the circuit performance by scaling down the transistor sizes and voltage levels of the circuit that ultimately reduce the surface area, power consumption, propagation delay, noise and expatiate the operating frequency range or speed of operation and packing density of the circuit [10]. In CMOS technology, when the device dimensions and supply voltage are reduced then threshold voltage also goes down [18]. However, the threshold voltage reduction causes an increase in the sub-threshold current during the off-state of the transistor due to surface potential lowering [22-24] and thereby, increases off-state power consumption significantly [25].

By doing a literature review, we have studied several research articles on CMOS-based adder circuit design. CMOS-based NAND gates were used to design a 2-bit parallel binary adder circuit using Microwind and DSch software [26]. In another article, speed and power consumption minimization issues were addressed for the VLSI binary adder circuits [27].

Various adder topologies, viz. ripple carry adder, carry look-ahead adder, carry skip adder, carry select adder, carry increment adder, carry-save adder, and carry bypass adder were analyzed based on their various performance factors in the Microwind simulation environment at 120 nm CMOS technology node. According to their simulation results, they concluded that the carry look-ahead adder circuit is one of the best performing circuits among various topologies in terms of the area occupancy, propagation delay, and power dissipation, and as such it meets the requirements of its application in the other complex circuits [28].

Then in 2015, a 90 nm CMOS technology node-based4-bit full adder circuit was analyzed and compared between the semi-custom and full automatic layout design through simulations. This analysis shows that the semi-custom design cansave72%silicon area as compared to the full-automatic design [29].

In another article published recently, Ripple Carry Adder (RCA) circuit was designed in DSch and then simulated in Microwind at various technology nodes and compared the results in terms of its performance parameters and was found that the lower technology node provides better performances [30]. However, Ripple Carry Adder (RCA) circuit has a higher propagation delay even at the lower technology node. Its value depends on the number of 1-bit full adder circuit block's propagation delay [31]. Proteus is a kind of software that is used to model and simulate virtual circuits and systems. This tool is used mainly for electronic design automation. It is combined with the SPICE circuit simulation software so that circuits or models may be simulated at both platforms simultaneously. The electronic design engineers used it to design and draw the schematic diagrams and printed circuit boards for design verification before going into its industrial production. It can provide practical outputs through simulations [32]. Therefore, in this work, we have selected Carry Look Ahead Adder (CLA) circuit to design in Proteus and then simulate in Microwind at various technology nodes to compare its various performance parameters.

III. Full Adder Design

A ripple carry full adder circuit adds two numbers and produces two outputs-sum and carry. If there are three single-bit inputs, *A*, *B*, $C_{in,}$ and the sum and carry outputs are *S* and C_{out} then the output expressions are given by the following two Boolean formulas [30].

$S = (A \oplus B) \oplus C_{in}$

$C_{out} = AB + C_{in}(A \oplus B)$

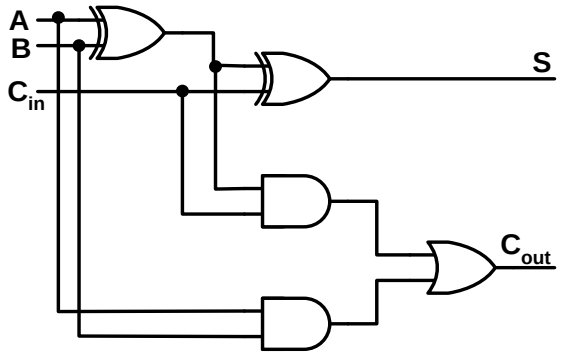

Figure 1. A single bit full adder unit cell using logic gates [30]

The logic gate-based diagram of a single-bit adder circuit is depicted in Fig. 1. Here we used the XOR, AND, and OR logic gates to implement the adder circuit. From this logic circuit, we find that the sum (S) output needs delays through the two XOR gates and the output carry (C_{out}) needs delays through the AND and OR gates. Since the propagation delays of XOR, AND, and OR logic gates are not identical and hence the circuit delay for these two outputs may not be equal. This circuit for single-bit addition is considered as a unit cell to produce an n-bit adder circuit by copying it n-times.

That is, here the input carry depends on the output carry generation of the previous cell or block. However, for the Carry Look Ahead Adder (CLA) circuit, the carry-in bits of each cell need not wait for the computation of the output carry of the previous cell. This is accomplished by defining each carry-in bit from the combination of the inputs of the previous cells and the computations of the previous carry-in bits. That is, in CLA, a carry-out bit for a particular cell is produced by generating and propagating carries for the successive carry-in bits. The carry generation bit for the i^{th} cell is formed by the AND operation of the two i^{th} inputs of the same cell as shown by the following Boolean expression. Here, i indicates integer numbers, like 0, 1, 2, and 3.

$G_i = A_iB_i$

The carry propagation bit for the i^{th} cell is formed by the OR operation of the two i^{th} inputs of the same cell as shown by the following Boolean expression.

$P_i = A_i + B_i$

Finally, the carry-in bit for the $(i+1)^{th}$ cell is formulated by using the carry generation and carry propagation as well as the carry-in bit of the i^{th} cell as shown by the following Boolean expression.

$C_{i+1} = G_i + P_iC_i$

In this work, we have designed a 4-bit carry look-ahead adder circuit, that is each input A and $B$are of 4 bits, likeA_0, A_1, A_2, A_3, andB_0, B_1, B_2, B_3, but carry input is of1 bit, i.e., C_{in}. Therefore, the sum output is also of 4 bits likeS_0, S_1, S_2, $S_3$and the carry output is of 1 bit, i.e., C_{out}.

Therefore, the carry-in bits for the four cells of the CLA adder circuit would be expressed by the following four Boolean expressions respectively.

$C_0 = C_{in}$

$C_1 = G_0 + P_0C_0 = A_0B_0 + (A_0 + B_0)C_0$

$C_2 = G_1 + P_1C_1 = A_1B_1 + (A_1 + B_1)C_1$

$C_3 = G_2 + P_2C_2 = A_2B_2 + (A_2 + B_2)C_2$

$C_{out} = G_3 + P_3C_3 = A_3B_3 + (A_3 + B_3)C_3$

A block diagram of a 4-bit Carry Look Ahead adder circuit is depicted in Fig. 2. In this diagram, we used four unit cells of Fig. 1.

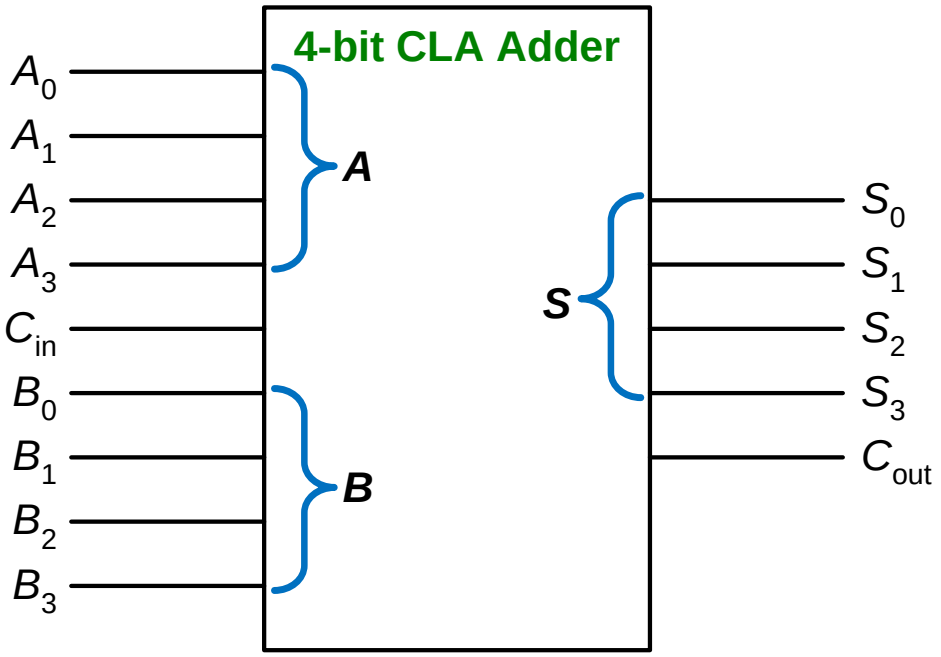

Figure 2. Block diagram representation of a 4-bit CLA adder circuit

The truth table of the 4-bit carry look ahead full adder circuit is presented in Table 1.

Table 1. The truth table of the 4-bit full adder circuit

C_{i-1}	A_i	B_i	S_i	C_i
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

The detailed schematic block diagram of the CLA adder circuit is shown in Fig. 3. In the first block of the CLA full adder circuit (CLA FA_0), A_0, B_0, and C_{in} are the input bits, and this block yield S_0, G_0, and P_0output bits. S_0possessesthe least significant bit (LSB) position of the 4-bit sum output. In the carry generation (CG) and carry propagation (CP) block, G_0, and P_0, and C_{in} together produces the carry-in (C_1) for the next block. In the second CLA full adder circuit block (CLA FA_1), the input bits A_1, B_1, and C_1 produce the output bits S_1, G_1, and P_1. Then in the carry generation and propagation block, G_1, and P_1, and C_1 produce the carry-in (C_2) for the next block, and in a similar fashion S_2, G_2, and $P_2$and finally, S_3, G_3, and P_3as well as C_{out} are created as the output bits by the third and fourth blocks respectively. S_3 possesses the most significant bit (MSB) position of the 4-bit sum output.

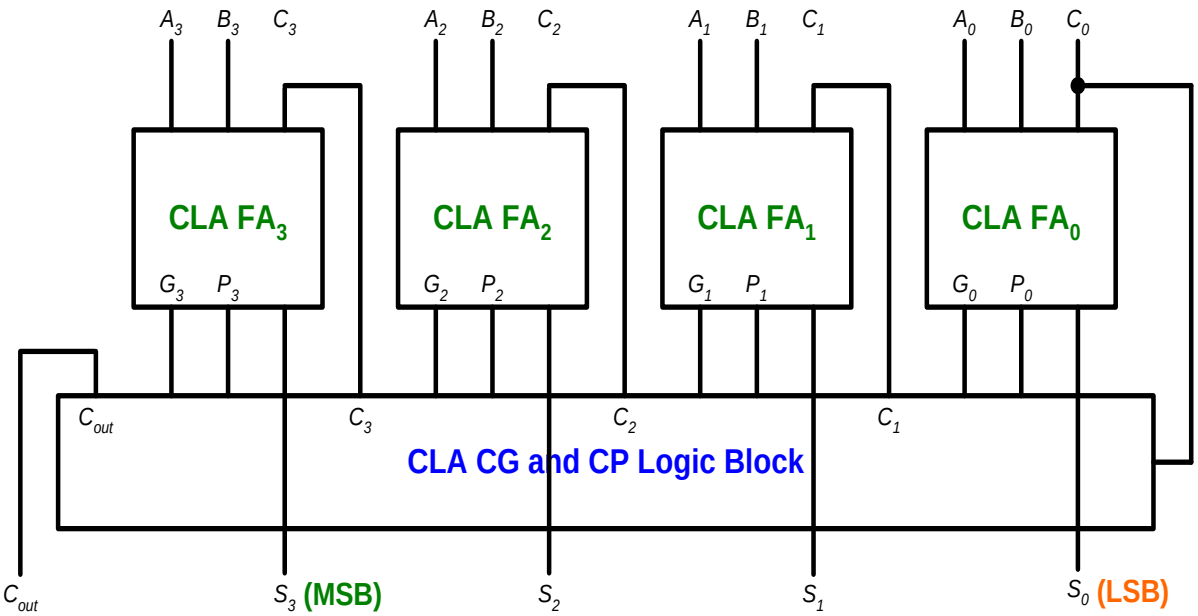

Figure 3. The detailed schematic block diagram of the 4-bit CLA adder circuit

To implement the CLA full adder circuits we need XOR, AND, and OR gates but to implement the CLA CG and CP logic block, we need AND and OR gates only. These logic gates should be designed using CMOS, that is, to design a transistor-level diagram, we need both NMOS and PMOS transistors. AND and OR gates are the basic logic gates and hence we may derive them using NMOS and PMOS. However, CMOS generates inverted output for the AND and OR gates. That is, we can design NAND and NOR gates instead. However, if we design a NOT gate using a single transistor and connect it at the output of these two gates then we can easily get the AND and OR operations. On the other hand, the XOR gate is a compound gate and may be derived from the NAND gates. As a result, if we design and implement the transistor-level circuits of three basic logic gates (AND, OR, and NOT) then combining these gates, we can design the complete CLA full adder circuit. A gate-level circuit design is shown in Fig. 4. In this gate-level diagram, we observe that basic AND, OR, and XOR gates are used. These gates can be implemented in any technology at the transistor level, like NMOS, CMOS, TTL, BiCMOS, etc. However, the CMOS technology is one of the most preferred technologies

for this purpose due to its numerous advantages, such as scalability, low power consumption, high noise immunity, high packing density, availability of technology, etc. [10].

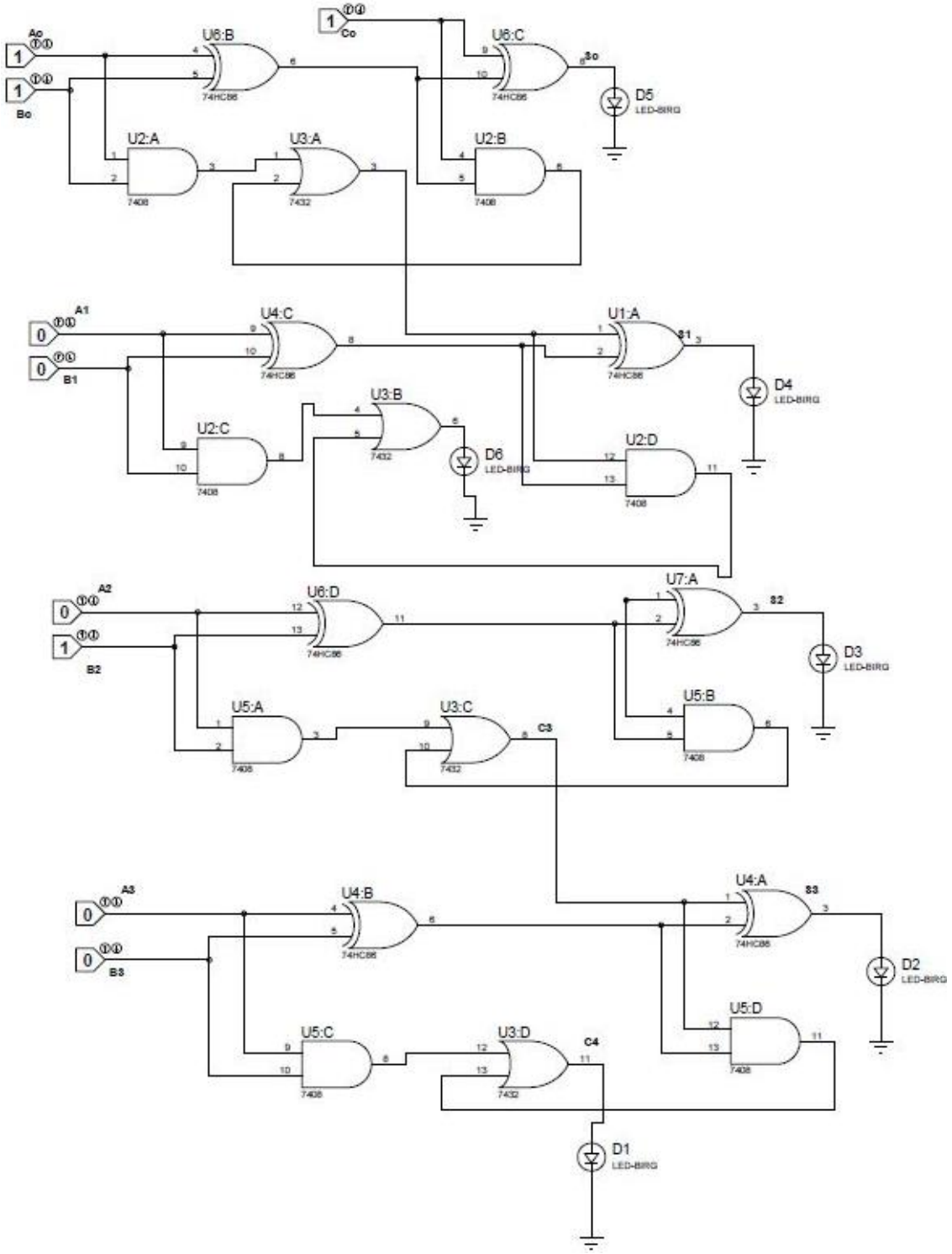

Figure 4. CMOS full carry look-ahead adder's gate-level circuit designed at120 nm technology node

If we intend to design these using CMOS technology then we have to choose a particular value of the channel length of both NMOS and PMOS transistors. This is called a technology node. Usually, the lengths of both NMOS and PMOS transistors remain the same but the width of the PMOS transistor is greater than the NMOS transistor. In Figs. 5 (a), (b), and (c), we have shown the transistor-level circuits of the three basic logic gates, AND, OR, and NOT gates respectively. From these three basic logic gates, we can construct other logic gates like NAND, NOR, XOR, XNOR, etc. as well. Then we may repeat these transistor-level circuits to

generate the complete 4-bit CMOS-based full carry look-ahead adder circuit. Hence, the NMOS and PMOS transistor is the basic building block of digital circuits.

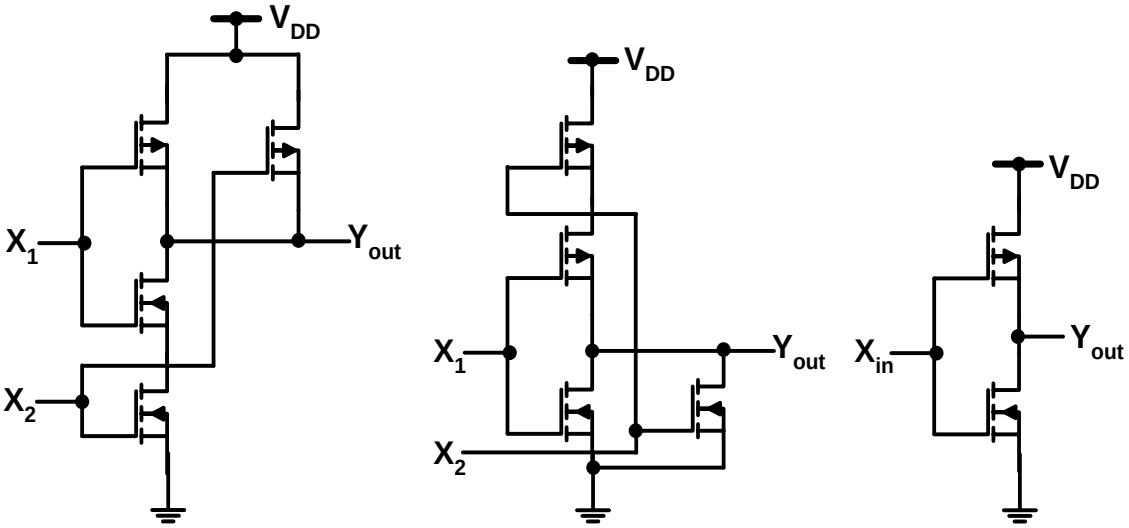

Figure 5. MOS transistor-level circuit diagram of the logic gates (a) AND gate, (b) OR gate, (c) NOT gate

IV. Results and Discussions

A portion of the transistor-level design of the 4-bit CLA full adder circuit is shown in Fig. 6 using 120 nm technology nodes in Proteus. However, the actual length is 130 nm. The total length (L) of the designed layout of the circuit is 130λ, that is 50×65= 8450 nm = 8.45 μm (since $\lambda = L/2$). The width of the NMOS transistor is 100 nm and that of the PMOS transistor is 200 nm. Since this is a CMOS circuit, as a result, there must be an equal number of NMOS and PMOS transistors in the circuit.

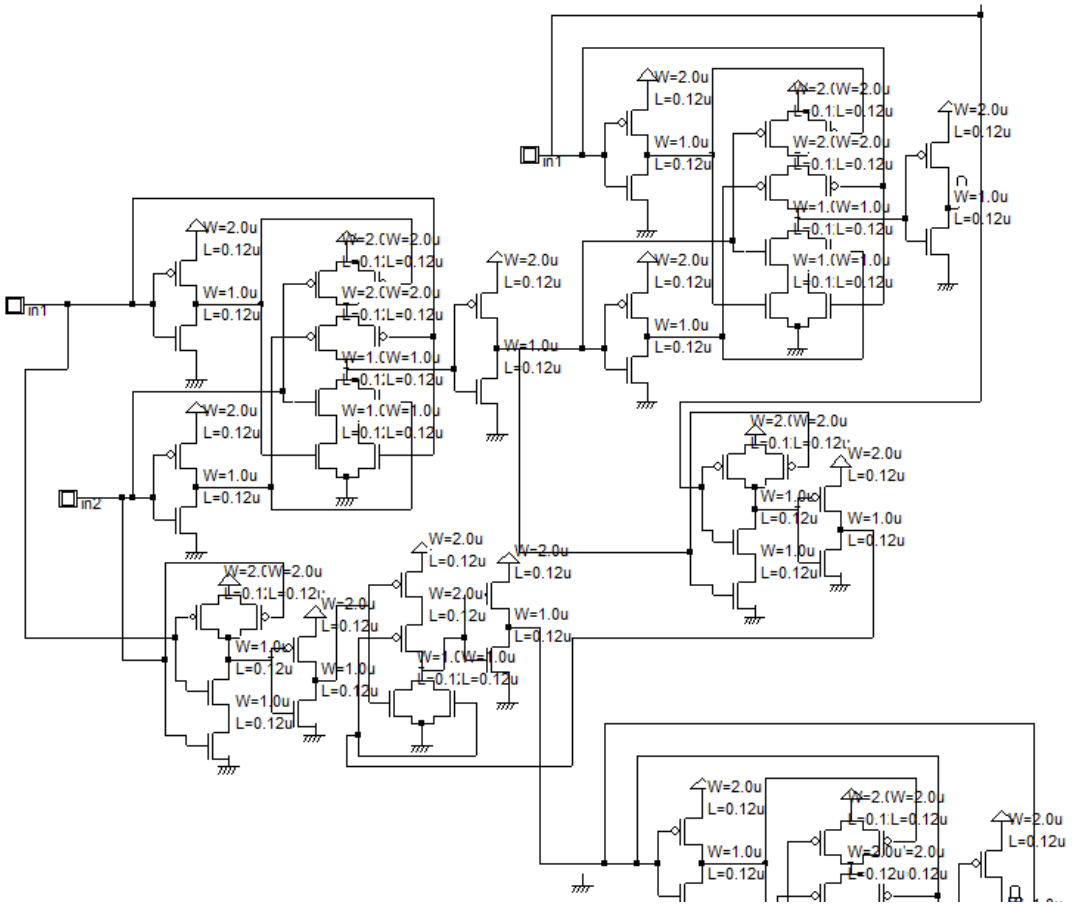

Figure 6. CMOS full carry look ahead adder's transistor level circuit designed at 120 nm technology node

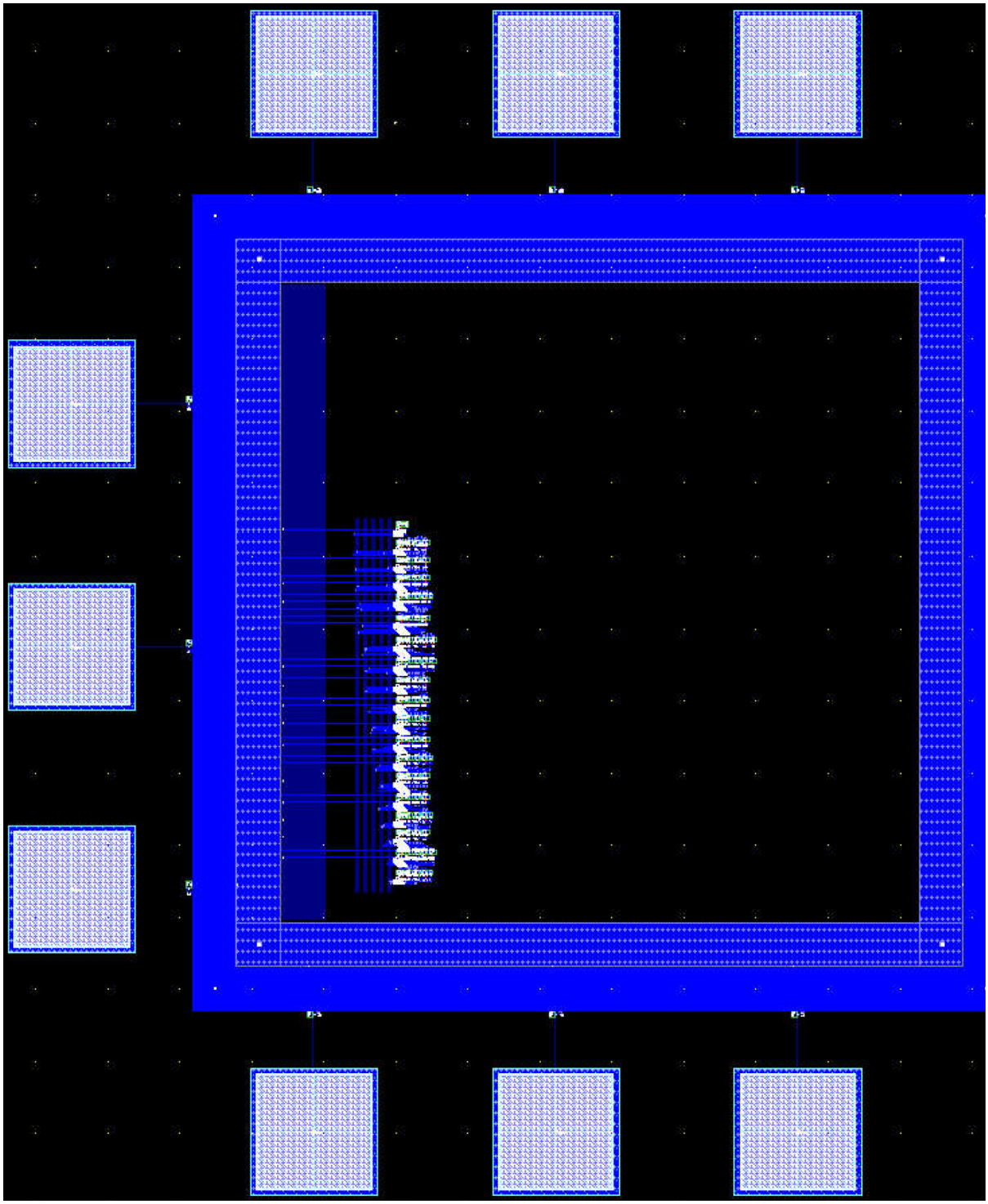

Figure 7. A portion of CMOS layout design for a 4-bit full adder circuit at 90 nm technology node

The layout of the designed carry look ahead full adder circuit using CMOS 90nm technology in Microwind environment is demonstrated in Fig. 7. It is extracted from the transistor-level designed circuit. In this process, 6copper metal layers are used with 2 types of the polysilicon layer, one type of p^+ diffusion layer, and one type of n^+ diffusion layer as well as an n-well. T simulate the designed circuit, the low and high-level voltages used here are 0.2 V and 1.8 V respectively for binary 0 and 1. The operating temperature is 27°C and the noise input is 0.1 V (rms). The threshold voltage of an NMOS transistor was 0.34 V.

To verify the designed transistor's working principle at 120nm node, the characteristics curves of each type of transistor are simulated. One such curve (I_{ds}-V_{ds} characteristics) for an NMOS transistor is revealed in Fig. 8. The transistor's threshold voltage (V_{th}) is 0.34 V, width (W) is 200 nm, and oxide thickness (t_{ox}) is 1.2

nm. The operating temperature during simulation time is 27^0C, and the propagation delay was only 0.14 ns. The maximum current drawn by the circuit is $I_{dd,max}$ = 455 µA, and the average current drawn is 43 µA.

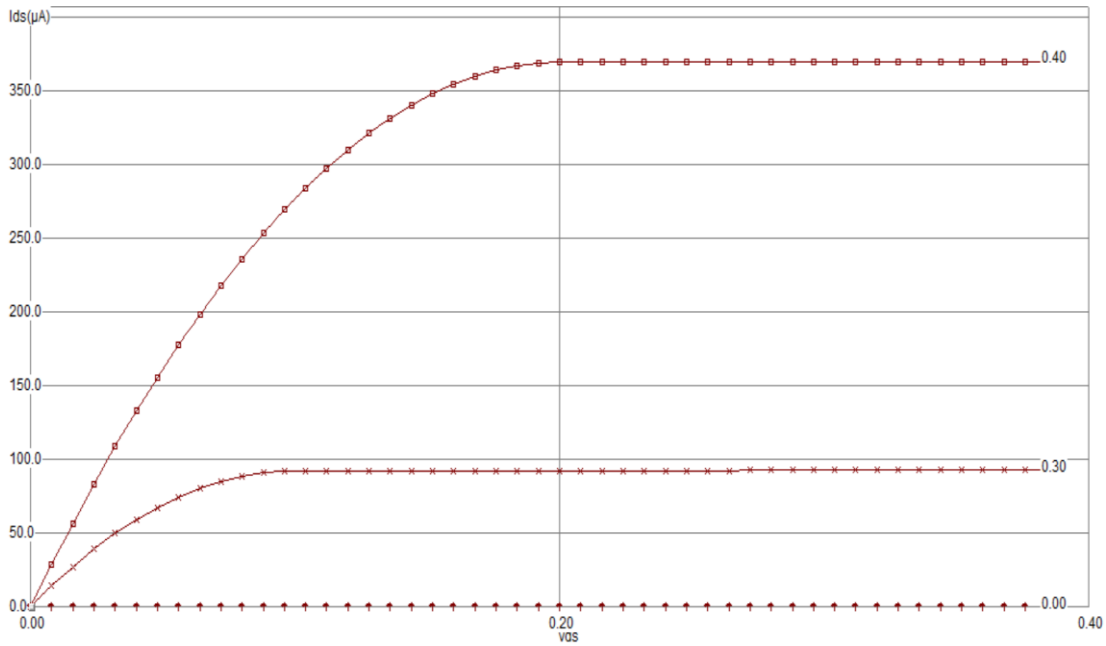

Figure 8. Output characteristics curves for an NMOS transistor at 90nm technology node

A part of the timing simulation from 1057 ns to 2657 ns is shown in Fig. 9 for the 4-bit carry look ahead full adder circuit. There are two 4-bit and one 1-bit input as well as one 4-bit and one 1-bit output. That is, there are a total of 14 single-bit lines in the simulation diagram. The timing states of the output lines changed as per input signals.

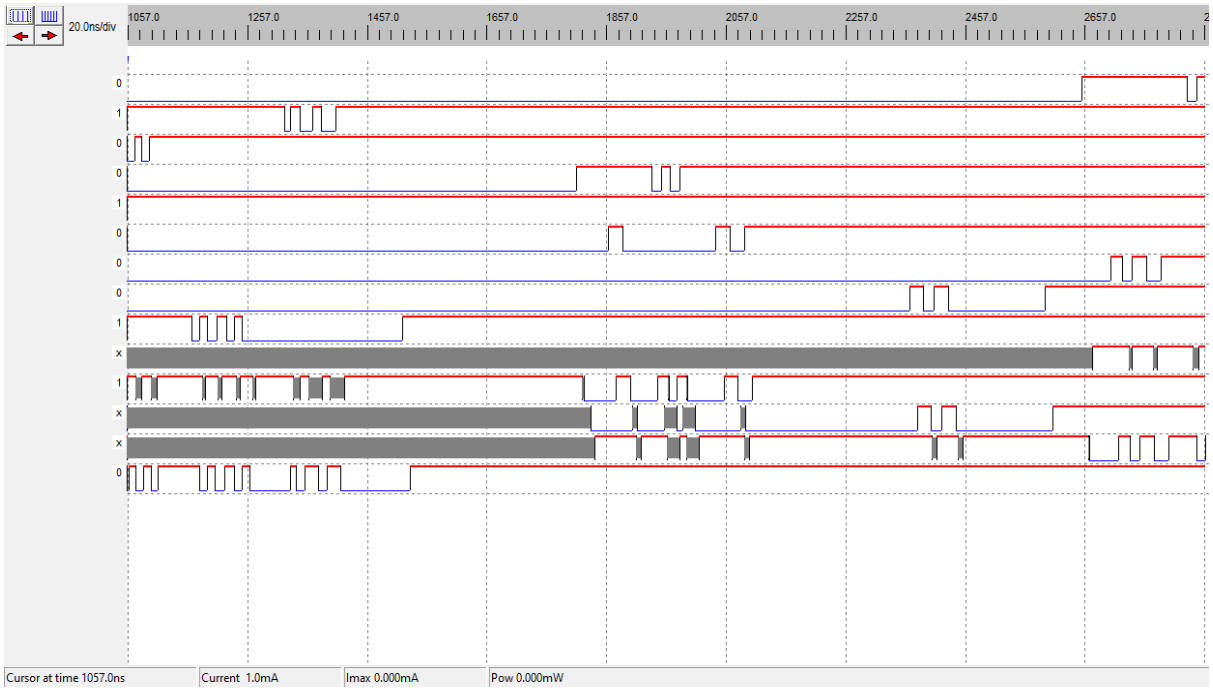

Figure 9. Timing simulation of a 4-bit carry look-ahead full adder circuit at 90 nm technology node

A part of the 3-D CMOS-based layout design of our 4-bit CLA full adder circuit is shown in Fig. 10. The gate capacitance at 120 nm was found as 2.5 fF and the drain capacitance was 0.25 fF at threshold condition at the 90 nm technology node.

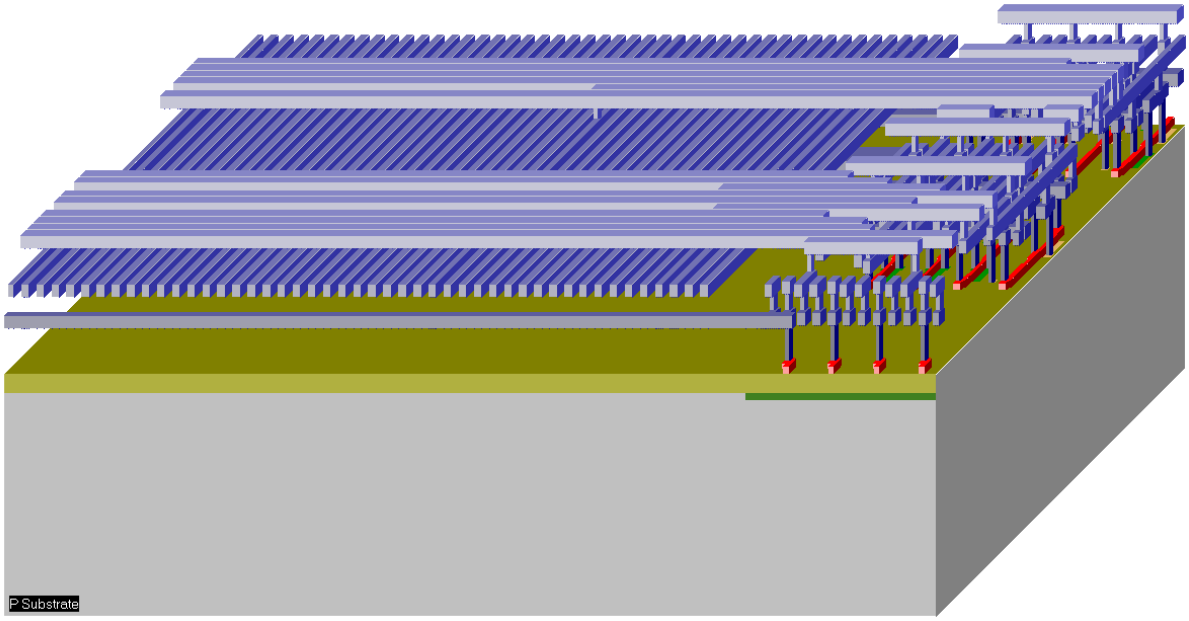

Figure 10. 3-D CMOS-based layout of a 4-bit carry look ahead full adder

V. Conclusion

In this paper, we designed a 4-bit CMOS transistor level carry look ahead full adder circuit in the Proetus environment and then simulated it at various CMOS technology nodes to test its performance. After that, we converted the schematic transistor-level circuit to the layout level in the Microwind environment. Then again simulated it to test the performance and computed various operational parameters, such as the propagation delay, gate and drain capacitance values, power consumption, maximum, and average current drawn by the circuit. In the future, further analysis may be performed for the other digital circuits. Such types of design works and comparative study can be applied in the elementary understanding of the VLSI Circuit Design theory course and simulation-based laboratory works.

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