IOSR Journal of VLSI and Signal Processing (IOSR-JVSP)
Volume 12, Issue 1 (Jan. - Feb. 2022), pp.01-06
e-ISSN: 2319-4200, p-ISSN: 2319-4197
www.iosrjournals.org

Digital to Analog Converter: A Survey

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Abstract— *For decades, there have been many developments found in the field of design techniques or strategies of digital to analog converter (DAC) to meet desired performance requirements of their endless applications among them few are wireless sensor networks (WSNs), radio communication , IoT applications and so on. Based on the literature review this paper exploits a brief summary of different DAC architecture, design strategies and techniques, and DAC modelling considering low power consumption, high performance and optimum area. These design methodology can be categorized into different classifications depending on optimum architecture and performance.*

Keywords— *DAC, Architecture, techniques, high performance , low power , area optimization.*

Date of Submission: 02-01-2022 Date of Acceptance: 13-01-2022

I. INTRODUCTION

In electronics, a DAC is a block that translates signals of digital form into an analog and are found everywhere feature of modern electronics. These DACs are important in those applications which takes the digital input and changes it into the analog form so as to interact with analog circuits. DACs are widely used in countless applications at present. Basic digital to analog converter block diagram is shown in figure 1.

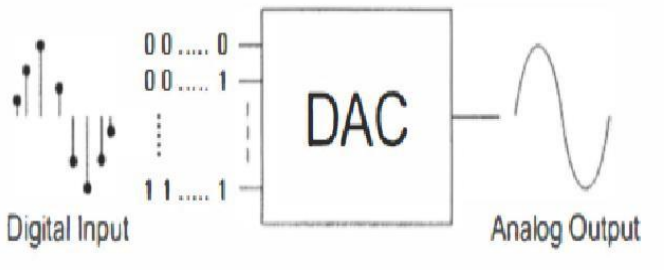

Figure 1. Basic block of a digital to analog converter

DAC's role is very important in converting 1s and 0s in the computer into audio, video, and other data information as per our convenient. Also, it translates instructions that are in digital form to physical information which enables the user to digitally control mechanical devices. Almost all electronic devices are equipped with DACs. Due to its widespread use in almost all applications, there have been many researches to optimize the architecture of DAC for different applications. DACs are widely used in applications such as in the computer's data processing done with the help of modem into audio frequency tones. Digital to analog converter is commonly found in audio players, that is digital data is converted into suitable audio form. Similarly for televisions and cellular phones, the video signals which are in the form of digital are converted into the analog form so as to display in colours. When it comes to its architecture DAC implementations are done with three different ways: resistor ladder, current-steering, and switched capacitor. Even though resistor and capacitor DACs are easy to implement and has good matching they are not suitable for applications that require high resolution and high frequency.

Instead, current-steering DAC is used because of it's high accuracy and speed. These current steering digital to analog converters are of three types they are binary-weighted, segmented and unitary. For optimum performance, discrete DACs are used that would be extremely high-speed, low- resolution and especially found in application such as military radar systems and sampling oscilloscopes.

II. ARCHITECTURE AND DAC TYPES

A. *Current steering*

Current steering are integrated DAC compared to resistor DACs. This DAC replaces the resistor element in the resistor architecture with a MOSFET current element. In this work, 130nm technology with current steering architecture is used. ^RMSB/RMSB <= (100%)/ 2~ resistors are correlated to the size of unit current source. Here DAC is integrated with class AB amplifier and a folded cascade amplifier configuration which is used to generate each operational trans conductance amplifier (OTA). NMOS is operated in input differential pair and hence compared to other methods the area required is more[1]. This work exploits 13bit 2.4GHz 180nm technology high-speed phase calibration current-steering DAC with quad – switch architecture. An interface is possible between analog and digital domain by adding a toggle bit so as to maintain frequency and PVT (pressure, voltage, temperature) variations. Current-Steering method is used as it the recent device for present day high speed DACs in the processes of CMOS[3]. It is known that this type of DACs are suitable for mentioned applications like high speed hence, in this research 1.2GHz 10bit DAC is suggested. The combination of resistor ladder with unit current sources and binary weighted architectures are suggested as it drops the number of current sources and power dissipation. The static and dynamic characteristics are improved by matching accordingly with proper resistors and equal number of current sources[4]. And when it comes to other evolving transistor technology this work suggests 14nm 12bit technology in FinFET's which are lightly doped channels. To lessen current source mismatch calibration technique is used and to reduce the impact of systematic mismatches, DEM(dynamic element matching) based on barrel shifter is used. For a safer operation NMOS to PMOS ratio is essential and it's made up of an output switch array, current source array, decoding logic and a bias generator. Result is that the proposed system is utilized with exceptional power competitiveness in multi mode cellular applications and shows fine figure of merits enclosed by frequencies that are utilized for cellular applications [6]. This paper has 40nm 10bit technology and converted MSB's into thermometer codes to control current- steering switches and current sources, CSB's to direct binary method. TIA(trans impedance amplifier) buffer is used in the output to achieve current to voltage conversion and output swing control. To reduce power consumption the smallest transistor which meets noise and mismatch requirements is used. Here the current is determined by random mismatch as well as thermal and flicker noise of the transistor of current source but as compared to calibration method the average area is more[10].

B. *Binary weighted DAC*

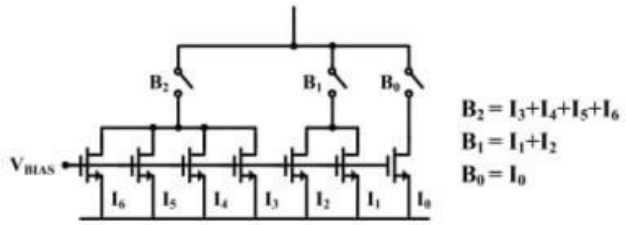

Figure 2. Basic block diagram of B*inary weighted DAC*

Binary weighted DACs are a group of data converters that translates binary number that are in digital form into the suitable analog output signal with respect to the value of digital number. Conventional binary weighted DAC is used for traditional approaches to designing DAC's. Figure 2 shows the basic architecture of binary weighted DAC. Here it focuses mainly on improving spurious free dynamic range(SFDR) which plays major role in enhancing the performance of digital to analog converters and the difference of the amplitudes between maximum and fundamental harmonic Nyquist bandwidth is used for measuring it. As discussed earlier to reduce the effect of mismatches calibration technique is widely used, but when compared DEM technique is finely effective method in overcoming the effect of mismatches hence it is suggested in this paper work. Among DEM techniques, Random Rotation Based binary weighted Selection (RRBS) DEMs are used[5].

C. *Current mirror*

In this paper, 130nm 10bit technology is used. To increase the circuit precision cascaded current mirror is used. By oversizing the transistor sensitivity to transistor mismatch can be reduced. The presented circuit which is in the current form is flexible and effective solution due to the usage of different ranges of branches and to increase the testing abilities they have realized it with high resolution. Compared to all other methods current mirror and ReDAC has very less area consumption

D. *Relaxation DAC*

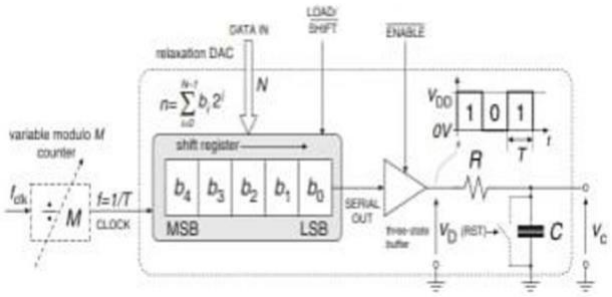

Figure 3. Block diagram of N=5 bit Relaxation digital to analog converter

A 300S/s 10bit technology with bit – stream data conversion technique is suggested in this paper which is suitable to ultralow voltage for IOT applications and it has been implemented on FPGA. To generate binary weighted voltages (BWV), first order low pass Resistor Capacitor network is used as it provides impulse response exponentially. While practically implementing ReDAC(relaxation DAC) in this work, the total energy per conversion is lowered due to lower capacitance[7]. This work is the advanced version of previous work here they have used 10bit 400KS/s technology. It includes three stage digital buffer that drives first order Resistor Capacitor network as shown in figure 3. ReDAC is low cost, energy and area efficient. Compared to BWC(binary weighted capacitor) array ReDAC includes RC network (Metal-oxide metal capacitor is used), digital core and a control unit. This method is best as compared to other methods as it has very low area consumptions[8].

E. *R-2R Ladder*

R-2R kind of DACs require only precision metal film resistors which makes them easier to build accurately. Addition of more section same R-2R values the number of bits can be expanded. With Changing input binary words, the node voltage is constant in inverted R-2R ladder digital to analog converters. Resistors are connected in parallel in BWR(binary weighted resistor) DAC which is used to connect between two voltages and millman's theorem is utilized to analyse their behaviour. In binary weighted resistor DAC the resistance which causes loading effect is varied whenever there is a variation in the binary bit value. Power dissipation and non linearity also varies. But in R-2R type operational amplifier is not considered hence R-2R ladder DAC is superior when compared to BWR DAC [9].

III. DAC STRATEGIES AND TECHNIQUES

A. *Current source*

Combination of resistor ladder with unit current sources and binary weighted architectures are used in this method which reduces the power dissipation and with this technique improvements are found in the dynamic and static characteristics. We expect high impedance at the output of unit cell to obtain the precise static characteristics. Due to this a cascade stage has been used.[4]. To achieve an over-drive voltage of 650mV, minimum current source area is achieved by selecting appropriate width to length ratio (W/L) and also to get low power consumption a super low LSB current of 100nA is addressed. The additional cascaded miller compensation technique used requires a compensation capacitance of nearly two to three times greater than standard miller compensation technique as it provides a betterment in power supply rejection ratio (PSRR). For source and sink operation the current at the output is exceeded to 10 mA and the power consumption found is below 60 μw.[1]

B. *Current mirror*

This work presents a two stage digital to analog converter that works in current mode and it's based upon two multi output current mirrors (CMs), which includes the selected gains of certain branches. The circuit precision is increased by cascading the current mirrors. The specific resultant of two stage branches has a gain that is equal to the gain products of specific current mirrors. [2]

C. *Switch array*

Linearity of the current sources are improved by a new technique called switching. So, when compared with thermometer mode current sources are dropped to half in numbers which results in low area and low power dissipation [4]. Calibration techniques proposed to reduce the current source mismatch suffer from complexity

of design and also area overhead. To overcome this, switch order shuffling is suggested that needs a proper cautious approach in selecting size of a unit transistor and configuration of the current source array.[6]

D. *Calibration*

Clock phase calibration – The combination of clock phase and calibration technique enhances the output performance of DAC as well as improves the maximum frequency of the clock for a given high resolution digital to analog converters, which adds an advantage for high sampling frequency design. To correct the timing violations of setup/hold around the domains of critical analog clock and digital clock and also to maximize the clock frequency, a new calibration strategy for better speed and resolution DAC is suggested here. Without declination of the critical analog clock's phase noise performance, low power designs are realized using this technique.[3]

Digital dichotomic calibration – With high resolution , the time intervals are tuned and controlled finely and by using dichotomic calibration the T value essential to meet the desired condition is achieved in this ReDAC research. Also, can obtain a resolution exceeding 10 bits easily which are finely suited to IoT applications. [7-8]

E. *Bit stream conversion technique*

For IoT applications there is a need of ultra low voltage and tight energy constraints. These can be achieved by the bit stream data conversion technique based on standard cell. In this work, a novel relaxation DAC bit conversion technique is presented as cost effective and insensitive for matching effects which are suitable for ultra low voltage applications. ReDAC proposed here consists of three stage digital buffer that drives first order Resistor Capacitor network with amplitude equals to the VDD supply voltage or 0V reference voltage and a successive N bit rectangular pulses of width T. By using parallel shift register with frequency of the clock equal to f=1/T, the sequence can be generated easily. [7-8]

F. *DEM*

When analogized to all other strategies the dynamic element matching(DEM) technique is best suitable for WSNs, one of the popular strategy used for DACs with high performance, this presents a light weight dynamic element matching(LWDEM) technique aiming lower power consumption and area efficient DAC. Thus, this work precisely concentrates on the RRBS DEM that is Random Rotation Based binary weighted Selection DEM that needs a barrel shifter and PRNG composed randomizer. A mechanism similar to RRBS that is LW-DEM is used which utilizes only a rotor without any additional complex logic to overcome the problem of glitch. When compared to conventional RRBS-DEM DAC, this can save power up to 39% and reduce area up to 52% in the randomizer[5]. As seen earlier in the calibration technique design becomes quite complex and hence occupies larger area and to overcome this switching order shuffling is used. Further more the effect of systematic mismatches is reduced by using DEM technique which has established barrel shifter. Level shifter with low crossing point has make before break process and it is achieved by designing the output switches. Also, to get minimum efficiency in the power of envelope tracking (ET), a full scale current trimming technique is used.[6]

G. *Layout*

The design consideration of architecture and floorplan have been proposed in this research aiming to minimize power consumption without degradation of linearity and spurious free dynamic range (SFDR). An optimized layout reduces parasitic and mismatch effects. Static and dynamic errors including current source matching errors, layout gradient errors, and signal synchronization errors are eliminated by optimization of floorplan and layout. [10]

IV. DAC MODELLING

To achieve voltage of 650mV the width to length(W/L) ratio is selected in such a way that the current sources areas are minimized. Power consumption is examined in the range of 0.45 mW to 0.6 mW (Bdec low to high) which is dependent on the value of input code, the discerned power consumption for 1.9V supply is found to be 10.1 mW. The area of the circuit core occupied is 0.18 mm2. The maximum INL(Integral Non Linearity) is found to be 10.4 LSB and placement, with the gradient profile the maximum INL error was found to be 3.69 LSB. The similarity between the INL characteristic and simulated INL result would not be achieved without the shuffling, that represents maximum INL of 1.86 LSB.[6]

A maximum INL and DNL equals to 2.4 LSB and 3.3 LSB(0.9 LSB rms and 0.62 LSB rms) respectively are presented in this work, a SFDR greater than 51 dB is achieved. Here, DAC operates at a higher clock rate and needs off-chip passive filter.[7].
The two 10 bit ReDACs(Relaxation digital to analog converters) in 40nm CMOS technology, occupies a silicon area of lesser than 1,000µm2 and operates from 600mV power supply. According to the post layout simulations the first ReDAC obtain a maximum INL and DNL equal to 0.33(0.1 LSB rms)

DNL(Differential Non Linearity) is found to be 10.3LSB.[1] and 0.2 LSB(0.01 LSB rms) respectively, where as the second the table 1 (figure. 4) shows the comparison with other DACs ReDAC obtain maximum INL and DNL about 0.72 LSB(0.34 with the present work LSB rms) and 1.27 LSB (0.07 LSB rms) and 9.9/9.4 The 60% of the DAC area within the ADC chip does not go beyond 0.01 mm2[2].

Table 1. COMPARISION WITH OTHER DACs			
Performance	[1]	[1] Reference	Present work
Architecture	Current string	Current string	Current string
Resolution(bit)	10	10	10
Technology	350nm	180nm	130nm
Area(mm^2)	0.55	0.35	0.18
Power dissipation(mw)	7.8	22	0.1

Figure 4. Comparison with other DACs

In 180nm CMOS technology a 13 bit 2.4GHz DAC is implemented with the help of detection and correction circuit. The maximum clock frequency and the period is approximately is 2.4GHz and 417ps respectively. The occupied area of the time to digital converter circuit is found to be 0.032 mm2. . When compared to set-up flash hold time of the re-timing Dflip flop, the minimum quantization range is much less i.e. 417ps/34=12.26ps. The total power consumption of phase calibration circuit is 3.65mW.[3]

The INL of 0.25 LSB and DNLof 0.12 LSB are presented in this work. Except the case of average curve(lesser than 0.01 LSB) all others have INL and DNL lesser than 0.8 LSB and 0.6 LSB respectively. The power dissipation of all digital and analog part of the circuit is found to be 8.4mW and the power supply is 1.2V.[4]. In this paper implementation of a 12 bit DAC in 65nm CMOS is suggested which has the area of 0.065 mm2. The area occupied by the digital circuit is 0.0036mm2 which consist of switch driver arrays, flip-flops and shifter. The power consumption of the shifter is 181.2µW and PRNG(Pseudo Random Number Generator) is 118.8µW.[5] The active area of 0.093mm2 of the DAC that is implemented in a 40nm FinFET CMOS technology is presented in this paper. More than 50% of the INL error was reduced due to the distribution of current error above the input code by switching order shuffling technique. A maximum INL error of 10.78 LSB is achieved whenever inversely mapped to the intrinsic layout ENOB(first/second) respectively. With respect to a FOM(Figure of merit) about 1.1/1.08 fJ/(conversion step) the average energy per conversion for first ReDAC found to be lesser than 1.1pJ and for second ReDAC will be lesser than 0.73pJ, all these are finely suited for applications that comes under internet of things (IoT)[8].

The INL and DNL of the Digital to Analog Converter ranges from 0.9529 and -0.004 to 0.0097 respectively. In R-2R ladder DAC's output with 8 bit resolution DNL has its range from 0.9996 to 0.0951 and INL is 1.6498. Whereas in the 8 bit BWR DAC's output the DNL will range from – 0.0044 to 0.0097 and INL is 0.0142. In the Voltage mode R-2R DAC's output with 8 bit resolution the INL and DNL ranges from 0.3182 and 0.3182 to 0.024 respectively. The comparison between the selected DACs implemented in CMOS technology is shown in the table 2 (figure 5). [9]

TABLE 2. COMPARISON OF SELECTED DACs IMPLEMENTED IN CMOS TECHNOLOGY							
Ref. (Techn.)	Supply [V]	Res. Bits	F_s [MSmpL/s]	P [mW]	A [mm^2]	FOM(power) fJ/conv	FOM(area) [μm^2]/bit
130nm	3.3	ND	6.144	7.26	0.61	ND	ND
180nm	1.8	10	1000	27	0.2	26.37	195.3
40nm	1.1	6	4000	13	0.09	50.78	1406
0.35µm	3.3	12	0.0285	0.00792	0.04	67.84	9.765
65nm	1.2	10	ND	0.00522	0.16	ND	156.25
This work	1.2	10	1	0.009	0.006	9.79(*)/70(**)	5.86

Figure 5. Comparison between DACs implemented in CMOS technology

A 10 bit low power 160-MS/s DAC in 40nm CMOS technology for BWT the SFDR is more than 70dB(67dB) for input signal up to 8.75MHz and power consumption is 0.43mW with a 1.1V power supply. The proposed DAC has been verified on 40nm CMOS and has an active area of 0.36mm2.[10]

V. CONCLUSION

This paper exploits the importance of digital to analog converter and its different types of architecture and design techniques are discussed. Each type of DAC has its own advantages and disadvantages depend on the application we can use any of them. These different techniques and strategies are used as per the condition for the high speed, high resolution, less area, low power dissipation, low voltage etc. Nowadays researchers are coming up with new technology trends like DSP technique, Dichotomic calibration technique and so on as discussed above that could satisfy the design specifications for optimum performance.

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