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Carbon Nanotube FET based high performance NAND Gate using Cascade Voltage Switch Logic

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Abstract : *This paper depicts the design of NAND gate for nanotechnology. The basic elements which are used in the sketch is Carbon Nanotubes instead of the conventional silicon-based units. The special properties of the carbon nanotubes such as high thermal conductivity & electrical conductivity, aspect ratio, very elastic, high flexibility, high tensile strength, low thermal expansion coefficient and highly flexible which means can be bent considerably without damage. In addition to these basic properties, the Carbon nanotubes give a special opportunity of scaling the circuit design to the nano regime. The logic gate which is designed with the help of CNFETs and CVSL proved to be such an achievement that can ahead used to make complex circuits. The circuit proposed of the logic gate in this paper is designed using the 32nanometre Stanford units CNFET technology and is compared with the conventional CMOS based CVSL circuits. The parameters used for the design analysis are the frequency, power consumption, PDP along with the number of transistors used. It was found that the power consumption for both the logic gate is 52.6% less than the conventional CMOS based NAND LOGIC respectively and the delay is 28.2% less. The obtained outcomes depict a great improvement and the work can be taken ahead for high end circuits.*

Keywords- *CNFET, CVSL, NAND Gate*

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I. INTRODUCTION

CNT, Carbon nanotube is basically made up of carbon elements having diameter in nanometers. In the modern world of advanced nanotechnology, the electronic devices are moving fast towards the nanotechnology. Important step to climb this ladder is the acceptance of CNFETs i.e. Carbon nanotube field effect transistors. CNFET is a field-effect transistor that opt a single carbon nanotube or an array of carbon nanotubes as the channel material instead of bulk silicon in the traditional MOSFET structure [1]. Carbon nanotube field effect transistors have been used in almost all sort of electronic devices. The characteristics properties of carbon nanotubes which make them optimum choice for complex and high-level circuits and applications and even it is a convenient option for replacement of CMOS technology. If we use CNFETs in electronic circuits then it results in high performance, high speed, have size in Pico scale and low power consumption. There are some utmost properties of CNFETs are its strength, compactness, tensile strength and inertness [2]. The improvements in CNFETs give a chance to all the technological research to move towards the nanotechnology regime. Another step in this advancement is the adoption of CVSL i.e. Cascade voltage switch logic. The CVSL gives better outcomes as compare to conventional logic circuits and it is used in designing the circuits. The combination of CNFETs and CVSL in designing of the logic gates results as a benchmark because with the help of that we can able to construct any simple and complex circuits easily. In any logic operations like comparators, multiplexers, or the RAMs to ALU, the universal gates are the basic logic gates, which are used in the construction of any logic devices. The universal logic gates are a type of logic gate, which can implement any Boolean function without the need to use any other type of logic gate and these gates basically used in all type of logic circuits irrespective of simple or complex circuits. Therefore, improvement in the basic unit will automatically leads to the improvement in the whole circuit design and will give efficient outcome in the end [3].

II. CARBON NANOTUBES AND ITS BASIC PROPERTIES

The Carbon is basically a chemical element with atomic number 6 and denotes with alphabet C as a symbol. Carbon is having two most important properties; it is non-metallic and it forms tetravalent bonds which means making four electrons available to make covalent bond and Carbon is available in different forms and these different forms are known as allotropes. The most popular allotropes of carbon are diamond, graphite, amorphous carbon and fullerenes [4]. Allotropes available in various dimensional structure likewise 0D, 1D,

2D, 3D. Low dimensional allotropes like 0D, 1D and 2D of Carbon are widely known as Carbon Nanomaterial. The example of 2D allotrope is graphite also known as the Graphene (2D layer of graphite) and 3D allotrope is known as Diamond. Diamond and graphene have the highest thermal conductivities of all known materials under normal conditions. The Carbon atoms presents in hexagonal or honey comb structure in graphite. The Carbon nanotube is formed by rolling up graphene sheets in a form of cylinder. Rolling up a single sheet known as single-walled carbon nanotubes, SWCNTs and rolling up multiple sheets known as multi-walled carbon nanotubes, MWCNTs. The length varies from nanometers scale to centimeters scale and the diameter for carbon nanotubes scale to nanometers range (10^{-9} meters) [5] CNTs depicts in various forms of structures which differentiated on the basis of length, layer count and thickness. As carbon nanotubes depicts in different type of structures, among those semiconductor form of carbon nano tubes is used in the design of Carbon nanotube field effect transistor (CNFET). The basic structure of how graphene sheet looks like is shown below in figure 1. These sheets of graphene consist of a mesh like structure with a combination of carbon atoms. These sheets when rolled up are called as the carbon nanotube.

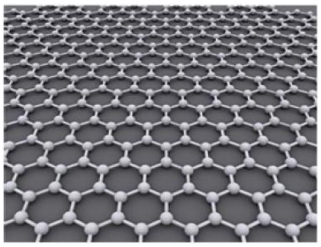

Figure 1: Structure of Graphene

The other basic structure of carbon nanotube is as shown below in figure 2. The type of nanotube depends on the shell count that constitutes the tubular structure [6].

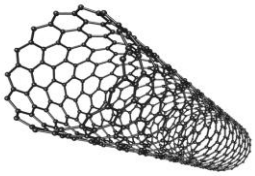

Figure 2: Structure of Carbon Nanotube

As mentioned above depending upon rolling properties, it may have one wall, two walls or multiple walls. The three types of carbon nanotubes are as explained below:

Single-walled Carbon Nanotubes (SWCNTs): This type of carbon nanotube consists of only single layer of graphene cylinder. This single layer can either be of metal or semiconductor.

Double-walled Carbon Nanotubes (DWCNTs): This type of nanotube lies between of the single walled and multi walled. They have dual layers of tubes which rolled up at some specific angles.

Multi walled Carbon Nanotubes (MWCNTs): This type of carbon nanotubes consists of multiple layers which comprises both the metal and semiconductor layers of cylindrical materials [7]. The metallic cylinder negates the properties of semiconductor material. Due to this drawback, MWCNTs is basically not preferred for the industry applications. The structure of all these types of CNTs is shown below in figure3, where (a) represents the Single walled CNTs and (b) represents the double walled CNTs and (c) Multi walled CNTs [8].

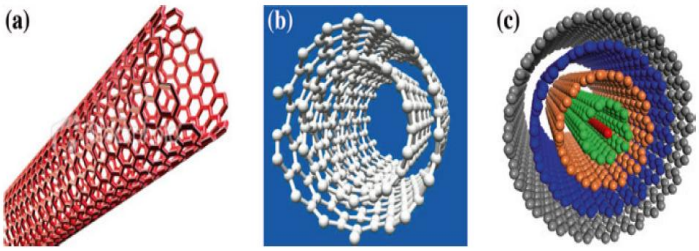

Figure 3: Types of Carbon Nanotubes

III. CARBON NANOTUBE FIELD EFFECT TRANSISTOR (CNFETS)

A Carbon nanotube field-effect transistor (CNFET) is basically a field-effect transistor that usually use of the carbon nanotubes or an array of these tubes instead of the bulk silicon. Advancement in carbon nanotube transistors boosted recently, because of the reason as they potentially be minimizing to such extent as compare to silicon transistors and therefore, they intend to produce stacked layers of circuitry more precisely than as can be done in silicon before [9]. For Channel material, nanotubes are used. CNFETs having similar structures as MOSFETs, as both have 3 terminals, that is source, gate and drain. The structure of CNFET is shown below in figure 4. The current flows from the source terminal to drain terminal, controlled by gate terminal. When the gate terminal is on, the channel present in the FETs, allows the current to flow from source to drain through it. The channel present in MOSFET and CNFET differentiate them from each other [10], as the MOSFETs use heavily doped Silicon material as channel material and the CNFETs use the carbon nanotubes as the channel material which is used for the current to flow in the circuit from source to drain [11].

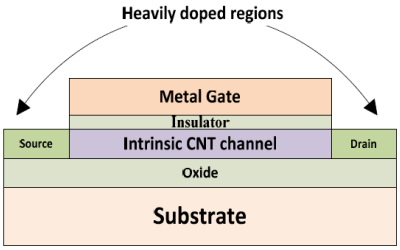

Figure 4: Schematic Diagram of a Carbon Nanotube FET

As seen in the figure 3, the Carbon nanotube field-effect transistor is a four terminal device just like the MOSFETs (conventional silicon based). The conventional techniques for fabricating CNFETs includes pre-patterning parallel strips of metal across silicon dioxide SiO^2 substrate. CNFETs comprises of Carbon nanotube-based channel [12]. The channel is separated from the metallic gate terminal with the help of the insulator sandwiched between the two layers which is one metal strip is the "source" contact while the other is the "drain" contact. Silicon oxide (SiO2) substrate is used as the gate oxide and metal contact can add on the back makes the semiconducting carbon nanotubes gate able. The current flows into the circuit via the source terminal and moves towards the CNT based channel and exit the device from the end terminal which is the drain terminal. The source terminal and drain terminal acts as the interconnection for connecting more devices [8-9]. Despite of similarity in structure between CNFET and MOSFET, but there is a drastically difference in the performance and characteristics. CNFETs replaced MOSFETs because of a number of drawbacks faced by them. Some of the setbacks are as follows like the temperature on threshold voltage is very high which is negligible in case of CNFETs, short channel effects, reliability issues, high leakage currents, threshold voltage decreases drastically, and many others [13]. With the advancement in nanotechnology, the CNFETs replaced the MOSFET devices very easily. On the other hand, CNFETs offers high temperature resistance, device in nanometer regime is to increase threshold voltage at 10nm and beyond the channel length, strong inter bonds that provides strength at such a small size, high electron hole mobility, large transconductance and many more. In inference, Carbon nano tubes based Field-effect transistors have become an ideal device for the transistor material [14].

IV. CASCADE VOLTAGE SWITCH LOGIC

Cascade voltage switch logic (CVSL) is a type of logic which refers to CMOS type logic family which is used to design the digital logic circuits for certain advantages. The main concept used in CVSL is that it requires both the true and complementary form of inputs and it needs mainly N-channel MOSFET transistors to design the logic using true and complementary input signals, and also it requires two p-channel transistors at the top to pull one of inputs high or pull up PMOS devices high. The design of simple CVSL Circuits is as shown below in figure 1.3 [15].

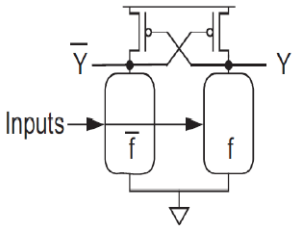

Figure 7: Basic CVSL circuit

As it is understood from the above-mentioned design, it comprises pair of pull-down N trees which are exactly same to one another and same as another pair of pull up p-type devices and among which cross-coupling would be done, whereas 'f' is pull down network and it describes the logic. "f-type" uses inverted inputs that are arranged as in a compliment manner [16]. The working of the circuit defined below: -

1. When input is given to the circuit, one of the pull-down networks is in ON state and other will be in OFF state or vice-versa [16].
2. The pull-down network which is in ON state makes the output le make the output LOW, this LOW output will turn the PMOS transistor to ON state and on the same note it will pull the other output to HIGH state.
3. And when the output of the other network becomes HIGH, as the outcome other PMOS transistor will be turned OFF. Therefore, no power dissipation will occur [17-18].

The CVSL has following advantages that make it a great choice for designing the logic devices.
1. CVSL performance advantage is up to 4X compared to CMOS/NMOS primitive NAND/NOR logic families.
2. The delay time is very less, which increase the speed of the simulation.
3. It improves the on-chip transistor area by reducing the number of transistors required for any circuit design [13].
4. It offers low power dissipation.

V. UNIVERSAL LOGIC GATES – NAND GATE

The logic gates that can be used to construct all logic circuits are termed as Universal Logic Gates. There are two types of universal logic gates termed as NAND and NOR logic gates. If we want to make any complex logic circuit then that can only be possible with the help of these two universal logic gate circuit. Among these two logic gates which is discussed in this research paper is the NAND logic gate. As NAND, its name described it is made up of AND and NOT logic gate connected into series combination to form NAND logic gate circuitry. In simple words the NOT of AND logic gate or the complementary form of AND logic gate is termed as NAND logic gate. Representation of NAND gate is shown below in figure 4. The symbolic representation for the NAND gate is as shown in figure 5.

Figure 5: NAND logic gate Symbolic Representation

The equation used for NAND logic gate is shown below in equation 1.

$$Q = \overline{A.B} \tag{1}$$

The truth table for NAND gate is shown below in table 1.

Table 1: Truth table for 2-input NAND Gate

A	B	NAND
0	0	1
0	1	1
1	0	1
1	1	0

As shown in the truth table, output of the NAND logic gate is high if any input to the logic gate is low. The NAND gates are generally known as the building blocks because they are used in the designing of all logic gates. It is the most used logic function. Therefore, they named as "Universal Gate". The NAND gates are available in various IC packages such as 7400 IC series, 74LS00 Quadruple IC and many more [20-21].

VI. CNFET BASED PROPOSED DESIGNS

The design and analysis of the NAND gate is done using CVSL. The carbon nanotube field effect transistors (CNFETs) is used as transistor base. The circuit is designed using the Cadence Virtuoso simulator and the schematic opt for the designing is the 32nm Stanford carbon nanotube FET library for Carbon nanotube field-effect transistors and 90nanometre Stanford standard cell library used for the Silicon based Cascade voltage switch logic circuit design. Proper biasing is done to ensure the circuits fully functional. The circuit designed is the universal NAND logic gate. Initially, the circuit designed is the CMOS based NAND logic gate using the CVSL and then the other circuit designed is the CNFET based NAND logic gate using the CVSL. These circuits are shown below in the figure 8 and 9 respectively.

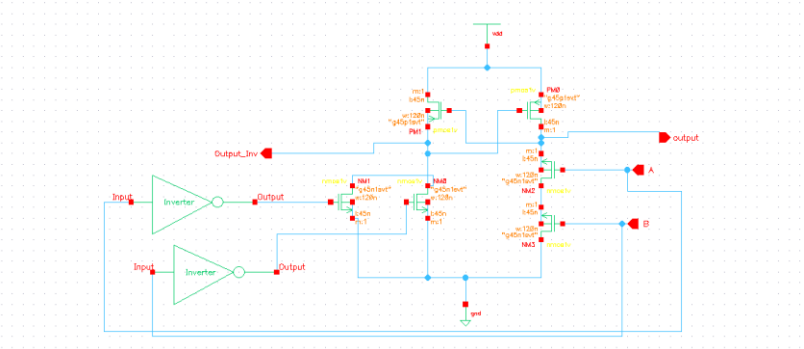

Figure 8: CMOS based NAND gate using CVSL

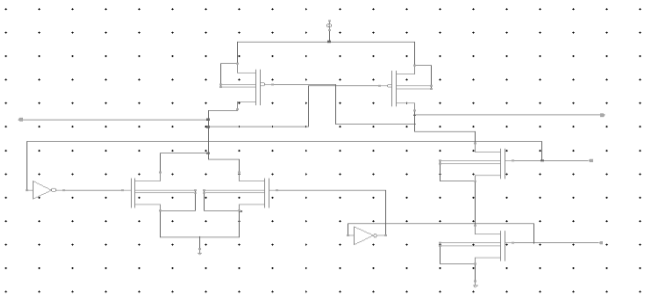

Figure 9: CNFET based NAND gate using CVSL

As shown in above two figures, the circuit designing is exactly similar for both the designs. There is only one difference that is material used in designing process. Both circuits are designed using the CVSL. As per the working of CVSL, at the end of each period, we get two output response. For any set of inputs, we use 0 and 1 as input which means one is true and other is complimentary form in every cycle. Then, at the end of each period we receive true and complemented outputs. For this circuit one is the NAND and the other is the inverted NAND logic output. Which implies at the end of each period, we get the output for NAND as well as AND logic. Therefore, CNFET based circuit is used for making a comparison with CMOS based logic gate circuit. Similarly, to the CMOS based circuit, at the output both the NAND and AND logic are obtained. Both the circuits are compared based on a set of different parameters.

VII. RESULT ANALYSIS

The analysis for the NAND GATE is done using the Cascade voltage switch logic in the Cadence Virtuoso environment. The output is obtained. The schematic designed with the proposed logic is compared with the CMOS technology and the CNFET based circuit. The corresponding schematic design output waveforms are as shown below in figures 12 respectively for the CNFET based NAND logic.

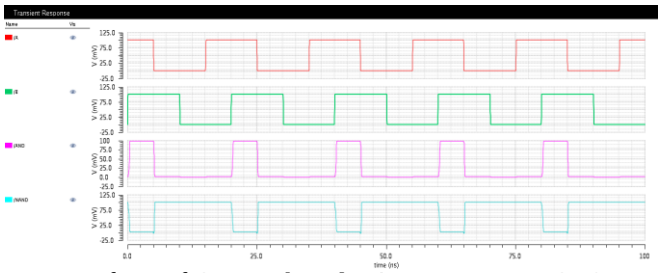

Figure 12: Waveform of CNFET based NAND gate using CVSL waveform

The parametric analysis for NAND logic for both type of circuits i.e. CNFET and CVSL along with the previous work done and observed summed in a tabular form is as shown below in table 2 [9]. All these parameters are observed taking the same frequency.

Table 2: Parameter Analysis for NAND Gate

Parameter	Previous CNFET Work	CNFET based NAND Gate using CVSL	CMOS based NAND Gate using CVSL
Frequency	1.00E+09	1.00E+09	1.00E+09
Power	2.83E-08	6.602E-12	13.942E-12
Delay	7.24E-13	19.43E-12	27.22E-12
PDP	2.05E-20	1.28E-22	3.79E-22
Transistor Count	10	10	10
Number of Cycles	2	1	1

It can be easily observed from the above given table that the delay obtained at the selected edge of the output and input, for CMOS based NAND gate is 27.22ps which is very high as compared to the CNFET based NAND gate which is 19.43ps. Also, power consumed by Carbon nanotube FET based NAND gate is 6.60pW which is low than the CMOS based NAND gate which is 13.94pW.

VIII. CONCLUSION

In this work, universal logic gate, NAND logic is designed, simulated, analyzed and compared with two different technologies. From the observations summed up in the table 2, it is very much apparent that the power consumption in case of the CNFET is almost 50% less than the conventional CMOS based NAND logic. In addition to it, it is observed that in comparison to previously design CNFET based NAND gate, the CVSL based CNFET circuits have shown a benchmark improvement in all the parameters. The time delay in the circuit is also reduced about 40% less than the CMOS based circuit for NAND. Thus, the proposed design of the universal gates gate using CNFET have shown a significant improvement in the design parameters when even the number of transistors used and the logic implemented are the same. Therefore, the CNFETs can be used further in the design of much more complex and larger circuits with parameters having much better performance than the CMOS based circuits.

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