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Design of a Radiation-Hardened SRAM Cell using 16nm Technology Node

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Abstract: *Electronic circuits are exposed to very high energy radiation in the harsh conditions of outer space. This leads to soft errors such as single-event upsets (SEU), double-event upsets (DEU) and single-event transients (SET). The memory circuits are the most susceptible to these soft errors resulting in severe data loss. This paper proposes the design for an SRAM cell that is radiation hardened by design (RHBD). A comparative study of the standard SRAM cell and the RHBD SRAM cell indicates that the proposed design is resilient to SEUs and DEUs. The proposed design is an improvement on the 8T SRAM cell design and includes a 20T triple interlocked cell (TICE) design. The error correction capabilities of both designs are compared by manually injecting bit upsets at crucial nodes in the circuit. It is observed that the TICE design provides a 96.75% and 98.5% improvement over the standard 8T cell for 1-0 and 0-1 bit upsets respectively. The proposed design has been implemented using the 16nm model from the Arizona State University's Predictive Technology Model (ASU-PTM), and the LTSpice software was used to carry out the simulations.*

Tools used: *LTSpice v17 is the tool used to design the schematic circuits and to obtain the simulation results. The library file used to design the schematic is the 16nm technology node from the library of the Arizona State University's Predictive Technology Model (ASU-PTM).*

Methods: *To perform a comparative study of the 8T SRAM and 20T TICE, the schematic circuits were designed using the 16nm technology node in LTSpice. A baseline for the expected voltages of logic 0 and logic 1 is established before injecting errors at the sensitive voltage nodes of the circuit. The next step is to manually inject bit upsets at the crucial nodes of the memory cell to induce either a 0-1 upset or a 1-0 upset. The read/write operation is carried out along with the error injection to compare the error mitigation capacity of the circuits. Finally, the results are tabulated to prove that the 20T TICE is resilient to soft errors arising from exposure to high radiation.*

Results: *During the normal operation of the 8T SRAM cell, the observed output voltage corresponding to logic 0 and logic 1 are 25mV and 780mV respectively. The voltage levels increased to 400mV during a 0-1 upset and dropped to 25mV during a 0-1 bit upset. This indicates that the cell is not reliable. In case of the 20T RHBD cell, the voltage levels for the normal operation were 5mV (logic 0) and 780mV (logic 1). The major improvement is shown in the case where the 20T TICE is injected with bit upsets, since it delivers a voltage of just 6mV during a 0-1 bit upset and maintains a voltage of 770mV during a 1-0 bit upset.*

Conclusion: *The work performs the schematic designs for the comparison of the error mitigation capabilities of a 8T SRAM cell and a 20T TICE which is radiation hardened by design. The study proves that the 20T cell is capable of successfully mitigating both a 1-0 bit upset and a 0-1 bit upset.*

Key Word: *DEU; Radiation Hardening; RHBD; SET; SEU; DEU; SRAM.*

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I. INTRODUCTION

With immense amelioration in nano electronics, technology is headed towards aggressive shrinking of electronic components such as transistors, resistors and capacitors in Integrated Circuits. With the technology headway and the high efficiency and stability of the device, VLSI circuits have constantly delivered high performance and minimum cost [1]. As the scaling down of structure increased expectations include improved speed and density, and reduced power consumption for amalgamating an entire system on a micro sized chip also increased.

SEUs are soft errors where the logic states are changed by high-energy radiation particles [2]. On the other hand, SETs are unwanted transient disturbances which can systems to malfunction, thus leading to SEUs or system deadlock [3]. Due to shrinking feature size of transistors the occurrence of multiple events (multiple upsets) has increased significantly.

It is important to enhance the reliability of memories in satellites as they constantly store crucial intermediate data which are to be processed [4]. Unfortunately, the memories are highly susceptible to soft errors including. To mitigate these soft errors, the design techniques for radiation-hardening is important. The RHBD techniques generally incur overheads and enhance either SEUs or SETs but not both [5].

Due to rapid evolution in technology, the parts of the devices which are most vulnerable to ion hits, namely, the sensitive volumes, become smaller, and the operational voltage of modern devices is reduced [6]. As a result, the critical charge needed for a bit flip in an SRAM device due to an impinging heavy ion becomes smaller. This reduces the charge present at sensitive nodes, thereby decreasing the static noise margin (SNM) [7]. Due to the lower node charge and decreased SNM, the SRAM is extremely susceptible to high energy radiation particles. Technology miniaturization has a negative impact on sensitivity to high radiation environments.

Compared to past technology nodes, the device scaling may cause an increase in SEU sensitivity of the regular (unhardened) six transistor (6T) SRAM cells [8]. Although an SEU is a non-destructive event, the increase of SEU probability may pose a significantly growing problem for the use of larger scale SRAM devices. This is especially true in commercial off-the-shelf products, in space missions and nuclear power reactors which uses high performance digital signal processors. This is an even larger concern due to multiple bit upsets, which may lead to multiple errors in the same word [9].

In the design proposed in this work, the standard SRAM cell is radiation hardened to mitigate SEUs and DEUs. The TICE memory cell can self-correct up to two simultaneous upsets. To further enhance the overall reliability, layout techniques are applied to place the critical nodes in TICE memory cell as far as possible. This reduces the possibility of the critical nodes being hit simultaneously, under the assumption that three simultaneous upsets are rare. When compared to the standard 8T memory cell and DICE memory cell, the memory cell proposed in this work is observed to have a higher radiation tolerance.

II. LITERATURE SURVEY

N. K. Z. Lwin, et al. propose the memory cell that is resilient towards SEU and SETs in [2]. The work includes a tabular comparison of the power consumption, read/write delay and the area consumed by the radiation-hardened memory cell. The cells are designed using the 65nm technology and include the design of a redundancy voter to read the accurate value for the SRAM cells. A dual interlocked cell is proposed to mitigate the soft errors and includes the layout of the said design.

Yuanyuan Han, et al. address the issue of radiation hardening by proposing the design of a 12T dual access SRAM cell using the 28nm CMOS technology [3]. The design is observed to have an area penalty of 209% and also includes the crossbar based peripheral circuit to deal with read failures at the architecture level. Further, this work suggests that the RHBD cell is resilient to only the SEU. This leads to a comparison of the various available SRAM cell configurations such as 12T-DA, standard 6T and standard 8T cells to observe the areas consumed by these cells when formed into a 2x2 memory array. This proved that the standard 8T cell consumed the least area, hence it is the initial cell considered in this paper's proposed design.

C. Naga Raghuram, et al.include the design for an RHBD 15T cell that is resilient to double node upsets arising from an SEU in [4]. It is illustrated that this design is nearly 3 times more robust than the corresponding 14T SRAM cell. The read and write delays are shown to reduce by a percentage of 42.3 and 5.02 respectively. A comparative study of RHBD 13T, Quattro 10T and RHBD 15T cells shows that the single event double upset (SEDU) sensitivity is the highest in the design proposed in this paper. The cells are designed using the 65nm technology and the work also includes the Monte Carlo simulation of 5000 charge-pair samples to illustrate that the design has a 0% failure probability for the given charge distribution.

A. Haran, et al. propose a design that provides the low power consumption in a radiation-hardened 13T cell used in space applications [6]. The design uses the 180nm CMOS technology. The proposed cell is tolerant towards single event upsets and the work also includes Monte Carlo simulations to illustrate the upset mechanism. It also includes a comparison of various SRAM cells like 6T, 12T DICE and the 10T Quattro cells and demonstrates that the radiation-hardened 13T cell is the better choice for error mitigation.

Ze-Xin Su, et al. present the cell design for a radiation-hardened 14T cell that uses the 28nm CMOS technology in [7]. This paper also compares the performance of a standard 6T cell, standard 8T cell and the RHBD 14T cell. The simulation results verify that the 14T SRAM cell is immune to single-point upsets and improves tolerance towards double-point upsets. The topology of the 8T cell excludes decoupled sections for read and write operations and is observed to be even more susceptible to soft errors in space environments. The

optimized 14T cell design retains the performance of the read-write separation SRAM cell for low power consumption and achieves high tolerance against SEU.

III. PROPOSED METHODOLOGY

A. Working of standard 8T SRAM cell

Fig. 1 illustrates the schematic circuit for a standard 8T SRAM cell. To understand the cause of the soft errors, it is important to understand the working of the circuit. Note that the read and write sections are decoupled in this design.

Write operation:

The write word line (WWL) is high and the read word line (RWL) is low. The input bit is provided using the write bit line (WBL) and its complement (WBLBar). Suppose WBL is high, this implies that WBLBar is low. Since WWL is high, the access transistors M5 and M6 are ON. The value of WBL is stored at node Q and the complement is stored at node QBar. Due to the interlocked nature of the SRAM cell, these values persist as long as the power supply Vdd and Ground are provided. During this process, the SRAM cell is effectively programmed to store the value of 1, since the value of node Q will be the readout. To write a value of 0, the bit lines WBL and WBLBar are set to low and high respectively.

Read operation:

The readout value is obtained using the Read bit line (RBL). The RWL is high and WWL is low. This implies that the read transistor is ON. Since the sense amplifier is connected to node Q bar, its state depends on the value stored at the crucial node QBar. Suppose the QBar value is 0, then the sense amplifier is OFF, and a high value through the M7 transistor is read. In case the QBar value is 1, then the sense amplifier is ON and the value at RBL is low.

Hold operation:

During hold operation the word line is low, hence the access transistors are open. The values inside the cross-coupled inverters have no path to charge or discharge hence the values are maintained

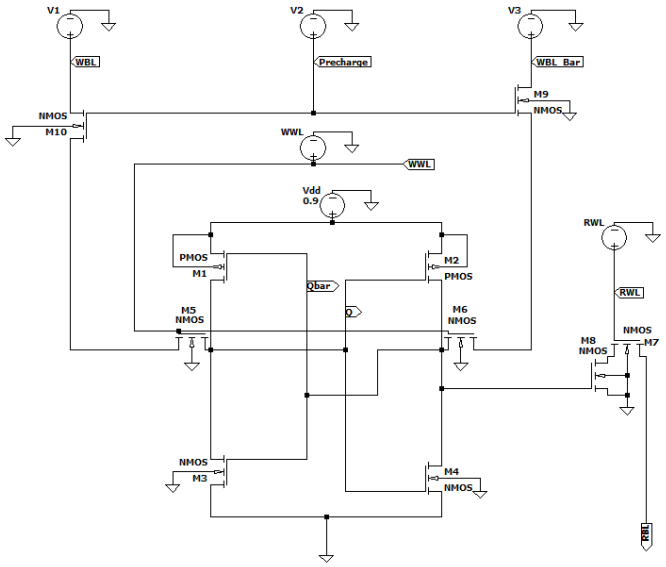

Fig. 1. Schematic design for standard 8T SRAM cell

B. Error injection at crucial nodes of 8T SRAM cell

To compare the error mitigation capability of the standard SRAM cell, an error injection circuit is introduced at the crucial node QBar. The bit upset is induced at this node because the sense amplifier is connected to it. Fig. 2 and Fig.3 show the error injection circuits used to simulate bit upsets of 0-1 and 1-0 respectively. A 1-0 bit upset is a kind of soft error in which the expected RBL value is 1, but the observed value is 0. Similarly, a 0-1 bit upset is the kind of soft error in which the expected readout is 0, but the readout value of 1 is observed.

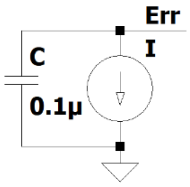

Fig. 2. Error injection circuit for 1-0 bit upset

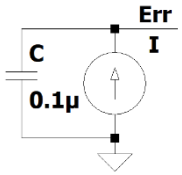

Fig. 3. Error injection circuit for 0-1 bit upset

C. ***RHBD SRAM cell design***

To mitigate the soft errors caused in the previous design, it is important to ensure that the value stored at the crucial nodes of Q and QBar is not affected even after collision with a high energy radiation particle. Fig. 4 illustrates the proposed RHBD SRAM cell design. It is a 20T cell with the input lines WWL, RWL, WBL and WBLBar and output line RBL. Notice that there are separate sections for the read and write operations in this design as well.

Write operation:

The prerequisites for the write operation remain the same, but the major difference is in the manner in which these values are stored. TICE provides a triple interlocked cell structure wherein the nodes 1, 3 and 5 represent the value of node Q and the nodes numbered 2, 4 and 6 represent the value of node QBar. This provides a mechanism to store redundant data within a single cell. The advantage of such a design is resiliency towards soft errors like SEU and DEU.

Read operation:

The mechanism to read the value stored in the cell remains the same, with the added capability to use a triple modular redundancy (TMR) voter to obtain the majority value as the RBL readout.

Hold operation:

As long as WWL remains low, this cell is capable of holding the stored value even when the error injection circuit is introduced at the crucial nodes. The bit upsets of 0-1 and 1-0 are both successfully mitigated using this 20T cell and the reliability of the memory circuit is vastly improved.

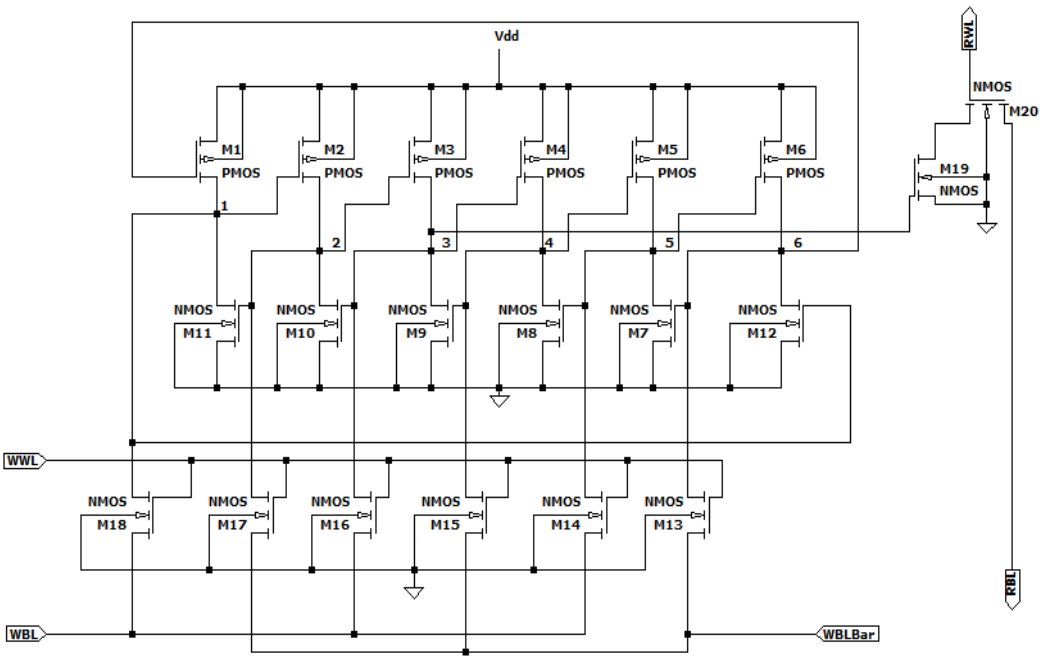

Fig. 4. Schematic circuit for 20T RHBD SRAM Cell

D. ***Error injection in the RHBD 20T SRAM design***

Fig. 5 and Fig. 6 represent the schematic circuit wherein there is a deliberate error injection done at 2 out of 3 sensitive nodes. Fig.5 represents an error injection to simulate 1-0 bit upset. Fig. 6 represents an error injection to simulate a 0-1 bit upset. It is observed that the RBL value accurately matches the value written into the cell via the WBL and WBL Bar in both cases. Hence, this design is resilient to SEU and DEU.

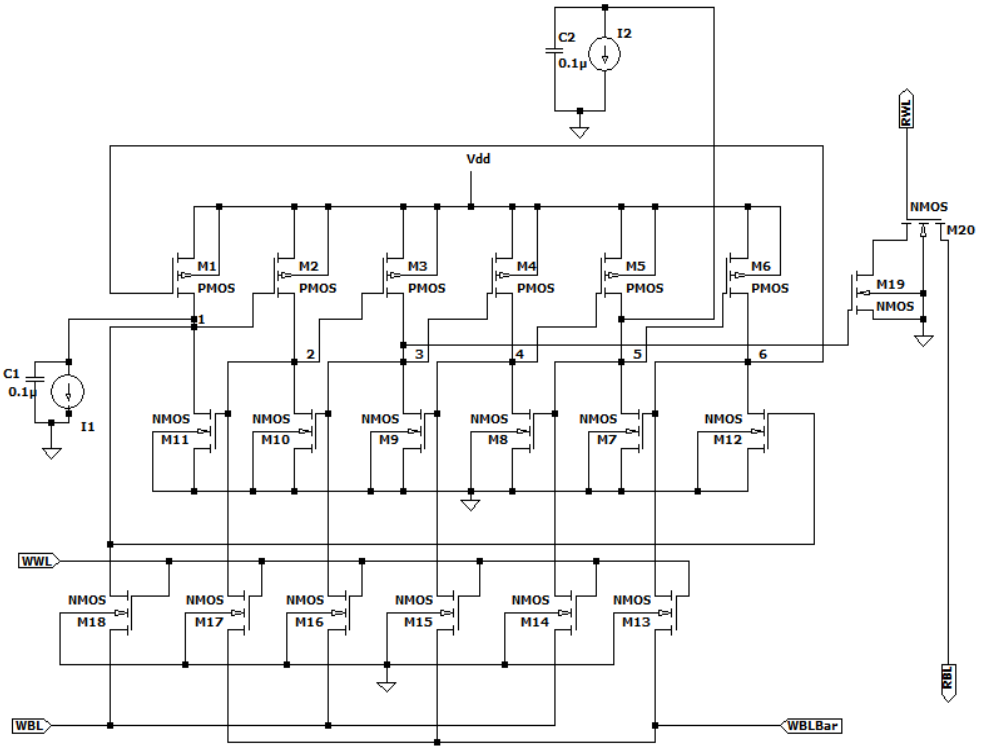

Fig. 5. Schematic circuit for 20T TICE with 1-0 bit upset

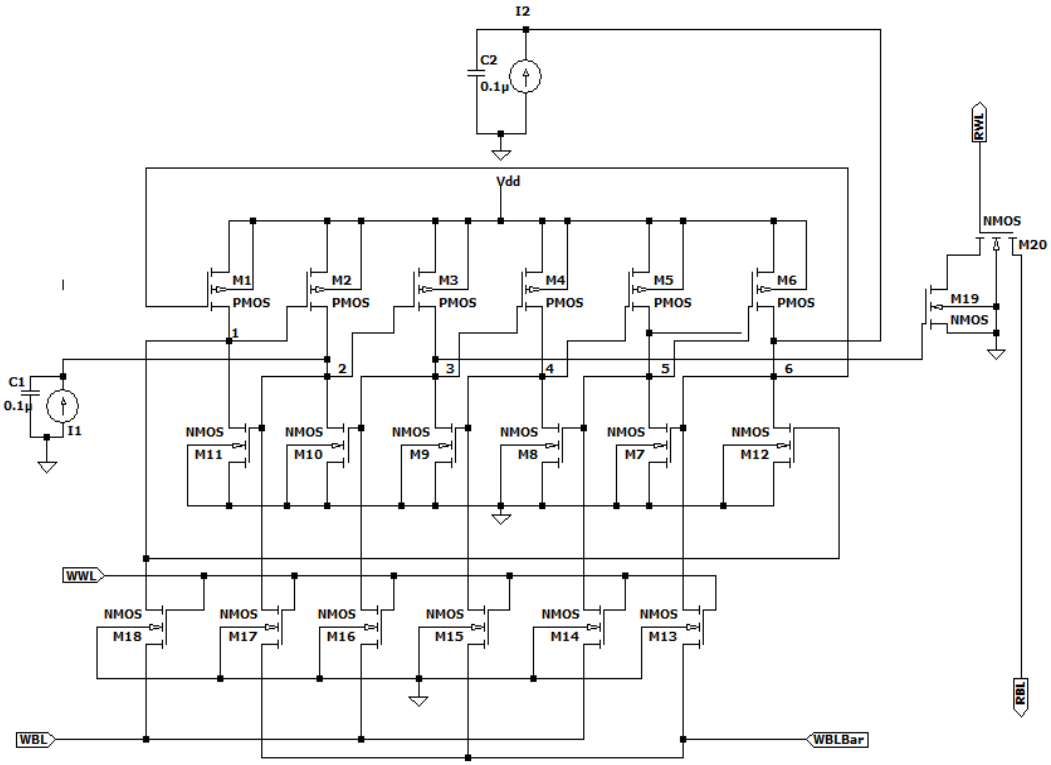

Fig. 6. Schematic circuit for 20T TICE with 0-1 bit upset

IV. RESULTS & DISCUSSION

Fig. 7 illustrates the simulation result for the voltage read at RBL of the standard 8T SRAM cell while reading a value of "1". The upper plot is the case in which there is no error injected at the sensitive nodes. It is observed that the voltage remains constant at 780mV. In the lower plot, it is observed that the RBL voltage drops to 25mV when the error injection circuit is introduced. This represents the 1-0 bit upset.

Fig. 8 illustrates the simulation result for the voltage read at RBL of the standard 8T SRAM cell while reading a value of "0". The upper plot is the case in which there is no error injected at the sensitive nodes. It is observed that the voltage remains constant at 25µV. In the lower plot, it is observed that the RBL voltage rises to 400mV when the error injection circuit is introduced. This represents the 0-1 bit upset.

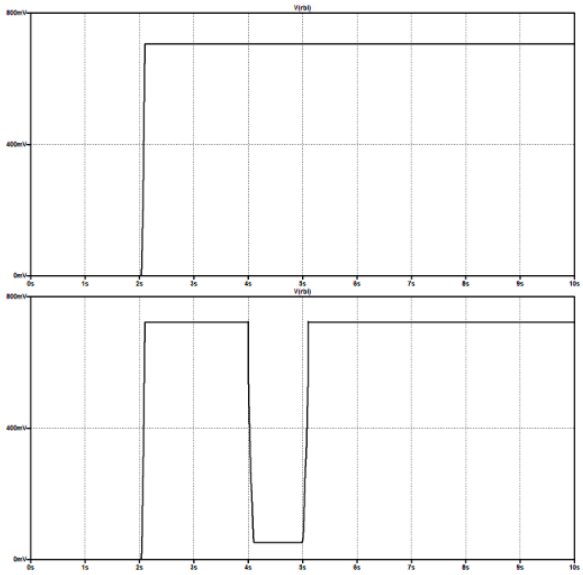

Fig. 7. 8T SRAM's RBL value without any error and with a 1-0 bit error while reading a stored value of 1

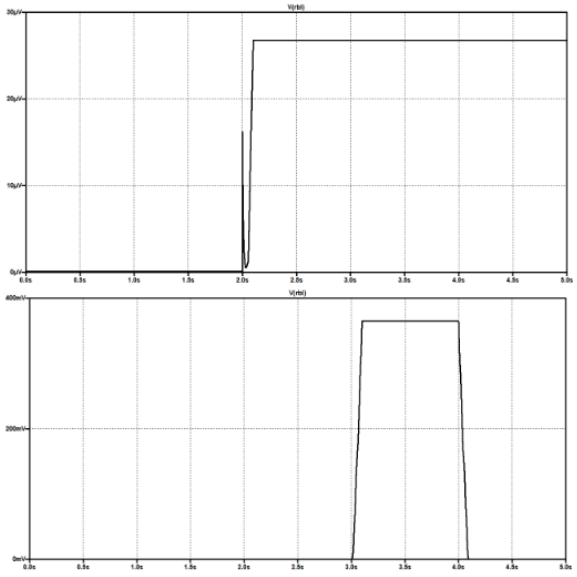

Fig. 8. 8T SRAM's RBL value without any error and with a 0-1 bit error while reading a stored value of 0

Fig. 9 illustrates the simulation result for the voltage read at RBL of the RHBD 20T TICE while reading a value of "1". The upper plot is the case in which there are no errors injected at the sensitive nodes. It is observed that the voltage remains constant at 780mV. In the lower plot, it is observed that the RBL voltage reaches a minimum of 770mV even after a DEU has been simulated. This voltage is too high to be read as a bit value of 0, hence the 1-0 bit upset has been mitigated.

Fig. 10 illustrates the simulation result for the voltage read at RBL of the RHBD 20T TICE while reading a value of "0". The upper plot is the case in which there are no errors injected at the sensitive nodes. It is

observed that the voltage remains constant at 50µV. In the lower plot, it is observed that the RBL voltage reaches a maximum of just 6mV even after a DEU has been simulated. This is insufficient to be read a bit value of 1, hence the 0-1 bit upset has also been mitigated.

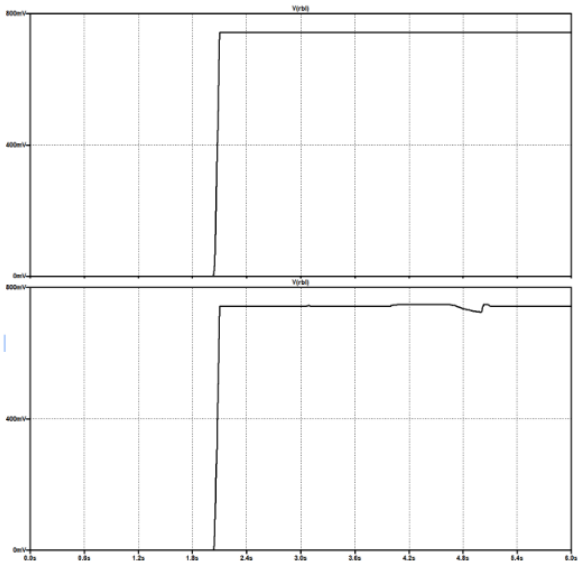

Fig. 9. 20T TICE's RBL value without any error and with a 1-0 bit error while reading a stored value of 1

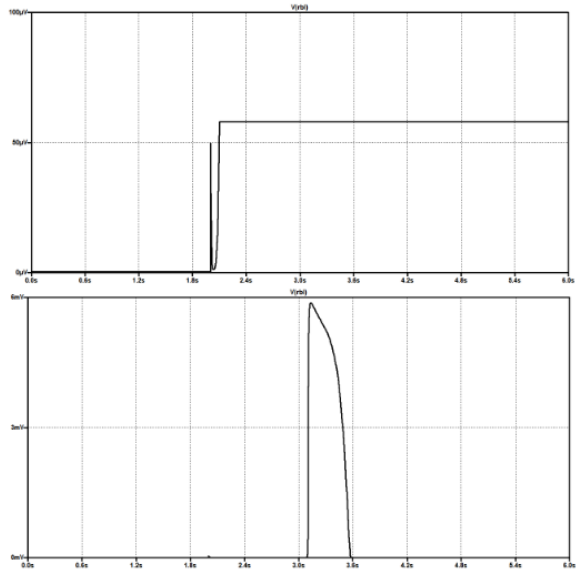

Fig. 10. 20T TICE's RBL value without any error and with a 0-1 bit error while reading a stored value of 0

Table I summarise the performance of both the standard SRAM cell and the RHBD SRAM cell. It is observed that the 20T TICE has outperformed the standard 8T SRAM cell in terms of mitigation of soft errors. The Q value represents the expected bit value to be read. The RBL voltages indicate that TICE is capable of maintaining the expected voltage levels even after error injection. But the 8T SRAM isn't capable of maintaining the required voltages.

TABLE I
COMPARISION OF PERFORMANCES OF 8T SRAM AND 20T TICE

Q Value	**RBL Voltage (mV)**			
	8T SRAM		***20T TICE***	
	Without error	***With Error***	***Without error***	***With Error***
0	0.025	400	0.05	6
1	780	25	780	770

V. CONCLUSION

The design of the RHBD SRAM cell proposed in this paper is shown to be more reliable and is capable of successfully mitigating soft errors like SEU and DEU. The 20T TICE cell is resilient to both a 1-0 bit upset and a 0-1 bit upset. The overall improvement in the voltage measured at the RBL output is 96.75% and 98.5% for the 1-0 and 0-1 errors respectively. Hence, the 20T TICE provides a robust alternative to the standard 8T SRAM cell. The simulation results provide a graphical representation of the error correction capabilities of the proposed RHBD cell. Although the design comes at the cost of area on chip, the reliability issues that are solved by this design is a decent trade-off in crucial applications like space missions.

The cell design proposed in this work can be used to implement a robust memory array for any space application. To further improve the reliability of the memory architecture, a crossbar based peripheral circuit (CBPC) can be included. This will lead to a significant improvement in the mitigation of read/write failures owing to radiation exposure.

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