Performance Analysis of CMOS and FinFET Logic

R.Rajprabu,V. Arun Raj, R. Rajnarayanan, S. Sadaiyandi, V. Sivakumar

Assisstant Professor(ECE),Final Year B.E (ECE) Kalasalingam Institute of Technology Krishnankoil

Abstract: *MOS is an old transistor technology that provides low power consumption, but has a shorter channel for the flow of current and thereby has some drawbacks like excessive current usage and larger size. The FinFET (Fin Field Effective Transistor) is an upcoming technology has a longer channel gate. The size ranges from 32nm, 22nm by Intel and finally it has been shrunk to 14nm by Samsung. This project is a study of these two technologies and we are able to distinguish the techniques and make CMOS as worth as FinFET.*

Keywords *:CMOS,FinFET,Samsung,Fin*

I.   Introduction

Very Large Scale Integration is a process that means to create integrated circuits by combining thousands of transistor-based circuits into a single chip. The microprocessor is a VLSI device. Each and every chip manufactured today use VLSI architectures. Current technology has leaped from the construction of larger transistors on a chip to a microprocessor with millions of gates and billions of individual transistors of small size. Due to this revolutionized idea it finds scope in the fields of high performance computing and communication systems, neutral networks, wafer-scale integration, microelectronic systems and research and development.

Hence there is a rising demand for these chip driven products in the present and upcoming future. To meet with these demands we must reduce the size, power, and efficiency. Out of which power dissipation has become an important objective in the design of both analog and digital circuits. It is demonstrated that because of neglecting short-circuit current, previous techniques proposed to optimize the area of a fan-out tree may result in excessive power consumption. The total active mode power consumption, the clock power, and the average leakage power of the combinational circuits are reduced by up to 55% , 29%, and 53%, respectively, while maintaining similar speed and data stability as compared to the circuits implemented in CMOS and FinFET technology.

II.   Era Of Cmos And Finfet

2.1 CMOS

The term 'Complementary Metal-Oxide-Semiconductor', or simply 'CMOS', refers to the device technology for designing and fabricating integrated circuits that employ logic using both n- and p-channel MOSFET's. CMOS is the other major technology utilized in manufacturing digital IC's aside from TTL, and is now widely used in microprocessors, memories, and digital ASIC's. The low input currents required by a CMOS circuit results in lower power consumption, which is the major advantage of CMOS over TTL. In fact, power consumption in a CMOS circuit occurs only when it is switching between logic levels. This power dissipation during a switching action is known as 'dynamic power'. Aside from low power consumption, CMOS circuits are also easy and cheap to fabricate, allowing denser circuit integration than their bipolar counterparts. In the 70's and 80's, CMOS IC's are run using digital voltages that are compatible with TTL so both can be inter-operated with each other. By the 1990's, however, the need for much lower power consumption for mobile devices has resulted in the deployment of more and more CMOS devices that run on much lower power supply voltages. The lower operating voltages also allowed the use of thinner, higher-performance gate dielectrics in CMOS IC's. The best example of a CMOS design is a Inverter circuit.
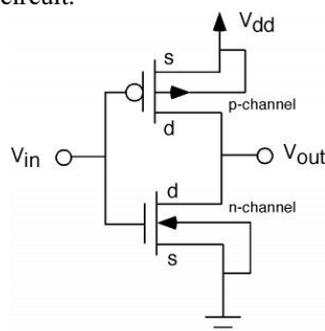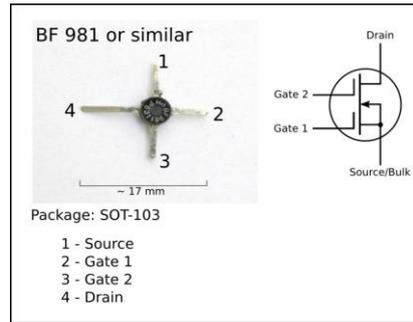

Figure   1: CMOS Inverter

Figure 2: FinFET

2.2 FinFET

Double-gate transistor built on an SOI substrate, based on the earlier DELTA (single-gate) transistor design. The distinguishing characteristic of the FinFET is that the conducting channel is wrapped by a thin silicon "fin", which forms the body of the device. The thickness of the fin (measured in the direction from source to drain) determines the effective channel length of the device. The "Omega FinFET" design is named after the similarity between the Greek letter omega (Ω) and the shape in which the gate wraps around the source/drain structure. FinFET can also have two electrically independent gates, which gives circuit designers more flexibility to design with efficient, low-power gates.

With these technologies in hand VLSI has taken a huge improvement in the field of production and distribution.

III. Small Transistors

Small transistors started to emerge only after the production of CMOS of size 10 μm. The reason behind smaller transistors is the use of gate material. In early CMOS, Aluminum was used as the gate material. The metal disappeared for awhile and we had poly-silicon gate materials. Along the way Copper integration was achieved to help improve conductivity over Aluminum metal layers (integrating Copper into CMOS was non-trivial). This carried forward up to around 65 nm. At 45 nm when we returned to Metal gates with high-k gate stacks. Though there were other processing changes that were used along the way these are the biggest ones, and it is notable that there were not many larger changes made for 40 years. But due to certain disadvantages and some minor drawbacks is overcome by Intel's fully depleted 22 nm FIN-FETs ie non planar transistors. Thus the current transistor size in production is 22nm FinFET.

IV. Parameters For Analysis

The main scope of our project is to bring in lots of parameters for analysis of these two technologies and when considered these parameters i.e. Gate Area, gate capacitance, channel length, delay, sub threshold leakage current, power dissipation play a major role.

4.1 In case of CMOS
4.1.1 Power Dissipation in a CMOS Inverter
For complementary CMOS circuits where no dc current flows, average dynamic power is given by

$$P_{ave} = C_L V_{DD}^2 f \tag{1}$$

where C_L represents the total load capacitance, V_{DD} is the power supply, and f is the frequency of the signal transition. Above formula applies to a simple CMOS inverter or to complex, combination CMOS logic. Applies only to dynamic (capacitive) power, dc power and/or short-circuit power must be computed separately.

4.1.2 Delay Dependence on Input Rise/Fall Time
For non-abrupt input signals, circuit delays show some dependency upon the input rise/fall time. Empirical relationship to include input rise/fall time on output fall/rise delay are given:

$$t_{df} = [t_{df}^2 (stepinput) + (t_r/2)^2]^{0.5} \tag{2}$$

$$t_{dr} = [t_{dr}^2 (stepinput) + (t_f/2)^2]^{0.5} \tag{3}$$

For CMOS the affect of input rise(fall) time on the output fall(rise) time will be less severe than the impact on the

falling(rising) delay.

4.1.3 Loading Capacitance on Gate Delay

Delay equations are often written to factor the impact of the fan-out and load capacitance to the circuit delay,

$$t_d = t_{dintrinsic} + (k_1 * C_L) + (k_2 * FO) \tag{4}$$

where CL is the load capacitance, FO is the fan-out, and tdintrinsic is the unloaded delay of the circuit.[1]

4.1.4 Gate Area

This parameter is also a cause for power efficiency. Thus the various CMOS gate area are considered and plotted with respect to threshold voltage. The gate area of different CMOS is given by the below table

Gate Area	μm^2
DPLCMOS	714.6
invbCMOS	816.92
BSBiCMOS	1277.9
MFSBiCMOS	1291.55
SRBBiCMOS	1568.93
DynBiCMOS	1587.14
BBCMOS	1955.09
BFBiCMOS	2140.07

Table 1: different gate areas

4.1.5 Sub-threshold leakage current

Every transistor has some specified threshold voltage for their ON condition.i.e, the voltage which is needed to make the transistor ON. But due to the movement of minority carriers in the sub threshold region there is some current flow leads to leakage current.

$$I_{ds} = I_{dso} e^{(V_{gs} - V_t)/nV_T} (1 - e^{-V_{ds}/VT}) \tag{5}$$

This leakage current plays a major role in power dissipation and other power related factors.[3]

4.1.6 Threshold voltage

The body effect describes the changes in the threshold voltage by the change in VSB, the source-bulk voltage. Since the body influences the threshold voltage (when it is not tied to the source), it can be thought of as a second gate, and is sometimes referred to as the "back gate"; the body effect is sometimes called the "back-gate effect".

$$V_{TN} = V_{TO} + \gamma(\sqrt{(|V_{SB} + 2\phi_F|)} - \sqrt{(|2\phi_F|)}) \tag{6}$$

where V_{TN} is the threshold voltage when substrate bias is present, V_{SB} is the source-to-body substrate bias, Φ_F is the surface potential, and V_{TO} is threshold voltage for zero substrate bias, is the body effect parameter

4.2 In case of FinFET
4.2.1 Sub threshold Leakage Current

When the transistor is turned on (Vgs $\succ$ Vth) a channel is created which allows a relatively high current to ow between the drain and source. The current from drain to source is modeled as in the below equation

$$I_{ds} = (\mu_n CoxWeff)/Leff ((V_{gs} - V_{th})V_{ds} - V_{ds}^2/2 \tag{7}$$

with μ_n the charge-carrier effective mobility, W_{eff} the effective channel width and L_{eff} the effective channel length. In First order approximation the effective channel width W_{eff} equals the channel width.[4]

4.2.2 Power dissipation

Power dissipation is a combination of static and dynamic power.But in maximum cases it relies on dynamic power.Hence it is given by,

$$P_{total} = \alpha_{ni} I_{sc} V_{DD} f.t_{sc} + \alpha V_{DD}^2 f C_{out} \tag{8}$$

Even though it depends on dynamic power, if static power is reduced then there is low power dissipation.[5]

4.2.3 Gate capacitance

For the gate to change state, the gate capacitance must be charged or discharged. Since the transistor driving the gate has a certain amount of output impedance (resistance), this together with the gate capacitance forms an RC network. The gate capacitance must charge through the driver's output impedance, and this takes time.

$$C_g = C_{ox}WL \qquad (9)$$

So, gate capacitance limits the maximum speed at which the device can be operated. Decrease the capacitance, and you can clock the device faster.

4.2.4 Gate delay

$$T_g = C_g V/I_{on} \qquad (10)$$

Similar to gate capacitance,gate delay is caused when there is some time deviation before of after the change of gate state.

4.2.5 Threshold voltage

Combining the gate work function difference between the gate and the silicon fin, the increase in potential and the increase in band gap results in the following threshold voltage formula

$$V_{th} = V_{FB} + 2\Phi_B + \delta_w + qN_b X_{dep}/C_{ox}(1 - X_h/L) \qquad (11)$$

where, V_{FB} is work function difference , Φ_B is surface potential at threshold voltage δ_w is a fitting parameter introduced to take into account the V_{th} changes.[4][2]

4.2.6 Self heating

Even though FinFET has great advantages it has been affected by self heating which normally measured in terms of rms current value ,

$$I_{rms} = \sqrt{((\int (I(t)^2))/T)} \qquad (12)$$

V.   Simulation Results

The simulated outputs are got from MATLAB with theoretical values of the equations mentioned above. The results obtained are only the first module of our project.The second part of our module is being in progress.
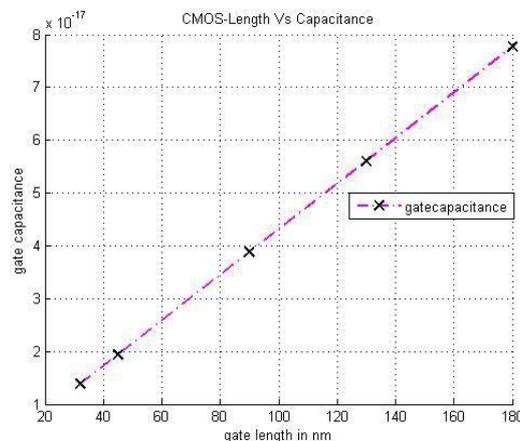

Figure   3: the gate capacitance linearly increases with the gate channel length. So the charging and discharging period for the capacitor formed between the gate and substrate will be increased. This may lead to some sort of delay.
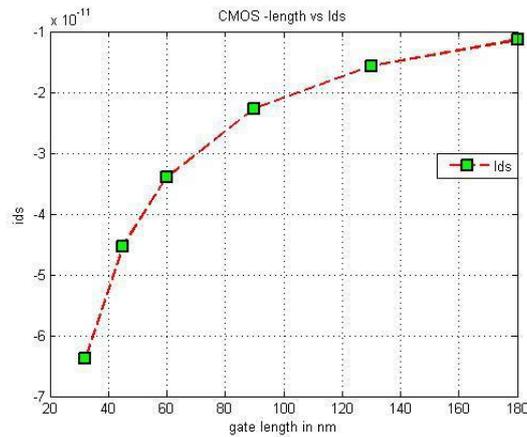
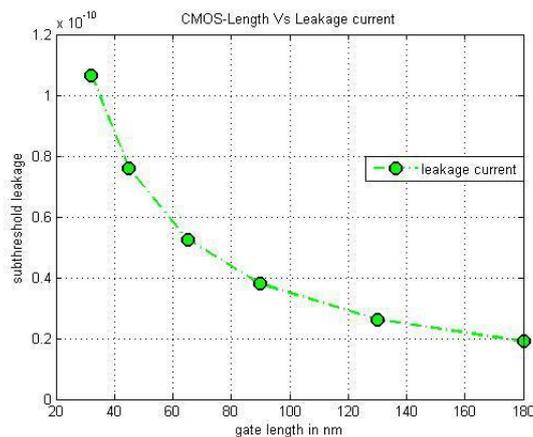Figure 4: In ON condition, Ids gets increased with the increase with channel length.

Figure 5: the leakage current in subthreshold region of transistor gets increased with the channel length decreases. This will lead to some sort of power leakage due to the minority carrier movements in that region.
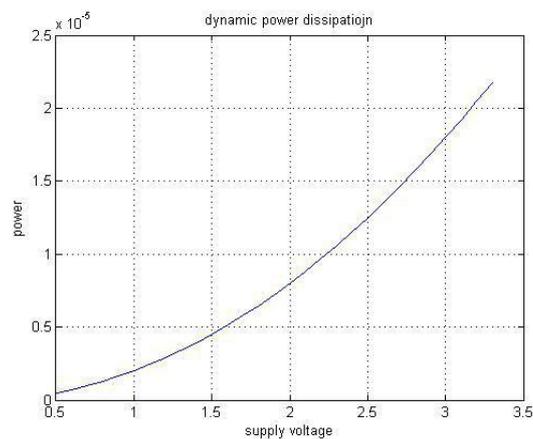

Figure 6: As threshold voltage varies with the gate length the supply voltage also gets varied. From the above results we can infer that the dynamic power dissipation gets increased with the supply voltage increases.

VI. Benefits Of Finfet Than Of Cmos

• Significant reduction in power consumption (50 % over 32nm)

• Faster switching speed

• Effective speed/power trade-off is possible with multi-V_t

• Availability of strain engineering

Eventhough the benefits are great, the only drawback is self heating. And it is said that there are there are two major contenders for the new transistor architecture: finFETs and fully depleted silicon-on-insulator. Both are practical solutions that solve the major short-channel difficulties, both have been proven on real designs, and both are backed by major semiconductor companies. It is not yet clear which technology will predominate or if they will continue to co-exist.

VII. Conclusion

FinFETs a necessary semiconductor evolution step because of bulk CMOS scaling problems beyond 32nm.Use of the FinFET back gate leads to very interesting design opportunities.Rich diversity of design styles, made possible by independent control of FinFET gates, can be used effectively to reduce total active power consumption.Thus the time has arrived to start exploring the architectural trade-offs made possible by switch to FinFETs.

References

[1]   R. Chau, J. Kavalieros, B. Roberds, R. Schenker, D. Lionberger, D. Barlage, B. Doyle, R. Arghavani, A. Murthy, and G. Dewey, "30 nm physical gate length cmos transistors with 1.0 ps n-mos and 1.7 ps p-mos gate delays," in *Electron Devices Meeting, 2000. IEDM'00. Technical Digest. International*. 1em plus 0.5em minus 0.4em IEEE, 2000, pp. 45–48.

[2]   T. Poiroux, M. Vinet, O. Faynot, J. Widiez, J. Lolivier, T. Ernst, B. Previtali, and S. Deleonibus, "Multiple gate devices: advantages and challenges," *Microelectronic Engineering*, vol. 80, pp. 378–385, 2005.

[3]   F. Rossem, "Doping extraction in finfets," 2009.

[4]   F. van Rossem, "Doping extraction in finfets," 2009.

[5]   B. Yu, L. Chang, S. Ahmed, H. Wang, S. Bell, C.-Y. Yang, C. Tabery, C. Ho, Q. Xiang, T.-J. King *et al.*, "Finfet scaling to 10 nm gate length," in *Electron Devices Meeting, 2002. IEDM'02. International*. 1em plus 0.5em minus 0.4em IEEE, 2002, pp. 251–254.