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Improving V_{min} of Sram by Schmitt-Trigger/Read-Write Techniques

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Abstract: *In modern Trends, the demand for memory has been increases tremendously. The reduction in SRAM operating voltage, cell stability and the increase in process variation with process scaling are the main concerns and can be done by Schmitt-Trigger Techniques. Read and write assist techniques are now commonly used to lower the minimum operating voltage (V_{min}) of an SRAM. This paper presents a proposed 7T, 8T SRAM cell based on a various read and write assist technique and reduces the total power consumption and not area overhead of SRAMs while maintaining their performance and compare the output power. Simulation results with 180nm, 120nm CMOS technology.*

Keywords - *Low-Voltage SRAM, Process Tolerance, Schmitt-Trigger (ST), $V_{min.}$*

I. Introduction

In modern integrated chips, RAM cells occupy a major portion .Now-a-days power dissipation in the memory chip require that power consumption during the read and write operation must be low. Technology scaling results in a high density of component but there is a significant increase in leakage current. A minimize size SRAM cell is highly desirable for increasing the memory integration density. As the integration of component increases, leakage power is becoming a prime concern in today's memory chips. Lower voltages and smaller devices cause a significant degradation of data stability in cells.

One possible solution to this problem is to design a more robust bitcell topology capable of larger read and write margins. The downside to this strategy is that adding more transistors to the bitcell increases the total area of the array [9]. The second strategy is to use various assist methods to make the cell easier to read and write. This method also results in a smaller area overhead and may require multiple voltage sources [1]. In this work we will analyze 7T and 8T bitcell topologies and assist methods to determine which is the most effective at reducing SRAM Vmin. In Section II, we will introduce a variety of sub-threshold bitcell topologies and explain the pros and cons of each. In Sections III and IV we will present an overview of read and write assist methods, and explain how each method can be used to improve margins. Section V will present the results from a test chip, and Section VI will conclude.

In order to resolve the conflicting read versus write design requirements in the conventional 6T bitcell, we have to apply Schmitt-Trigger principle for the cross coupled inverter pair[10]. A Schmitt Trigger is used to modulate the switching threshold of an inverter depending on the direction of the input transition. Fig.1. shows the schematic which reveals the Schmitt-Trigger principle. During 0→1 input transition, the feedback transistor (NF) tries to preserve the logic '1' at output (V_{out}) node by raising the source voltage of pull down NMOS (N1). This results in higher switching threshold of the inverter with very sharp transfer characteristics. Since a read failure is initiated by a 0→1 input transition for the inverter storing logic '1', higher switching threshold with sharp transfer characteristics give robust read operation.

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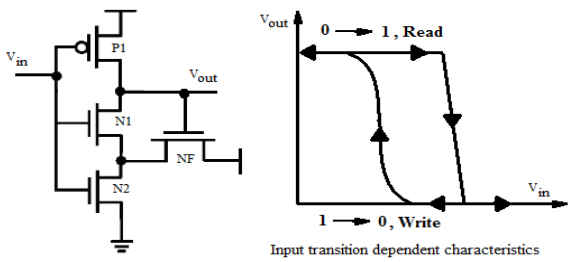

Fig. 1. Schmitt-Trigger Principle

For the 1→0 input transition the feedback mechanism is not present. This results in smooth transfer characteristics essential for easy write operation. This input dependent sharp/smooth transfer characteristics improves both read-stability as well as the write-ability by employing Schmitt-Trigger principle in the SRAM bitcell.

Static random access memory (SRAM) is a critical part of most VLSI system-on-chip (SoC) applications. The SRAM bit cell design has to cope with stringent requirement on the cell area leading to minimum (or close to minimum) sized transistors [10]. Due to this scaling trend, device variations and\ leakages are increasing sharply with each shrinking technology node. Further, the supply voltage is scaled down to reduce dynamic and leakage power consumption. The operation of the SRAM at lower supply voltage becomes even more challenging. The predominant yield loss from increased device variability occurs at minimum operating voltage, a term defined as V_{min}. The failures at V_{min} can be due to write failure, read disturb failure, access failure or retention failure.

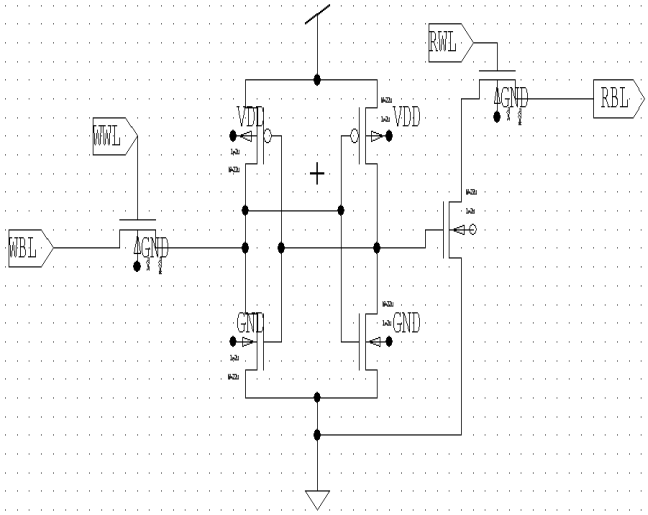

Fig. 2. The schematic of 7T dual-Vt SRAM

Usually the SRAM V_{min} is limited by write failure or read disturb failure. It is, however, difficult to predict a priori as to which of the two failure mode dominates because it is dependent upon many factors including the bit cell architecture, technology node etc. The read disturb problem can be mitigated by adding a dedicated read port where the bit cell nodes are isolated from the bit-lines. These 8T bit cells are larger in area but they eliminate the read disturb issue. Solving the issue of write failure, however, is more challenging. Write failure is defined as the failure to intentionally flip the value of the bit cell during the write operation.

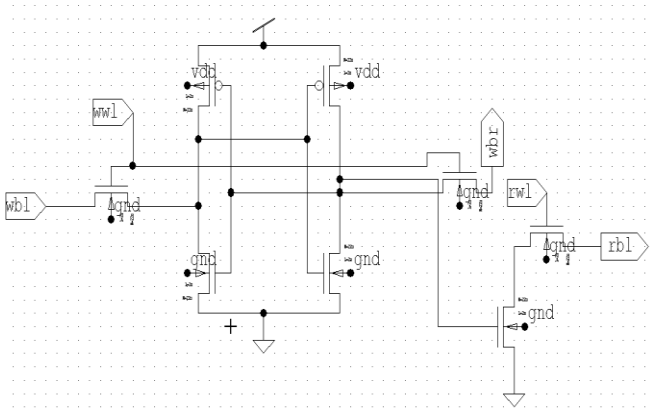

Fig.3. Single Ended 8T bitcell

Various write-assist (WA) schemes have been proposed in literature to help the bit cell to flip during the write cycle. For the SRAMs in which the V_{min} is dictated by write failures, the WA techniques push the V_{min} lower and make it limited by other failure modes, say read disturb failures. In this work we analyze the efficacy of the leading WA techniques in low power SRAMs in aggressive nanometer technology nodes. Further, we analyze the impact of supply voltage scaling on the efficacy of the WA techniques. We also investigate the impact of these WA techniques on the dynamic read noise margins of the half-selected cells (half-selected cells

exist due to column multiplexing and for these cells the word-line is asserted but the bit-lines are not pulled low). Understanding the impact of technology and voltage scaling on the efficacy of write-assist schemes is crucial in designing low power SRAMs.

II. 7T and 8T CELL DESIGN

The 7T dual-Vt SRAM cell is presented in this section. The circuit schematic of the SRAM cell with transistors sized for an 180nm CMOS technology is shown in Fig. 2. The cross-coupled inverters formed by the transistors N1, P1, N2, and P2 store a single bit of information. The write bitline WBL and the pass transistor N3 are used for transferring new data into the cell. Alternatively, the read bitline RBL and the transistor stack formed by N4 and N5 are used for reading data from the cell. Two separate control signals RWL and WWL are used for controlling the read and the write operations, respectively, with the circuit as shown in Fig. 2. Prior to a read operation, the RBL is pre-charged to V_{DD}. To start the read operation, the read signal R transitions to V_{DD} while the write signal W is maintained at V_{GND}. If a "1" is stored at Node1, RBL is discharged through the transistor stack formed by N4 and N5. Alternatively, if a "0" is stored at Node1 RBL is maintained at V_{DD}. The storage nodes (Node1 and Node2) are completely isolated from the bitlines during a read operation. The data stability is thereby significantly enhanced as compared to the standard 6T SRAM cells. The RBL is conditionally discharged through the N4-N5 stack during a read operation. The transistors of the cross-coupled inverters are not on the read-delay-path. The transistor sizing of the dual-V_t cross-coupled inverters therefore does not affect the read speed of the SRAM cell.

In the 8T SRAM, the write and read bits are separated. While bit and bit-bar lines are used for writing data in the traditional 6T SRAM, only the WBL in Figure 2 is used in the proposed SRAM cell to write for both "0" and "1" data. The writing operation starts by disconnecting the feedback loop of the two inverters. By setting RWL signal to "0", the feedback loop is disconnected. The data that is going to be written is determined by the WBL voltage. If the feedback connection is disconnected, SRAM cell has just two cascaded inverters. WBL transfers the complementary of the input data to Q2, cell data, which drives the other inverter (P2 and N2) to develop Q_bar. WBL have to be pre-charged "high" before and right after each write operation. When writing "0" data, negligible writing power is consumed because there is no discharging activity at WBL. To write '1' data at Q2, The WBL have to be discharged to ground level, just like 6T SRAM cell. In this case, the dynamic power consumed by the discharging is the same as 6T SRAM. The write circuit does not discharge for every write operation but discharges only when the cell writes "1" data, and the activity factor of the discharging WBL is less than "1", which makes the proposed SRAM cell more power effective during writing operation compared with the conventional ones. All the RBL lines are pre-charged before any READ operation. During read operation, transistor N5 is turned on by setting RWL signal high and the READ_ROW(RD) is "high" to turn on N6. When Q2="0", the N4 is off making the RBL voltage not change from the pre-charged value, which means the cell data Q2 holds "0". On the other hand, If Q2= "1", the transistors N4 and N6 are turned on. In this case, due to charge sharing, the READ_BIT voltage will be dropped about 100~200mV, which is enough to be detected in the sense amplifier.

III. Proposed 7t Sram

The schematic of seven transistor (7T) SRAM cell is shown in figure 2. In this section, a new 7-transistor SRAM cell which have low leakage current in stand-by-mode. The gated-ground 7T cells are deemed superior in the high performance process, while traditional 6T cells are deemed the best in the low power process. The 7 cell investigated in the seven transistor (7T) gated ground SRAM cell depicted in fig 3.This cell has an additional NMOS transistor placed in the ground path of a traditional 6T SRAM cell to reduce leakage while the cell is in standby mode.

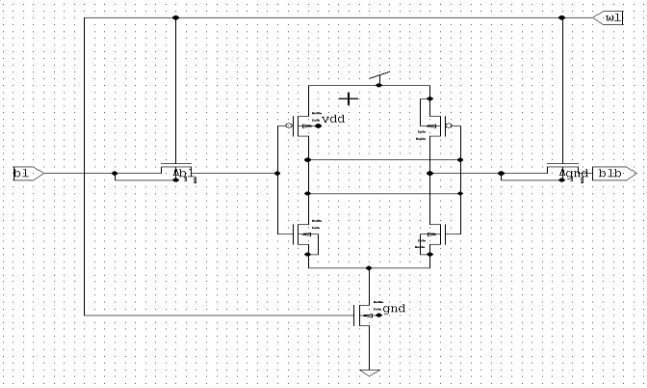

Fig. 4. Schematic of proposed 7T SRAM bitcell

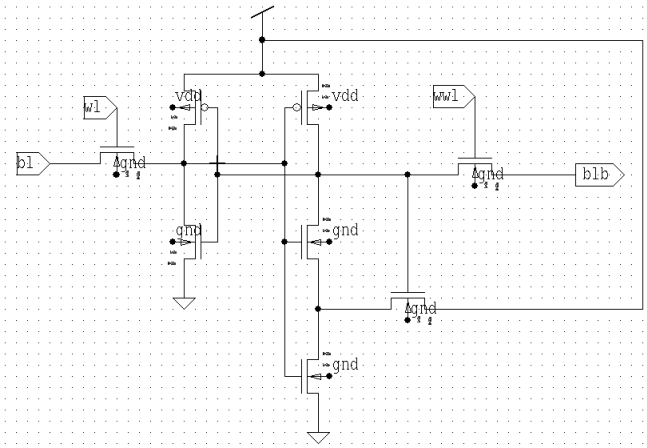

Fig. 5. Schematic of 8T asymmetric ST bitcell

In practice has shown that the cell retains its value during standby even in the absence of a ground rail. In this study, the bottom transistor's gate is connected to the WORD line. The bottom transistor is sized identically to the inverter NMOS transistor to match their current carrying capacity.

A. Write operation of 7T SRAM cell

To write "1" to the storage node Q, at first, BL and BLB are respectively charged and discharged, WL is set to low to turn P1 and P2 on. Next WL is maintained at a low voltage to keep N5 off is charged up to high –level by BLB through p3.when Q is charged sufficiently, set WL to high and turn P1 and P2 off. In contrast, to write "0" to the node, BL and BLB are discharged are charged respectively. There is no additional power consumption even if the write and read cycle come alternately, because there is no mismatch between the voltages level of bit lines in read cycle and that in write cycle.

B. Read operation of 7T SRAM cell

Given that Q stores "1",at first ,WL is set to high to turn P1 and P2 off, next WL is maintained at a high voltage to keep N5 ON, BL is discharged through N3 and N5.Whereas BLB stay high because N4 insulates BLB from the GND. The storage nodes Q and QB completely decouple the datum from the BL during a read operation. In contrast when Q stores "0" as long as turning P1 and P2 off, and turning N5 on, the BLB is discharged through N4 and N5.The read operation of the proposed SRAM cell is different from that of the 6T and 4T SRAM cells. In 7T SRAM cell, reading path is separated from writing path.

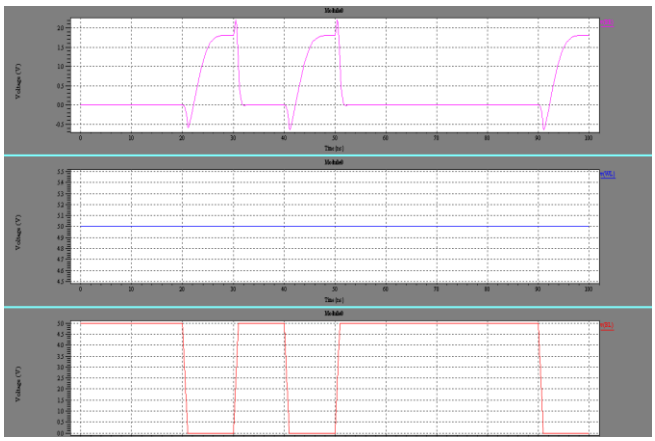

Fig. 6. Waveforms of 7T bitcell in read and write operations

Reading datum does not interfere the storage nodes. Besides, the voltage of the storage node which stores "0" is closely maintained at the ground level during a read operation. Therefore, the 7T SRAM cell has higher endurance against external noise. Fig.6 shows the waveforms of 7T bitcell in read and write operations.

IV. Proposed 8t Sram (8t St Cell)

The proposed system is an 8T asymmetric Schmitt Trigger bitcell (Figure 5). This bitcell uses single-ended reading and asymmetric inverters, similar to the asymmetric 5T bitcell into improve read margin. By using an asymmetrical design, the trip point of the ST inverter is increased, resulting in higher read stability. Because the 5T bitcell has only one access transistor, write assist methods must be used when trying to write a '1' into the bitcell. The advantage that this design has over the 5T bitcell is that it is written like a traditional 6T bitcell, which eliminates the need for write assist methods.

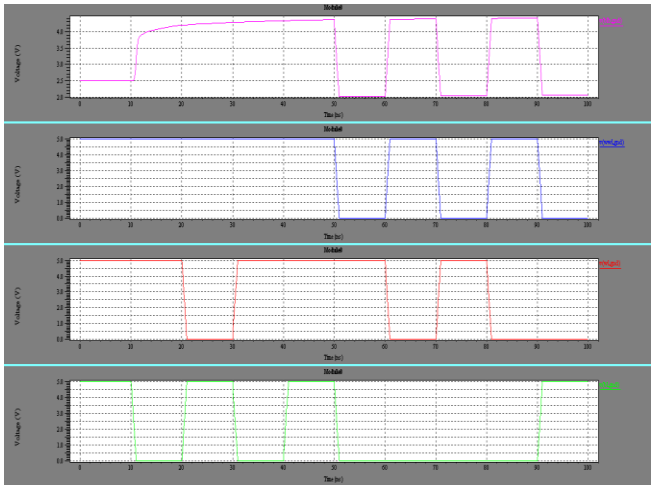

Fig. 7. Waveforms of 8T asymmetric ST bitcell in read and write operations

The WL is pulsed high during both a read and write, and the WWL is only pulsed high during a write. In simulation bitcell achieves 86% higher RSNM than the 6T cell and 19% higher RSNM than the 10T ST bitcell with no VT variation added. Fig.7 shows the waveforms of 8T asymmetric ST bitcell in read and write operations.

V. Circuit Simulation And Results

The simulation results is presented is obtain by T-Spice and process parameter for the 180nm, 120nm CMOS technology using tanner 13.0v. Compared the 7T and 8T with proposed method and measured the power. The measured average power is obtained in the Table I. The comparison is done by using stick diagram in Fig. 8.

TABLE I
COMPARISION OF BITCELL IN 180nm

Analysis	Existing Method		Proposed Method	
	7T bitcell	8T bitcell	7T bitcell	8T ST bitcell
Average Power(watts)	2.2352 e+004	3.1794 e+004	2.0834 e+000	2.0808 e+000
Maximum Power(watts)	5.0782 e-003	6.3588 e-003	8.8625 e-003	1.0773 e-003
Minimum Power(watts)	7.1971 e-008	7.8541 e-008	1.6786 e-007	3.6863 e-007
Area W*L(µm)	14*8.4	15.5*7.9	14*8.4	15.5*7.9

From the circuit results it is clear that the average power is reduced in the proposed systems and can improve the V_{min} of the SRAM.

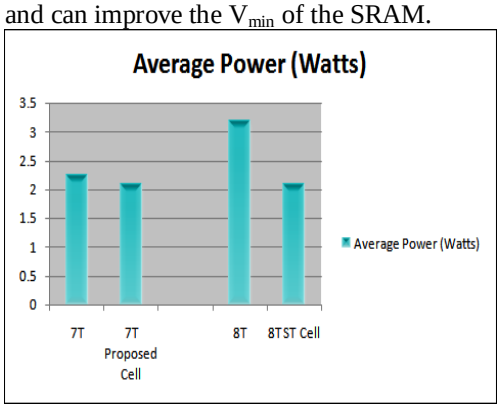

Fig. 8. Stick Diagram indicating the Average Power of proposed systems

VI. Conclusion

In this paper we presented 7T and 8T SRAM bitcell topologies are analyzed for achieving low voltage operation. In terms of power the read and write assist technique, significant improvement compared to proposed technique. The power of the V_{min} is reduced more than 45% and area is not overhead.

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