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Design of a Decimator Filter for Novel Sigma-Delta Modulator

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Abstract*: In this paper, the designing of decimation filter for sigma-delta (∑-Δ) ADC having different oversampling ratio (OSR) is described. The decimation filter perform the operation of down sampling of a high frequency, low resolution signal to Nyquist rate, high resolution digital output. The design of a decimation filter is projected that employs IIR-FIR structure; second order Cascaded Integrator Comb (CIC) filters. This approach eliminates the need for multiplication, requires a maximum clock frequency equal to the sampling. Specifications of decimation filter are dependent upon the overall specification from Σ-Δ A/D converter with sampling frequency 5 MHz. The design implements a decimation ratio of 16, 64 allows a maximum resolution of 9,13 bits in the output of the filter respectively and implemented in 0.25µm CMOS technology. The overall objective is to optimize the decimator in terms of performance and reliability .This paper examines the practical design criteria for implementing the decimator in ∑-Δ ADC.*

Keywords - *cascaded integrator comb filter (CIC), IIR-FIR Structure, oversampling ratio (OSR), sigma-delta modulator, SPICE.*

I. INTRODUCTION

Over the last three decades there were tremendous developments going in the area of digital signal processing supported by the development of integrated circuits. Since most of the signals in this world are analog, they need to be converted to digital form for processing. This is done with the help of Analog to Digital converters. Different types of analog to digital conversion techniques are available today, each having its own advantages and disadvantages. Comparing with different ADC architectures, sigma delta ADC provides high resolution in low and medium frequencies which makes them suitable for medical application and audio application. A sigma-delta A/D converter consists of two parts: an analog oversampled modulator and a digitally implemented decimation filter [1]. The decimation filter relaxes the requirement of high precision analog circuits in the modulator stage and increases the output resolution of ADC. A first order sigma-delta modulator integrated with a second order decimation filter to form a sigma-delta ADC is simulated in SPICE with MATLAB as the computing software package. The 1-bit output of the modulator is used as the input to decimation filter implemented in 250nm CMOS technology.

II. SIGMA DELTA CONVERTER ARCHITECTURE

Analog-to-digital converters can be categorized into two types depending upon the sampling rate [2]. The first kind samples the analog input at the nyquist frequency Fn such that Fs = Fn = 2 * B, where Fs is the sampling frequency and B is the bandwidth of the input signal. The second type of ADCs samples the analog input at much higher frequencies than the nyquist frequency and are called oversampling ADCs [2], sigma-delta ADCs come under this category. In sigma-delta ADC, the input signal is sampled at an oversampling frequency Fs = K * Fn where K is defined as the oversampling ratio and is given by:

$$K = \frac{\mathrm{Fs}}{2\mathrm{B}} \qquad (2.1)$$

The block diagram of a sigma-delta ADC is shown in Fig. 2.1. The modulator samples the analog input signal at much higher frequencies set by the oversampling ratio and converts the analog input signal into a pulse density modulated digital signal containing both the original input signal and the unwanted out-of-band noise [2]. A decimation filter following the modulator filters out the out-of-band noise. Both the modulator and the decimator are operated with the same oversampling clock. In Fig. 2.1, the modulator shown is of first order with a 1-bit quantizer and generates a 1-bit output. The output of the decimator is shown as N-bit digital data, where N is the output resolution of the ADC and is dependent on the oversampling ratio. The order of the decimator depends on the order of the modulator. The order of the decimator is one more than the order of the modulator.

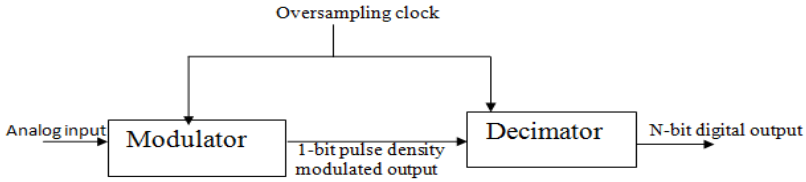

Fig 2.1 Block Diagram of Sigma-Delta Analog to Digital Converter

An economical hardware implementation of a multistage decimation filter can be done using Cascaded Integrator Comb filter (CIC) with the transfer function:-

$$H(z) = \left(\frac{1 - z^{-k}}{1 - z^{-1}} \right)^{L} \qquad (2.2)$$

Where k is the oversampling ratio, L is the order of the decimator filter (L=2). Figure 2.2 shows the direct implementation of decimator. Since the whole circuit is working at sampling frequency, Fs (Fs = k * Nyquist rate) the power consumption of the circuit is high [3].

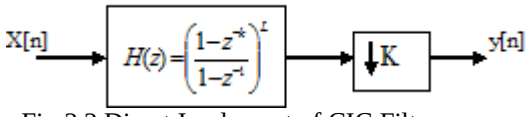

Fig 2.2 Direct Implement of CIC Filter

So, different decimation filter architectures are required. These are IIR-FIR structure, Non-recursive structure and Polyphase structure. But after the analysis it has been shown that IIR-FIR structure has highest power consumption, minimum area on chip, Polyphase structure requires maximum area and minimum power consumption [4]. In this paper we are using IIR-FIR structure A simplified implementation of CIC filter is shown in Fig. 2.3. In this circuit, the IIR filters work at fs and the FIR filter works at Nquist rate (F_n). So the power consumption of this architecture is reduced significantly. Moreover the area is reduced due to the reduction of registers and adders. To avoid register overflow the word length of the IIR filter should be b+ $\log_2 K$, where b is the length of the output of modulator (here b = 1) [4]. Here IIR filter can be implemented as digital integrator, FIR filter can be implemented as digital differentiator in SPICE.

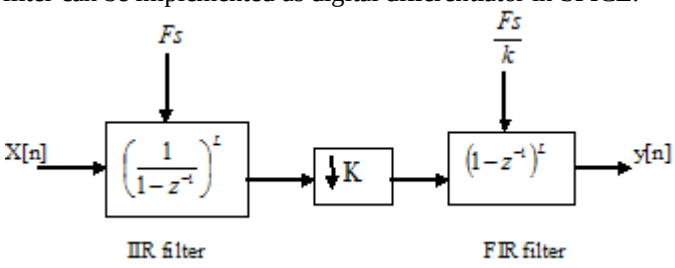

Fig 2.3 Block Diagram of IIR-FIR Decimator Filter Structure

III. SPECIFICATION OF THE DECIMATION FILTER FOR SIGMA DELTA CONVERTER

A sigma-delta A/D-converter consists of a sigma-delta modulator, which produces the bit stream at the sampling rate, which can be in the megahertz range. The figure 2.1 shows a digital side of sigma-delta modulator. The specifications of the decimation filter are dependant upon the overall specification from the sigma-delta converter. These are summarized in Table 1.

TABLE1
SIGMA-DELTA ANALOG TO DIGITAL CONVERTER

Parameter	Symbol	Value1	Value2
Signal bandwidth:	BW	50 KHz	50KHz
Sampling Frequency:	Fs	5 MHz	5MHz
Over Sampling Ratio:	OSR	64	16
Modulator order:	M	1	1
Number of bits in modulator bit stream:	Bmod	1	1
Number of bits in output of filter:	B	13	9

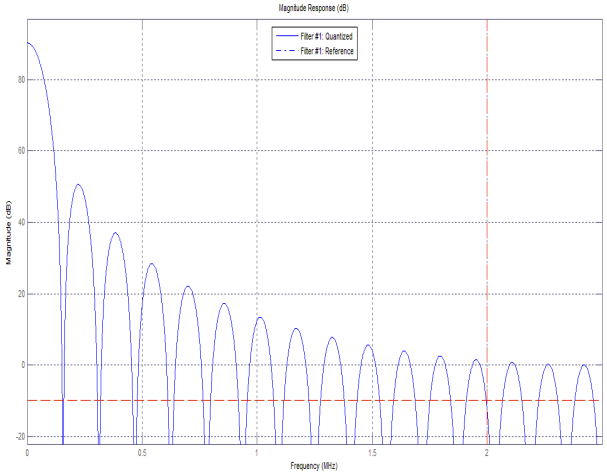

Fig 3.1 Magnitude response of CIC filter(k=16)

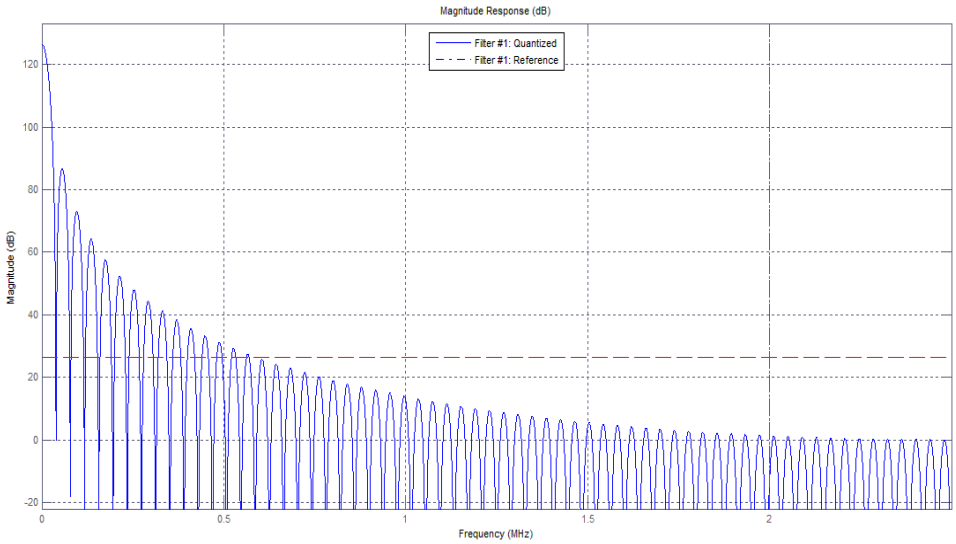

Fig 3.2 Magnitude response of CIC filter(k=64)

IV. DESIGN OF SECOND ORDER PROGRAMMABLE DECIMATION FILTER

The block diagram of the decimator designed in this work is shown in Figure 4.1. The input to the decimator is a 1-bit pulse density modulated signal from a second order sigma-delta modulator. The output from the decimator is a 13 bit digital output. The different blocks were designed to be implemented in 250nm CMOS technology. The tool required to build each block was designed using T-SPICE in Tanner *v* 15.14.

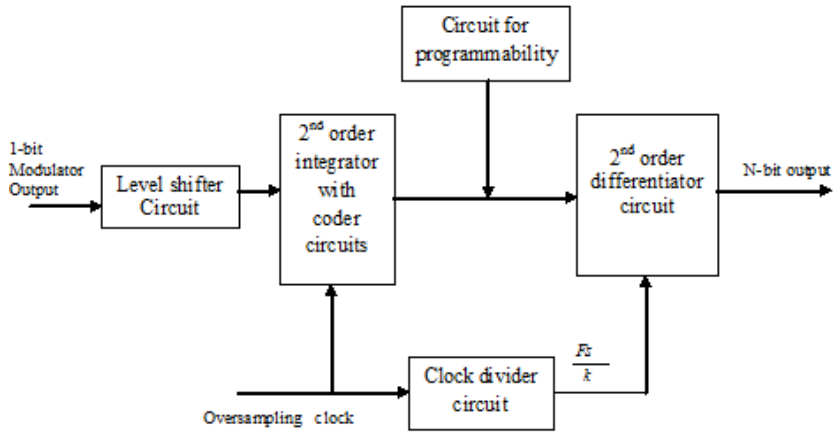

Fig 4.1 Block diagram of the proposed decimation filter

4.1 Coder Circuit

The purpose of the coder circuit is to increase the resolution of the ADC. The output from the second order modulator is one bit binary, i.e. it is either 1 or 0. A register overflow might occur at the multiples of Fs due the infinite gain. This register overflow can be avoided if the register length of the integrator is chosen according to equation (10) and also by using the 2's complement method of coding. The two outputs of the coder circuit for binary 1 and 0 inputs are shown in Table 2.

TABLE2
OUTPUT OF CODER CIRCUIT

	Coder circuit 1		Coder circuit 2	
	input	**output**	**input**	**output**
For k= 64	1	0000001	1	0000000
	0	1111111	0	1111111
For k= 16	1	00001	1	00000
	0	11111	0	11111

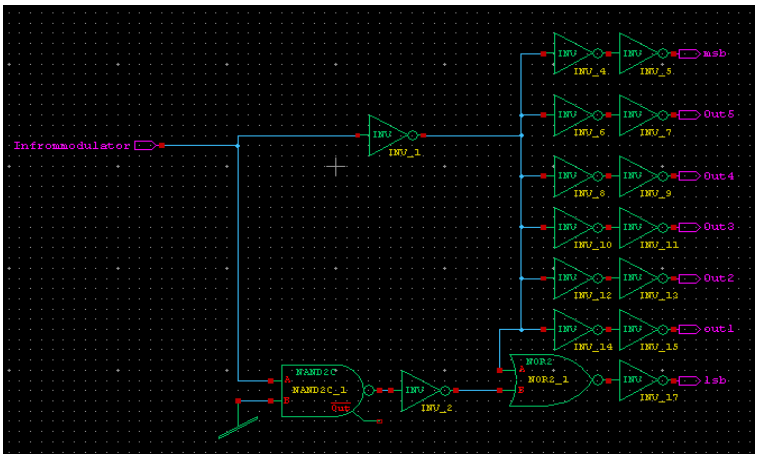

Fig 4.2 Schematic of coder circuit

4.2 Clock Divider Circuit

The function of the clock divider circuit is to divide the clock frequency by the oversampling ratio, K=64. The input to the clock divider circuit is the oversampling clock, Fs, which is also used as the clock for the modulator. Hence, the output of the clock divider is Fs/64 and is applied to the differentiator circuit of the CIC filter [5]. The clock divider circuit is designed using negative edge triggered T-flip flops and AND logic gates.

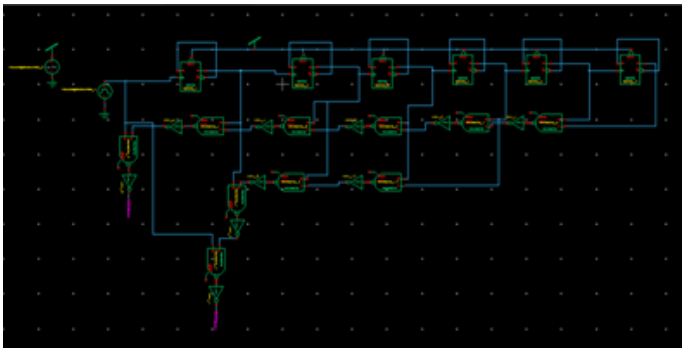

Fig 4.3 Schematic of clock divider circuit

4.3 Delay Element

A delay element is a register circuit, which is used to provide a delay by one clock period. The integrator and differentiator circuits of a 2nd order CIC filter requires 46 delay elements. The integrator block alone requires 20 delay elements. The differentiator block requires 26 delay elements. Hence it is very important to design a delay element which is area efficient and has smaller rise and fall times. A delay element can be implemented using a combination of switches and inverters.

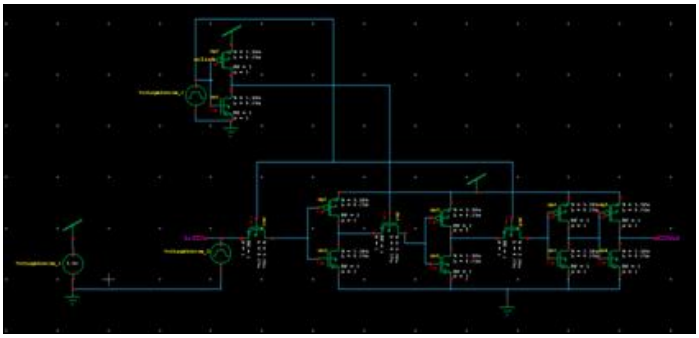

Fig 4.4 Schematic of delay element

4.4 Circuit for Programmability

The CIC filter has been designed to work for two oversampling ratios and this is made possible with the use of the circuit for programmability. This circuit works with the coder circuit -2 defined in the above section to give correct inputs to the second stage integrator for the two oversampling ratio cases. Referring to Fig. 4.5, for case K = 64, the MSB of the 7-bit output of the first stage integrator is complemented by the coder circuit-2 and extended to form a 13- bit data so that the second stage integrator works with 13-bits of data. But for K = 16 case, the second stage integrator should work with 9-bit data and only the first 5-bits of the first stage integrator output should be considered. For K = 16 case, the 5-bits from the first stage integrator are to be extended to 9-bits two's complement data and to do this the 5th bit output of the first stage integrator has to be complemented and the complemented value should be substituted from 5th bit to the 9th bit.

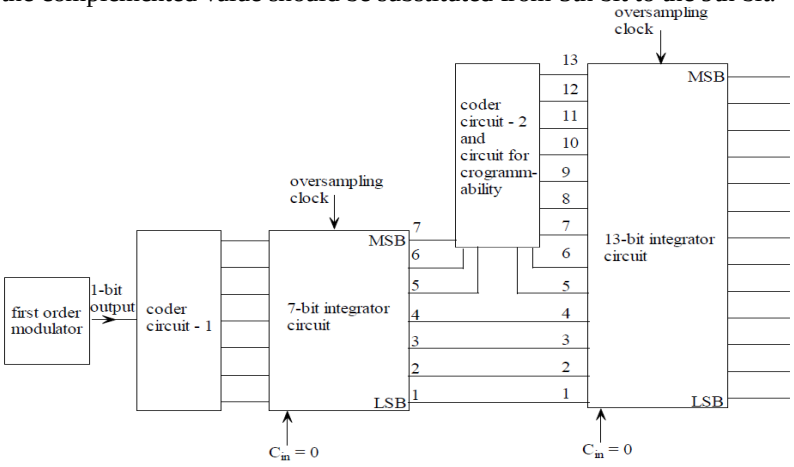

Fig 4.5 Block diagram of the 2nd order integrator circuit

In order to use the same CIC filter for both oversampling ratios, a circuit has to be designed which can program bit 5 to bit 9. The circuit for programmability is designed to solve this problem. The circuit takes an enable signal as an input for choosing either of the two K values. When enable is HIGH, K =16 case is considered and when enable is LOW, K=64 case in considered. The circuit for programmability is shown in Fig. 4.6. The circuit has been divided into three blocks shown as a, b, and c in Fig. 4.6. It should be noted that the complement of bit 5 exists in all the three circuits. When enable is HIGH, K = 16 case is considered and the complement of bit 5 to 13 is applied to the next stage. Even though the circuit has 13-bit output, only the first 9 bits are considered for this case. When the enable signal is LOW, K = 64 is considered and the bits 5 and 6 are transferred from the output of the first stage integrator without any change but the complement of bit 7 is applied as the input to the bit 7 to bit 13 of the next stage. When the enable is LOW, Bit 5 has no valid output so in Fig. 4.6 (c), bit 7 is transferred to the next stage.

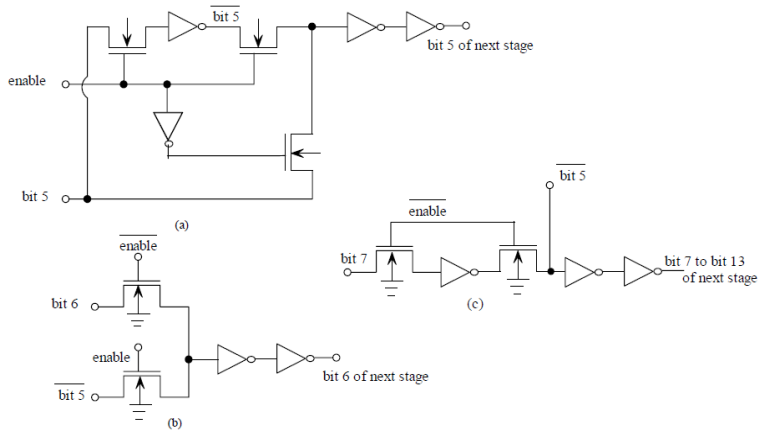

Fig 4.6 Circuits for programming the CIC filter to operate at two different oversampling ratios of 16 and 64.
Note: Bit 5 has a valid value only if Enable = 1, if Enable = 0 it is at high impedance state.

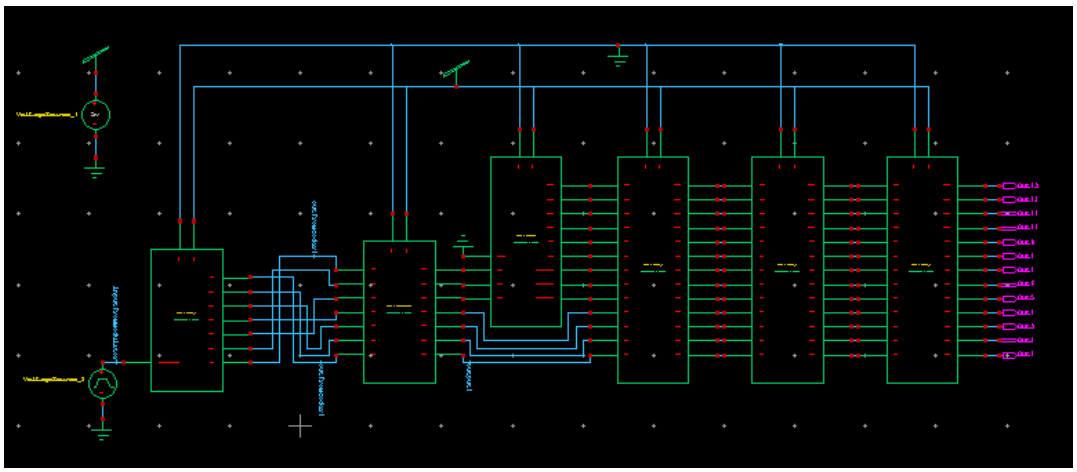

Fig 4.7 Final design of decimator

V. CONCLUSION

An efficient IIR-FIR filter structure has been designed that eliminates the out-of-band noise. This structure can be easily implemented; output sampling rate is the minimum possible one and the same structure can be used for many OSR's. The designed multirate decimator computationally less complicated and architecture is superior over the conventional single stage decimator implementation method. This multirate decimator technique is easy for on-chip VLSI implementation. The implementation of this structure for lower OSR increases the computation instead of decreasing it, in comparison with the single stage implementation. Therefore, at lower OSR a compromise should be made between the computation and area. Hence, multirate decimator technique is an efficient technique for the implementation at higher OSR's.

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