

## Analysis and optimization of Active Power and Delay of 10T Full Adder using Power Gating Technique at 45 nm Technology

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**Abstract :** An overview of performance analysis and comparison between various parameters of a low power high speed 10T full adder has been presented here. This paper shows comparative study of advancement over active power, leakage current and delay with power supply of (0.7v) .We have achieved reduction in active power consumption of 39.20 nW and propagation delay of 10.51 ns, which makes this circuit highly energy efficient and optimization can be achieved between power and delay. In this circuit we have reduced leakage current of 18.21 nA for power supply of 0.5v to 0.9v. Signification of these designs is substance by the simulation results obtained from cadence virtuoso tool at different technologies.

**Keywords** - Full Adder, Leakage Power, CMOS Circuit, Sleep Transistor.

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### I. INTRODUCTION

Today's there are a growing number of portable applications requiring small-area low-power high-throughput circuitry. Therefore, circuits with low power utilization grow to be the most important candidates for design of microprocessors and system mechanism. The battery technology does not advance at the same rate as the microelectronics technology and there is a imperfect quantity of power available for the mobile systems. The goal of extending the battery life span of portable electronics is to reduce the energy consumed per arithmetic operation, but low power consumption does not essentially imply low energy. To execute an arithmetic operation, a circuit can obtain through very low power by clocking at very low frequency but it may take a very long time to complete the operation [1] [2] [3]. An adder is one of the most critical components of a processor which determines its throughput, and for address generation in case of cache or memory access. The full adder performance would affect the system as a whole. A variety of full adders using static or dynamic logic styles have been reported in the literature [4]. In this paper, we propose a systematic approach to design 10-transistor full adders. Our new adders also have the threshold-loss problem; however, the adders are useful in larger circuits such as multipliers despite the threshold-loss problem. A new full adder called static energy-recovery full adder uses only 10 transistors which has the least number of transistors and has reported to be the best in power consumption, according to. Power minimization is one of the primary concerns in today's VLSI design methodologies because of two reasons one is the long battery operating life requirement of portable devices and second is due to increasing number of transistors on a single chip leads to high power dissipation. In VLSI applications, 1-bit full adder cell is the fundamental gate used in many arithmetic circuits like adders and multipliers. Thus, increasing the performance of the full adder block leads to the enhancement of the overall system performance [5], [6]. A full adder has three inputs and two outputs block in which the outputs are the addition of three inputs. Basic fundamental units used in various circuits such as parity checkers, compressors and comparators are full adders [7]. This technique uses high threshold voltage sleep transistor which cut-off a circuit block when the block is not switching [8].

### II. REVIEW OF FULL-ADDER DESIGN

A 1-bit full adder adds three one bit numbers, frequently written as A, B and C. A and B are the operands and C is a bit carried in from the next less important stage. Full adder is typically a part in a cascade of adders' binary numbers [9]. The circuit generates a two-bit output sum typically represented by the signals Carry and Sum. Here a full adder is constructed with the help of two half adders by connecting A and B to the input of first half adder, connecting the sum from that to an input to the second adder, connecting C to the other input and OR the two carry outputs. Also Sum could be made the three bit XOR of A, B, and C and Carry could be made the three-bit common function of A, B, and C. The expression of Sum and Carry outputs of 1-bit full adder based on binary inputs A, B, C are represented as:

$$Sum = A \oplus B \oplus C \quad (1)$$

$$Carry = AB + BC + CA \quad (2)$$

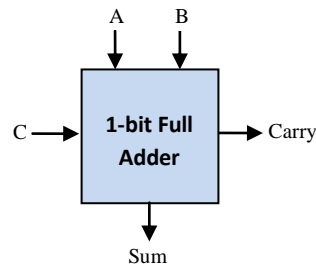


FIGURE 1. BLOCK DIAGRAM REPRESENTATION OF 1-BIT FULL ADDER

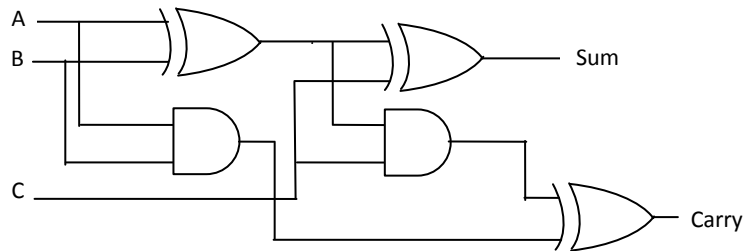


FIGURE 2. SCHEMATIC OF A FULL ADDER

### III. 10T FULL ADDER TOPOLOGIES

A transmission gate or analog switch is defined as an electronic constituent that will selectively block or pass a signal level from the input to the output. This solid condition switch is comprised of a pMOS transistor and nMOS transistor. The control gates are biased in a corresponding method so that both transistors are either on or off [10]. The designed 10T full adder shown in figure 3.

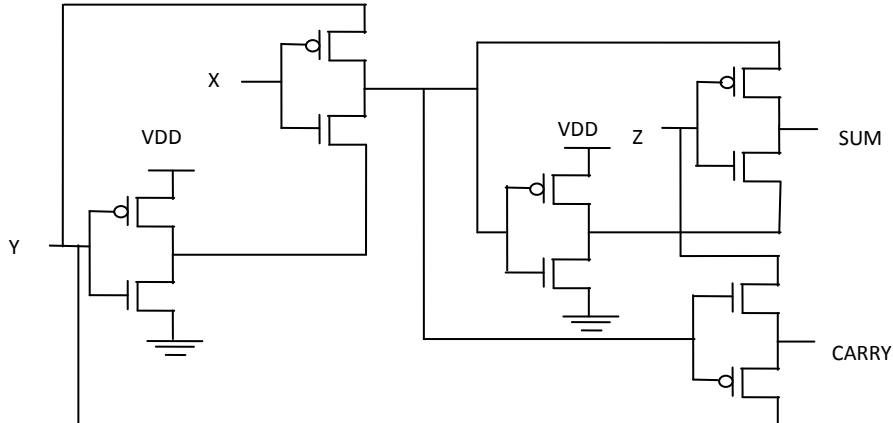
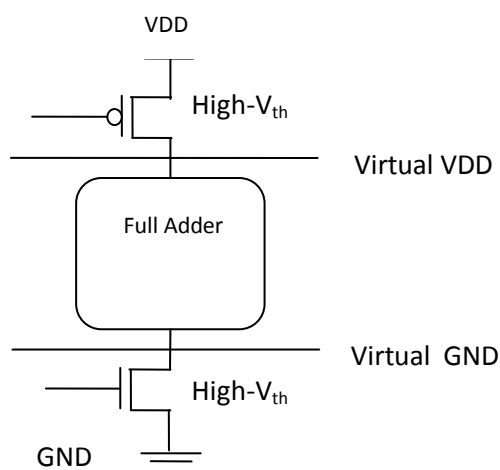


FIGURE 3: SCHEMATIC OF 10T FULL ADDER 45NM TECHNOLOGY

The basic advantage of 10T full adders is smaller area and lower power utilization. It becomes more not easy and even obsolete to keep full output voltage swing operation as the design with fewer transistor count and lower power utilization are pursued. In pass transistor logic the output voltage swing may be degraded due to the threshold voltage defeat problem. The reduction in voltage swing leads to lower power consumption but may also lead to slow switching in the case of cascaded operation such as ripple carry adder. A low VDD operation the corrupted output may even cause break down of circuit [11]. The smallest voltage that 10 T adder can work at 0.7V. The excessive power dissipation and long delay are attributed to the threshold voltage drop problem and the poor driving capability of some internal nodes at input combinations that create non full-swing transitions [12]. The elimination of the path to the ground reduces the total power use by reducing the short circuit power . The combination of low power and low transistor add up makes the SERF adder circuit a viable option for low power design.

#### IV. POWER GATING TECHNIQUE

MOSFET scaling deep into the sub-100-nm system has resulted in Power gating has become one of the most widely used circuit design techniques for reducing leakage current. Its thought is very simple but its application to standard cell VLSI designs involves many careful considerations. The great complication of designing a power-gated circuit originate from the side effects of inserting current switches which have to be determined by a mishmash of extra circuitry and customized tools and methodologies. In this tutorial we analysis these design considerations and look at the best practice within industry and academic world. Topics include output isolation and data with holding current switch design and sizing and physical design issues such as power networks increases in area and wire length and power grid analysis. Standby leakage is in general smaller than active leakage. The device operating at room temperature. substantially greater leakage power consumption compared to a few generations ago [13]. Technology scaling calls for a reduction of the supply voltage to restrain power density [14]. The sleep transistor can be turned off when the low-V<sub>th</sub> logic block is still therefore resulting in a important reduction of sub-threshold leakage current. Figure 4. shows a sleep transistor used for power gating. A sleep transistor can be a high nMOS or pMOS transistor. A pMOS sleep transistor served as a description switch connects the power network to virtual VDD. An nMOS sleep transistor served as a footer switch connects the ground network to virtual GND. Normally, either a header switch or a footer switch is used to conserve area and reduce timing penalty caused by voltage drop across sleep transistors. In this work, we will consider only header switch. The logic network in Figure 4. can be as simple as a logic gate. If it is a logic gate in a standard cell library we call it a power-gated cell. If the power-gated cells in a standard cell design are used in a cut off method i.e. their virtual VDDs are not connected.

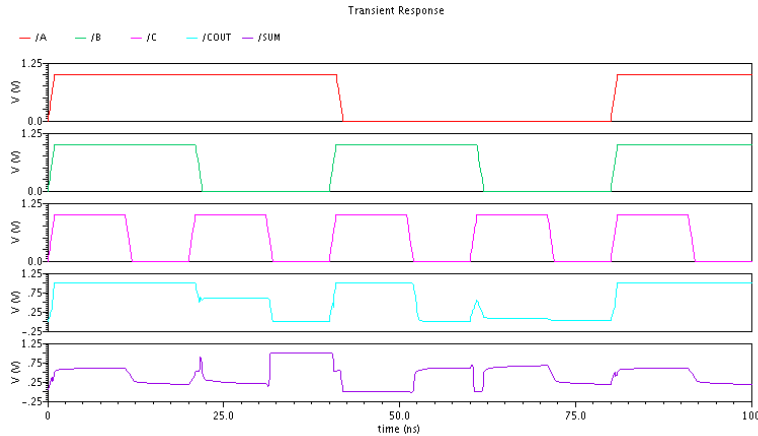


**FIGURE 4: WE CALL THIS POWER GATING APPROACH FINE-GRAINED POWER GATING.**

Power Gating Technique has two main features. First “active” and “sleep” operational modes are associated with Power Gating Technique technology for efficient power organization. Second two different threshold voltages are used for N channel and P channel MOSFET in a single chip [15]. This technique based on disconnecting the low threshold voltage (low-V<sub>t</sub>) logic gates from the power supply and the ground line via cut-off high threshold voltage (high-V<sub>t</sub>) sleep transistors is also known as power gating. The schematic of power gating technique shown in Fig.3. The transistors having low threshold voltage are used to implement the logic. The low threshold voltage transistors from supply and ground during standby (sleep) mode to prevent leakage dissipation [16].

#### V. SIMULATION RESULTS

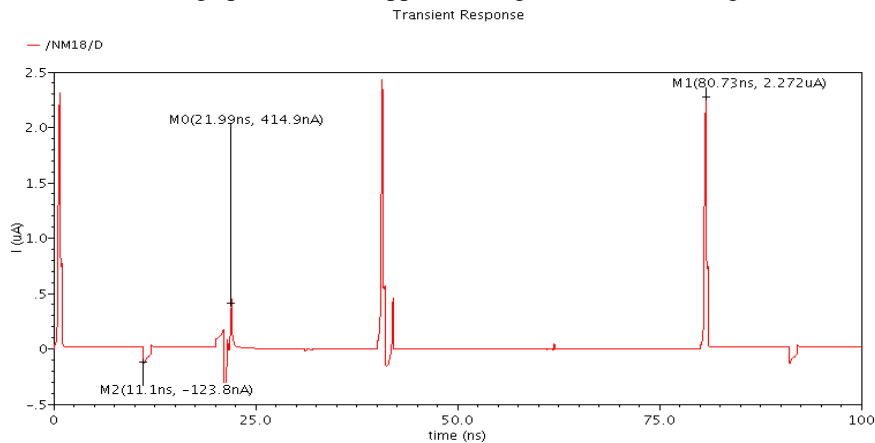
We have performed simulated results using spectre simulator in cadence tool at 45 nm technology. The supply voltage is 0.7v (45nm). The data analysis of the input and output such as a, b, c, sum and carry shown in figure 2. The output waveform of 10T full adder simulated at 45 nm technology under the process of transient analysis for the period of 100ns and power supply of 0.7 V.



**FIGURE 5: SIMULATED OUTPUT WAVEFORM OF TRANSIENT RESPONSE 10T 45NM TECHNOLOGY.** Figure 4 shows the output waveform of leakage current of 10T full adder simulated at 45nm technology under the process of transient analysis for the period of 100ns and power supply of 0.7 V. Leakage current is also the current that flow when the ideal current is zero, such as in electronic assemblies that are in stand by disabled or “sleep” mode.

$$P(V_t) = V_{cc} I_{off}(V_t) \tag{1}$$

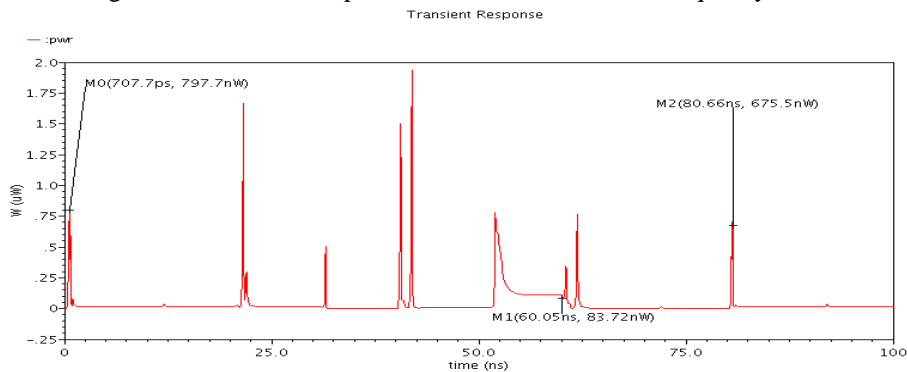
Where,  $P(V_t)$  = leakage power,  $V_{CC}$  = applied voltage and  $I_{off}$  = leakage current



**FIGURE 6: SIMULATED OUTPUT WAVEFORM OF LEAKAGE CURRENT 10T AT 45NM TECHNOLOGY.** Figure 5 shows the output waveform of active power simulated at 45nm technology under the process of transient analysis for the period of 100ns and power supply of 0.7V.

$$P_{avg} = CV_{DD}^2 f_{CLK} \tag{2}$$

Where,  $P_{avg}$  = Average Power, C = load capacitance and  $f_{CLK}$  = clock frequency.

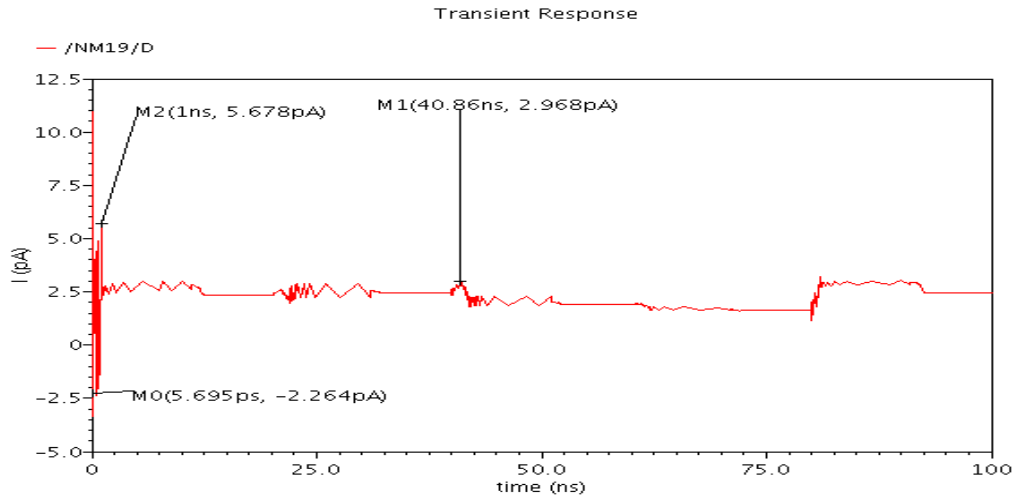


**FIGURE 7: SIMULATED OUTPUT WAVEFORM OF ACTIVE POWER 10T AT 45NM TECHNOLOGY.**

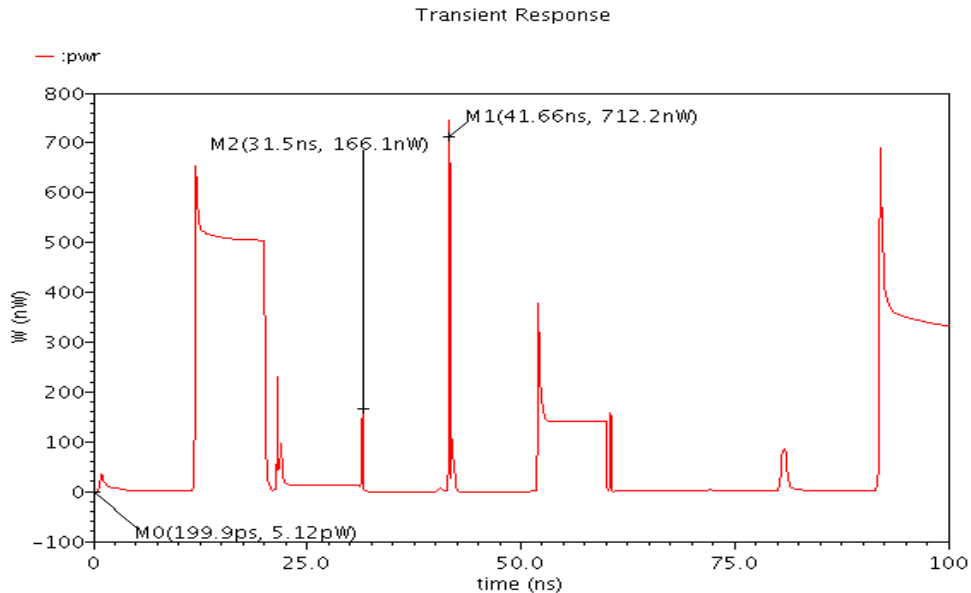
Figure 8: shows the output waveform of leakage current of 10T full adder using power gating technique simulated at 45nm technology under the process of transient analysis for the period of 100ns and power supply of 0.7 V. Leakage current is also the current that flow when the ideal current is zero, such as in electronic assemblies that are in stand by disabled or “sleep” mode.

$$P(V_t) = V_{cc} I_{off}(V_t) \tag{3}$$

Where,  $P(V_t)$  = leakage power,  $V_{CC}$  = applied voltage and  $I_{off}$  = leakage current



**FIGURE 8: LEAKAGE CURRENT OF 10T FULL ADDER USING POWER GATING TECHNIQUE AT 45NM TECHNOLOGY.**



**FIGURE 9: ACTIVE POWER OF 10T FULL ADDER USING POWER GATING TECHNIQUE AT 45NM TECHNOLOGY.**

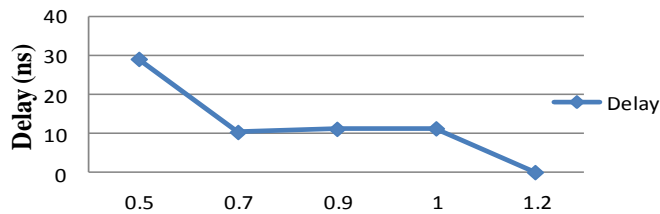
Figure 9: shows the output waveform of active power simulated at 45nm technology under the process of transient analysis for the period of 100ns and power supply of 0.7V.

$$P_{avg} = CV_{DD}^2 f_{CLK} \tag{4}$$

Where,  $P_{avg}$  = Average Power, C = load capacitance and  $f_{CLK}$  = clock frequency.

**VI. RESULT AND DISCUSSION**

Table 1 shows the simulation results for 10T Full adder Performance comparison regarding power, leakage current, and delay and power delay product. All the full adders were supplied with two different technologies. Simulation result also derives the variation in delays. Rise time refers to the time required to change from a specified low value to a specified high value. Fall time (pulse delay time) is the time required for the amplitude of a pulse to decrease fall from a specified value. The average gate delay for rising and falling transition is:

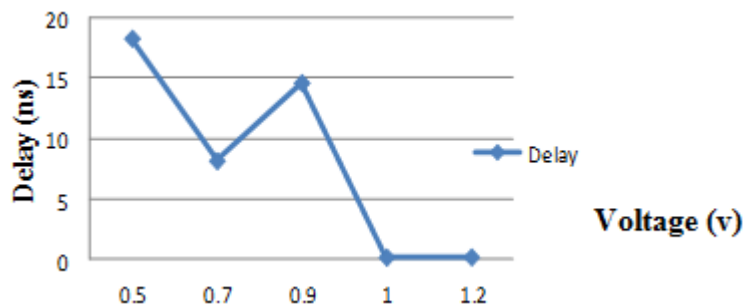


**FIGURE 10: DELAY OF 10T FULL ADDER AT 45NM TECHNOLOGY**

**TABLE 1 : SIMULATION RESULT OF 10T FULL ADDER**

TECHNOLOGY	VOLTAGE (V)	ACTIVE POWER (μW)	LEAKAGE CURRENT (μA)	DELAY	PDP
10T Full Adder	0.5	64.81	18.02	29.17	1890.50
	0.7	39.20	18.21	10.51	411.99
	0.9	41.61	21.54	11.31	470.60
10T Full Adder power Gating Technique	0.5	91.50	16.69	18.34	1678.11
	0.7	89.02	10.43	08.23	732.63
	0.9	64.79	07.48	14.67	950.46

**FIGURE 11: DELAY OF 10T FULL ADDER USING POWER GATING TECHNIQUE AT 45NM TECHNOLOGY**



**VII. CONCLUSION**

The 10T full adder has been simulated here at 45nm technology for calculation of different parameters and is compared with the 10T full adder using power gating technique simulation results at The results show that power consumption of the circuit is reduced to 89.2nW for 0.7V at 45nm and reduces further on reduction of the supply voltage. Delay has also been improved and reduced to 08.23ns at 0.7V at 45nm technology. The comparison shows that the implementation of the 10T full adder using power gating technique would be better at 45nm technology as compared to 10T full adder.

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