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Design of Low Power FFT using Self-sleep Buffer with Body bias Technique

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Abstract : *Leakage power has become an important contributing factor of power for the CMOS circuits in deep sub-micron process. MTCMOS is a very effective technique to reduce the leakage current of circuits in the standby mode. Placing a global sleep device is not practical and sleep device at fine grain level involves more number of sleep transistors and more routing space. Distributed MTCMOS is better technique with self sleep circuit to avoid complexities in routing and sleep distribution network. A simple FFT processor is designed with self sleep buffer using body bias to reduce its standby power. Ccomparisons are made between leakage power for FFT implemented in CMOS and distributed self sleep FFT using the 90nm CMOS technology in cadence tools.*

Keywords – *FFT, Leakage power, MTCMOS, Sleep device, Standby mode.*

I. INTRODUCTION

The Leakage power has become a major concern for the CMOS circuits in deep sub-micron process. As process moves to finer technologies, there is a decrease in the feature size and increase in the device density. Lowering the supply voltage leads to lower threshold voltages and oxide thickness. High device density and low threshold voltages result in a significant increase in the leakage power dissipation [1]. This work deals with technique which reduces the leakage power. MTCMOS is a very effective technique to reduce the leakage current in the standby mode. The principle of the MTCMOS technique is the employment of low V_{th} transistors to design the logic gates for which the switching speed is essential, and the high V_{th} transistors, also called sleep transistors to effectively isolate the logic gates in the standby state and reduce the leakage dissipation.

Although MTCMOS is a very effective technique, it introduces some overheads and design challenges. The area penalty due to the sleep transistors is one of the MTCMOS overheads. Correct sizing of sleep transistor is required since over-sizing leads to an extra unnecessary area penalty and under-sizing leads to performance degradation and reduced noise margin. Signal integrity is another issue that should be considered during standby-to-active transition. Also, MTCMOS latches and flip-flops must retain the data in sleep mode.

MTCMOS design styles

MTCMOS design style is applying a sleep signal at different levels. It can be at gate level or block level. A block is defined as a circuit whose elements share the same sleep signal. Depending on the system-level design, a block can be a whole chip, a core, a clock/V_{DD} domain, a data path, and it can be a global bus as well. Applying MTCMOS design to a block can be done in several ways.

1.1. Global MTCMOS

Global MTCMOS controls the whole block via a large centralized single sleep transistor. Global MTCMOS style has the lowest optimal total sleep transistor area. However, determining the optimal size of the global sleep transistor is hard, and impractical for large blocks. This complicates the design and leads, in most cases, to an over-sized sleep transistor, which in turn reduces the efficiency of global MTCMOS in terms of area. Regarding signal integrity, global MTCMOS is also impractical since it suffers from degraded noise margin and large ground bounce in power/ground networks. Figure 1 shows the placement of sleep device in global MTCMOS circuit.

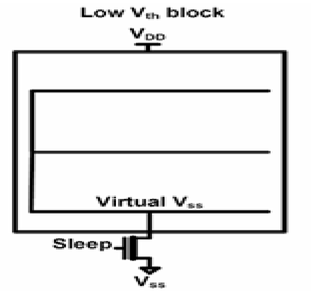


Figure 1: Global MTCMOS

Global MTCMOS does not require intra-block sleep signal routing but it suffers from high virtual power/ground lines sizing and routing complexity. In deep submicron technologies, the increased power density coupled with reduced supply voltage and increased interconnect resistance make global MTCMOS not feasible [2-3].

1.2. Fine Grain MTCMOS

In fine grain MTCMOS each gate has its own sleep Device as shown in figure 2. Determining the optimal sleep transistor size for fine-grain MTCMOS is easy. However, the area penalty is large. Fine-grain MTCMOS has the best signal integrity since the virtual power/ground are embedded within the gates. Fine-grain MTCMOS does not require virtual power/ground traces, but the sleep signal has to be delivered to all gates. Fine-grained MTCMOS offers many desirable advantages in terms of signal integrity and sleep transistor sizing complexity. However, it can only be considered when the sleep transistor area penalty can be tolerated [4].

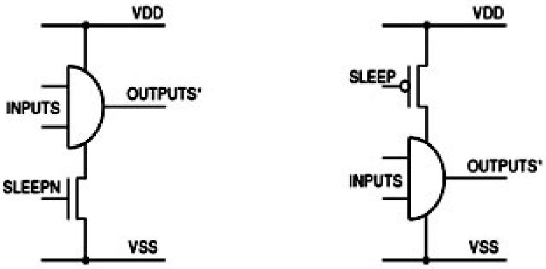


Figure 2: Fine Grain cells

1.3. Distributed MTCMOS

Distributed MTCMOS design shown in Figure 3 employs multiple sleep transistors for a single block. It can be applied in two ways. One way is cluster based, where a block is divided into clusters and each cluster has its own virtual power/ground and sleep device. Clustering is done based on the switching behavior of the gates to minimize the total sleep transistor area. Another way for distributed MTCMOS design is network-based, also known as coarse-grain where many distributed sleep transistors are inserted between the actual and virtual power/ground networks inside the block [5]. In this type of network the sleep transistors share the charge/discharge currents. Distributed sleep transistor network was shown to be better than distributed clusters in terms of sleep transistor area and performance. Distributed MTCMOS styles simplify sleep transistor sizing compared to global MTCMOS, and reduce the total sleep transistor area compared to fine grain MTCMOS.

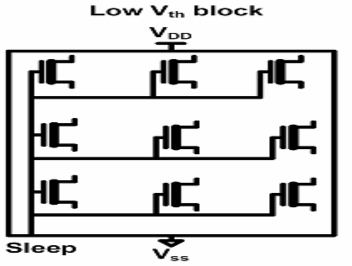


Figure 3: Distributed MTCMOS

Previous projection indicates that repeaters and buffers required for intra-block signaling will take70% of the total block cell count at the 32-nm node [6].Therefore, adding extra intra-block signals and buffers is not desirable. Distributed Cluster and network based MTCMOS are the most commonly used in industrial designs since they combine the advantages of both global and fine-grain MTCMOS. Moreover, unlike fine-grain style, distributed MTCMOS styles use the same standard-cells provided by library vendors.

2. Short Comings of Distributed MTCMOS

In distributed MTCMOS, the sleep distribution network presents an overhead since the sleep signal has to be routed to all the sleep devices within the block. The sleep network is a multi-sink network which adds considerable routing complexity. Regular sleep transistor placement reduces the sleep signal routing complexity. However, the sleep signal still consumes precious routing resources and increases the total intra-block wire length, which in turn increases design cost. Moreover, sleep signal buffers consume leakage power in active and standby modes, and complicate buffer floor-planning and sleep signal routing.

Important metrics that greatly affect MTCMOS efficiency include active-to-sleep and sleep-to-active energy overheads. These metrics determine the minimum standby period that achieves overall power saving. Charging/discharging the sleep distribution network and its associated buffers introduce energy overhead comparable to the energy overhead of charging/discharging the virtual power/ground networks. Also sleep signal network delay affects performance since it is also a major contributor in the total standby-to-active delay. Moreover, sleep signal network requires careful timing analysis to accurately determine the wake-up delay. With all these complexities related to sleep signal distribution in distributed MTCMOS design styles, the integration density of a single block continues to increase.

In this work, the distributed MTCMOS challenges related to sleep signal distribution are targeted. The sleep network grows as the block size increases and more sleep transistors are employed. Distributed MTCMOS self-sleep buffer that is capable of generating a sleep signal based on the clock behavior is proposed.

II. SELF-SLEEP BUFFER

NMOS and/or PMOS devices can be used for ground and/or power gating respectively. However, NMOS is preferred due to its reduced on-resistance compared to same size PMOS. During standby mode, the sleep transistors are turned off to disconnect the logic cell from the actual power/ground lines. During active mode, the sleep transistors are turned on to maintain the functionality of the circuit. The energy and performance overheads of going from active-to-standby and standby-to-active should be minimized. Also, MTCMOS requires extra routing due to the virtual power/ground lines, and sleep signal distribution. The latter, which is a major issue in distributed MTCMOS.

1. Necessity of Self Sleep Buffer

In distributed MTCMOS cluster-based or network based, the sleep distribution network presents an overhead since the sleep signal has to be routed to all the sleep devices within the block. The sleep network is a multi-sink network which adds considerable routing complexity. Regular sleep transistor placement reduces the sleep signal routing complexity. However, the sleep signal still consumes precious routing resources and increases the total intra-block wire length, which in turn increases design cost.

Maintaining good signal integrity in the sleep distribution network is essential, especially for cluster based design where all the charging/discharging currents flow through a single sleep device. Sleep distribution network noise during active mode, as shown in Figure 4, increases the on-resistance of the sleep device and reduces its overdrive, which in turn degrades circuit performance and noise margin. This noise issue is critical for cluster based design since a single sleep transistor is shared by all the gates in the cluster.

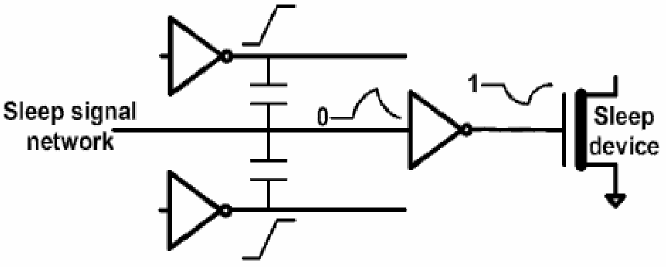


Figure 4: Sleep signal crosstalk noise during active mode.

Therefore, the increased ON resistance of the sleep device affects all the gates performance. If such noise occurs during the peak current switching of the cluster, functional failure might occur. Buffering and shielding the sleep signal greatly helps in this issue. However, shielding increases the wiring cost and area. Whereas, buffering increases area and active-to standby-to-active power overhead. Moreover, sleep signal buffers consume leakage power in active and standby modes, and complicate buffer floor-planning and sleep signal routing.

Important metrics that greatly affect MTCMOS efficiency include active-to-sleep and sleep-to-active energy overheads. These metrics determine the minimum standby period that achieves overall power saving [7]. Also, sleep signal network delay affects performance since it is also a major contributor in the total standby-to-active delay. Moreover, sleep signal network requires careful timing analysis to accurately determine the wake-up delay. With all these complexities related to sleep signal distribution in distributed MTCMOS design styles, and as the integration density of a single block continues to increase, design methods that take sleep signal distribution into account should be considered.

2. Advantages of self-sleep buffer

For distributed cluster-based and network-based MTCMOS, a self-sleep buffer is assigned to each sleep transistor. The number of stages and the transistor sizes of the self-sleep buffer are based on the size of the sleep device. But, the self-sleep buffer eliminates the need for distributing a sleep signal to all the sleep devices since it uses the available clock signal as its input. As a result, the total intra-block wire length, routing complexity, and interconnect buffers are reduced. Sleep signal integrity during active mode is improved by the self-sleep buffers. The first reason for that is the very high resistance of the body biased PMOS. This makes the self-sleep buffer a noise filter during active mode, which helps in maintaining a glitch free sleep signal. The second reason is that the self-sleep buffer is driven by the clock signal which is the most well designed signal on the chip.

Moreover, the delay and power characteristics of the clock network are known, which eliminates the need for extra design effort in characterizing the delay and energy of the sleep network and maintaining its signal integrity. Scheduling the sleep signals inside the block to reduce ground bounce during sleep-to-active transition can be done easily by adding various delay elements to the self-sleep buffers. Also, the timing relation between the sleep signal and the clock is well determined, which helps in timing synchronization when going from standby to active mode.

The active-to-sleep and sleep-to-active MTCMOS energy overheads are reduced with the self-sleep buffer due to the elimination of the charging/discharging of the sleep signal interconnect and its associated buffers. The clock signal is gated in the presence of a sleep distribution network as well, thus clock switching during active-to-standby and standby-to-active transitions cannot be considered as overhead for self-sleep buffer method. The reduction in MTCMOS energy overhead during mode transitions reduces the minimum standby period that is required to achieve overall power reduction, and helps in switching more frequently between active and standby modes[7].

III. Self Sleep Buffer With Body Bias

Body effect refers to the change in the transistor threshold voltage V_{th} resulting from a voltage difference between the transistor source and body. Because the voltage difference between the source and body affects the V_{th}, the body can be thought of as a second gate that helps determine how the transistor turns on and off.

Body bias involves connecting the transistor bodies to a bias network in the circuit layout rather than to power or ground. The body bias can be supplied from an external, off-chip source or an internal, on-chip source. In the on-chip approach, the design usually includes a charge pump circuit to generate a reverse body bias voltage and/or a voltage divider to generate a forward body bias voltage. Reverse body bias, which involves applying a negative body-to-source voltage to an n-channel transistor, raises the threshold voltage and thereby makes the transistor both slower and less leaky. Forward body bias, on the other hand, lowers the threshold voltage by applying a positive body-to-source voltage to an n-channel transistor and thereby makes the transistor both faster and more leaky. The polarities of the applied bias described above are the opposite for a p-channel transistor.

By taking advantage of the body effect phenomenon the sub threshold leakage current can be exponentially reduced. In addition, the gate to source voltage, V_{gs} becomes negative. The net effects are that the transistor is turned off more strongly and the leakage currents can be reduced during the standby mode.

In order to fully reduce power during standby mode, when a block goes into standby, its sleep transistors, as well as its clock, are turned off. This method, uses the relation between sleep signal and the clock in order to eliminate the sleep distribution network.

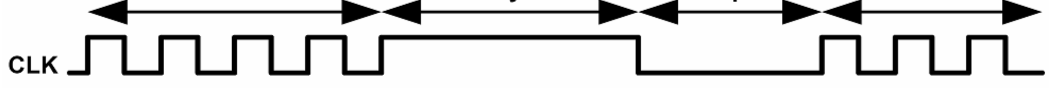


Figure 5: Operation modes based on clock signal.

It is assumed that the clock is gated high, as shown in Figure 5. Before the block switches back to active mode, the clock goes low, which indicates a wake-up period. The wake-up time depends on the distributed MTCMOS style being used. Also, several MTCMOS techniques that were previously proposed can be employed during this mode to achieve better signal integrity and lower energy. After the wake-up period, the block resumes its normal operation.

Figure 6 presents a two stage dual-V_{th} self-sleep buffer. The self-sleep buffer outputs the sleep signal based on the clock. In the active mode and during the low-phase of the clock, node X is low and node S (sleep) is high. During the high-phase of the clock, node X starts charging. The self sleep buffer should be designed such that at the worst corner, the voltage at node X cannot reach a level that causes a glitch at node S. Therefore, node S remains high during all the active period. Transistors N2 and P2 have high and low V_{th}, respectively.

This increases the high to low switching threshold of the second stage inverter in the buffer, which helps in maintaining a glitch-free node S. Transistors N1 and P1 have minimum size channel length and width, in order to maintain the minimum possible clock loading. In the case of a large sleep device, extra stages can be added to the buffer to maintain the minimum possible clock load at the input. P1 and the P4 have high V_{th}, and the channel length of the transistors equals to the minimum channel length allowed by the design/manufacturing rules. Reverse body bias is used to increase the threshold voltage of PMOS transistor P4 of minimum size.

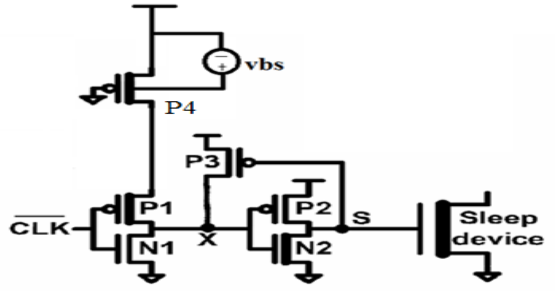


Figure 6: Self sleep buffer using body bias

Alternatively, in the case of a large sleep device, extra stages can be added to the buffer to maintain the minimum possible clock load at the input. P1 and the weak PMOS stack offers high V_{th}, and the channel length of the transistors in the weak PMOS stack equals to the maximum channel length (L_{max}) allowed by the design/manufacturing rules[8]. But the self-sleep circuit with P-stack occupies more area compared body bias technique. With body bias technique comparatively 75% of area is saved for the self sleep circuit. The distributed design more number of blocks, still better savings in the area.

IV. LOW POWER FAST FOURIER TRANSFORM

FFT is a critical block in signal processing applications. Decomposing is an important role in the FFT algorithms. There are two decomposed types of the FFT algorithm. One is decimation-in-time (DIT), and the other is decimation-in-frequency (DIF). The difference between these two types is in the input and output data ordering in signal flow graph (SFG). The DIT algorithm means that the time sequence is decomposed into small subsequence, and the DIF algorithm decomposes the frequency sequence. The Basic concept of 4 point FFT which applies Radix-2 architecture is shown in figure 7.

Figure 8 shows 4 point FFT circuit that can be implemented by using 4 butterfly processing elements as shown. Radix-2_0 is designed with adders and subtractors as shown in figure 9. The functioning of the radix2 is according to the output equations. The outputs are addition and substraction of the input combinations. The equations for the outputs are, O1re=in1re+in2re; O1img=in1img+in2img; O2re=in1re-in2re; O2img=in1img-in2img;

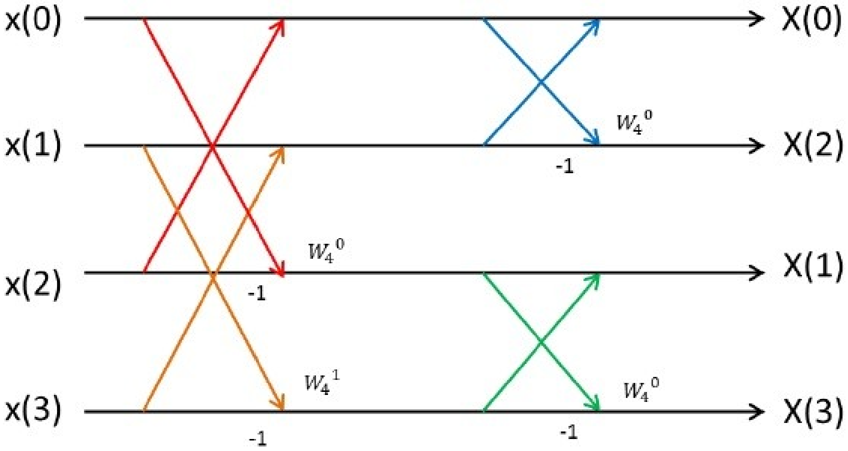


Figure 7: Basic concept of 4-point FFT

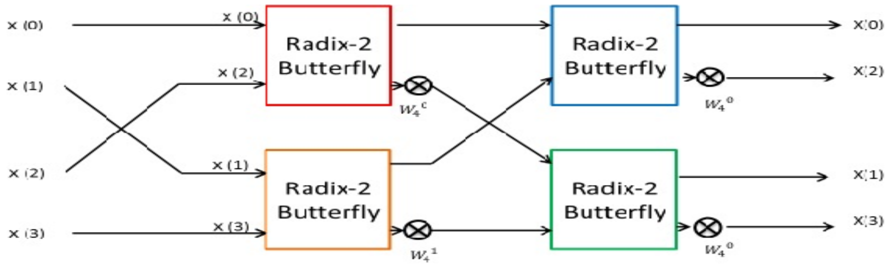


Figure 8: 4 points FFT circuit block diagram

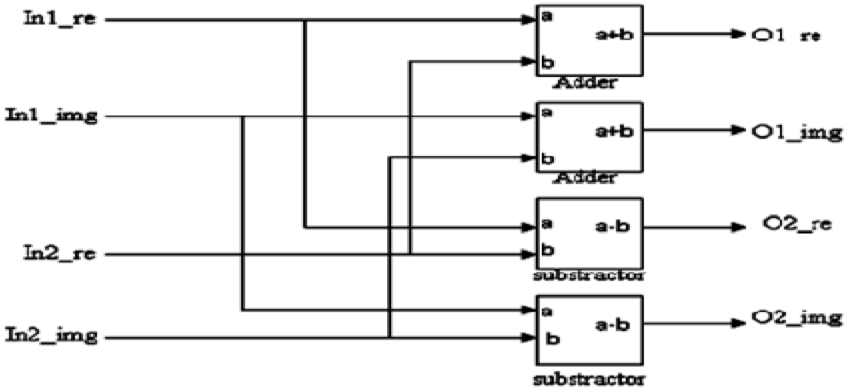


Figure 9: Model of subsystem radix-2_0

MULTIPLIER

This section shows the MULTIPLIER to the MULTIPLIER3 subsystem. The MULTIPLIER subsystem multiplies a twiddle factor. The Complex number operation $a_x + ja_y$ mutiple $b_x + jb_y$ is showed by $a_x b_y - a_y b_y + j(a_x b_y + a_y b_x)$. As following this process, multiple twiddle factors in terms of complex input. Figure 5.11 shows the circuit blocks of the MULTIPLIER subsystem. The MULTIPLIER1 subsystems to the MULTIPLIER3 subsystem are of the same architecture as the MULTIPLIER subsystem against the constant block, the W_real and the W_imag of figure 5.11, parameters. Table 1 shows the Constant block parameters showing the twiddle factors depending on $W_4^0 = 1 + 0j$ or $W_4^1 = 0 - 1j$ in the MULT subsystem, the MULTIPLIER subsystem [9]. The subsystem MULT multiplies the complex twiddle factor in terms of the complex input signals shown in table1. The Block diagram of FFT is shown in figure 10.

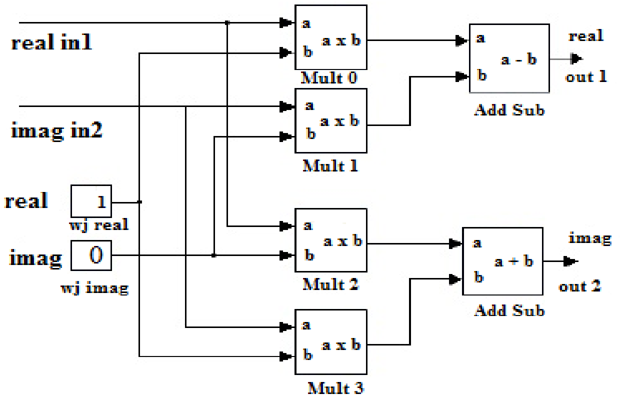
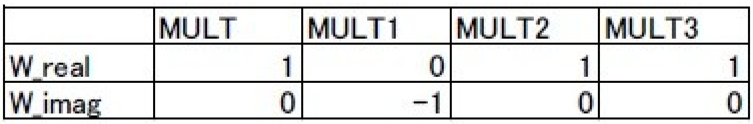


Figure 10: Architecture of the MULTIPLIER subsystem

Table 1: Parameter of the twiddle factor



	MULT	MULT1	MULT2	MULT3
W_real	1	0	1	1
W_imag	0	−1	0	0

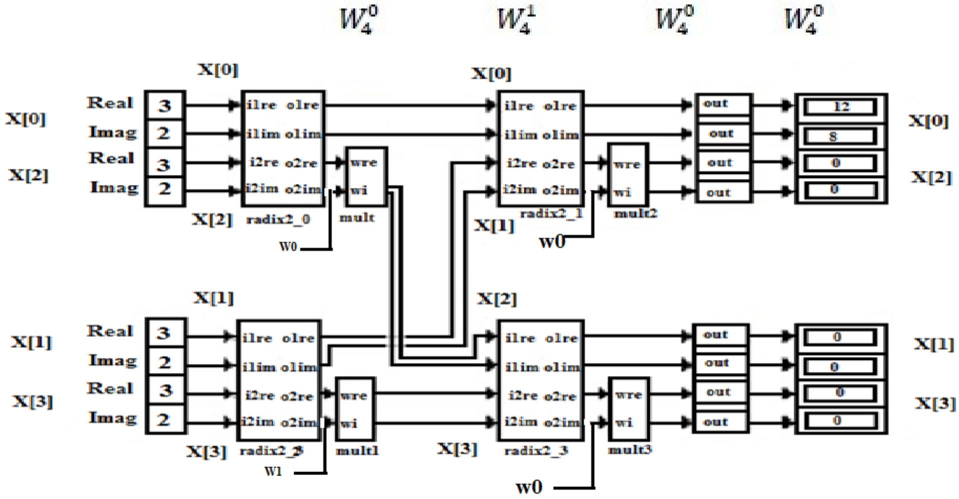


Figure 11: Design of 4 points FFT circuit for parallel input

V. Results

Self sleep buffer circuit with body bias technique consumes 481.7 nW and 25.5 nW of power in active and standby mode respectively. The table2, 3 and 4 shows the power comparisons made, in 90-nm CMOS process with $V_{dd} = 1V$. It is observed that 30 % of power savings are there in active mode for both Radix and multiplier blocks. Power savings are very high in standby mode for both the blocks. In FFT block compared to distributed and with self sleep much more power savings are observed in standby mode.

Table 2: Power comparisons of radix-2 block

Design Module	Radix-2	radix-2 with self sleep buffer using body bias
Active power(uW)	5	3.5
Standby power(uW)	0.70	0.215

Table 3: Power comparisons of Multiplier block

Design Module	Multiplier block	Multiplier with self sleep buffer using body bias
Active power(mW)	1.5	1.047
Standby power(uW)	870	0.862

Table 4 :Power comparisons of FFT block

Design Module	FFT block	FFT with self sleep buffer using body bias
Active power(mW)	5.5	0.00519
Standby power(uW)	400	$1.949\text{x}10^{-6}$

Below is the table giving the delay comparisons calculated in 90nm CMOS technology. From the table 6.8 it is observed that the self sleep buffer with transistor as diode yields less delays. The standby to active delay is less which does not affect the wake period. Self sleep buffer circuit with body bias technique offers 200pS and 300pS standby to active and active to standby mode respectively.

Table 5: Comparison of Delay

Design Module	Self-Sleep Buffer Using Body Bias Standby to Active (ps)	Self-Sleep Buffer Using Body Bias Active to standby (ps)
Radix-2	550	1.2
multiplier	700	1.4
FFT	950	1.8

VI. CONCLUSION

Thus self-sleep buffer with body bias technique has been designed and simulated at schematic level using Cadence tools using 90 nm technologies successfully. The self-sleep buffer eliminates the need for a sleep distribution network, while maintaining good sleep signal integrity in active mode and low energy overhead during active-to-standby-to-active transitions. Active to standby delay is very less that it can be neglected for 2GHz clock frequency. Approximate sleep signal buffer sizing is useful to achieve sleep to active mode transitions with low energy overhead. Compared to other self-sleep technique with p-stack, this circuit occupies comparatively 75% less area. If foundry provides MOS devices of different threshold voltages (only HVT and LVT are available in library) required delay can be maintained for different source currents.

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