

Design and FPGA Implementation of a Low Power Arithmetic Logic Unit

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Abstract : Arithmetic logic unit is the core of any CPU that can be part of a programmable reversible computing device such as a quantum computer. The major concern for ALU design ,using normal gates is heavy power consumption. The main reason for power consumption is the normal irreversible gates. In order to ensure low power design constraint a new type of gates called reversible gates were introduced. In reversible gates the number of inputs is equal to the number of outputs and there is a one to one mapping between the inputs and outputs. Here in this paper we discuss the design of a low power ALU using reversible gates and its implementation on FPGA.

Keywords – ALU, FPGA, Reversible gates, Reversible logic, Spartan.

I. INTRODUCTION

Moore's law provide a platform for the development of integrated circuits and the law will stop it's function sooner. So some dramatic evolution has to happen in microelectronics in near future. Power consumption of CMOS circuits has to become a major problem as the complex digital circuits being built turns to much faster and complex .Landauer [1961] provides proofs for the fact that power loss is an inevitable drawback of irreversible circuits[1] .Bennett[1973] proved that incorporation of reversible gates keeps a circuits from dissipating any power. The major feature of reversible gates is that ,the number of inputs for a reversible is same as the number of outputs. Not only that, there is one to one mapping between the inputs and outputs of a reversible circuit[2].

Arithmetic logic unit is the vital part of CPU since it allows computer to perform arithmetic and logic operations. In simple sense arithmetic logic unit is a combinational logic circuit having one or more inputs and a single output. Which implies that the present value of output depend only on the present input values only. The complexity of Arithmetic logic unit depends on the processor variations. It can be a simple one or complex structure. Thomson[2010] designed an arithmetic logic unit made up of reversible gates for performing modular operations[3].Y Syamala et.al[2011] designed a reversible ALU for performing logic and arithmetic operations Here in this paper we propose a new design of ALU made up of reversible gates with better power saving property.

The rest of the paper is organized as follows: theory of reversible gates and types of reversible gates used in the design in section 2. In section 3 ,proposed ALU design and in section 4 a comparison study with previous ALU design .Section 5 discuss the FPGA implementation and simulation results .Finally section 6 concludes the paper.

II. THEORY OF REVERSIBLE GATES AND TYPES OF REVERSIBLE GATES USED IN THE DESIGN

2.1 Theory of reversible gates

In 1964, "Moore" proposed a law according to that, the number of transistors in an integrated circuit doubles every 18 months. Addition of extra numbers of transistors will not be possible in a few next years and will cause power consumption cost and can be realized as a problem. Whenever we use a logically irreversible

gate it will dissipate energy into the environment. Let us illustrate this with an example as shown in Fig 1.



Figure 1: Irreversible XOR gate

Consider a two input XOR gate with both the inputs zero .Definitely we will get a value `zero' in the output. Here in this process we lost a bit of information .This information loss can be treated as energy loss. One bit of information loss dissipates `kTln2' of energy where `k' is the Boltzmann's constant and `T' is the absolute temperature of the system. So the solution is Reversibility. In reversible computation the power dissipation under idle physical circumstances is zero because reversible computation does not result any kind of information loss . Today reversible computation became an interesting area of research because of reduced heat dissipation there by allowing higher densities and higher speed to circuits. Thus, energy dissipation is proportional to the number of bits lost during computation. The reversible circuits do not lose information and can generate unique output from specified inputs and vice versa (there is a one-to-one mapping between inputs and outputs).This can be illustrated as shown in Fig .2.



Figure 2: Reversible XOR gate

An n-input n-output function F is said to be reversible if there is a one-to-one correspondence between the inputs and the outputs. Therefore, the input vector can be uniquely determined from the output vector. As per Landauer/Bennett[1][2] all the operations required in computation can be performed in reversible manner thus dissipating no heat. A deterministic device is said to be logically reversible if its inputs and outputs are retrievable from each other and physically reversible which implies the device can run backwards. An `m' input `k' output Boolean function $f(x_1, x_2, x_3, x_4, x_5, x_n)$ is called as a reversible function if ,

1. The number of inputs is equal to the number of outputs.
2. Each input pattern maps to a unique output pattern. In reversible logic vector of input states can always be reconstructed from vector of output states since it has a one to one mapping between the vectors of inputs and vector of outputs.

2.2 Types of reversible gates used in the design

Gates which are designed based on the reversible logic are called reversible gates. Reversible are circuits (gates) that have one to one mapping between vectors of inputs and outputs; thus the vector of input states can be always reconstructed from the vector of output states Several reversible gates have been proposed over the years. The main types of gates used for the design of ALU are,

2.2.1 YAG gate

Logical AND and OR functions can be realized using this gate and its quantum cost is 4 as shown in Fig .3[3].

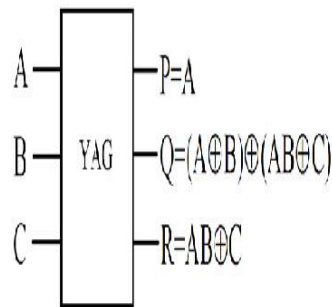


Figure 3:YAG gate

2.2.2 Feynman gate

Feynman gate is a 2*2 one through reversible gate as shown in Fig 4. The input vector is I(A, B) and the output vector is O(P, Q). The outputs are defined by P=A, Q=A xor B. Quantum cost of a Feynman gate is 1[4].

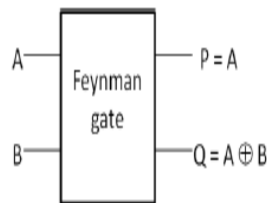


Figure 4:Feynman gate

2.2.3 Fredkin Gate

Fig 5 shows a 3*3 Fredkin gate. The input vector is I (A, B, C) and the output vector is O (P, Q, R). The output is defined by P=A, Q=A’B xor AC and R=A’C xor AB. Quantum cost of a Fredkin gate is 5[5].

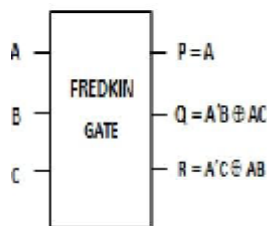


Figure 5:Fredkin gate

2.2.4 DPG gate

Fig 6 shows a Double Peres Gate. The input vector is I (A, B, C, D) and the output vector is O (P, Q, R, S). P=A,Q=A B,R=A B D and S=(A B) D AB C. The full adder using DPG is obtained with C=0 and D= Cin and its quantum cost is equal to 6 [6].

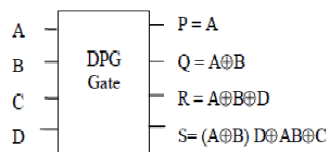


Figure 6:DPG gate

III. Proposed Alu Design

An ALU is the critical core component of a microprocessor .ALU performs the instruction execution functionality. An ALU is a multifunctional unit the conditionally performs one functionality at a time depending on the selection inputs. A one bit ALU that performs four operations is shown in Fig 7.

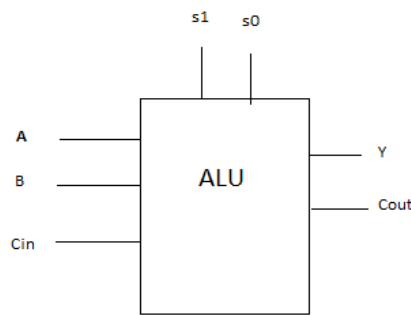


Figure 7: One Bit Conventional ALU

In the actual design of ALU using reversible gates seven basic reversible gates are used. They are (2 Feynman, 3 Fredkin, 1 YAG, 1 DPG). Fig 8 shows the realization of ALU using reversible gates.

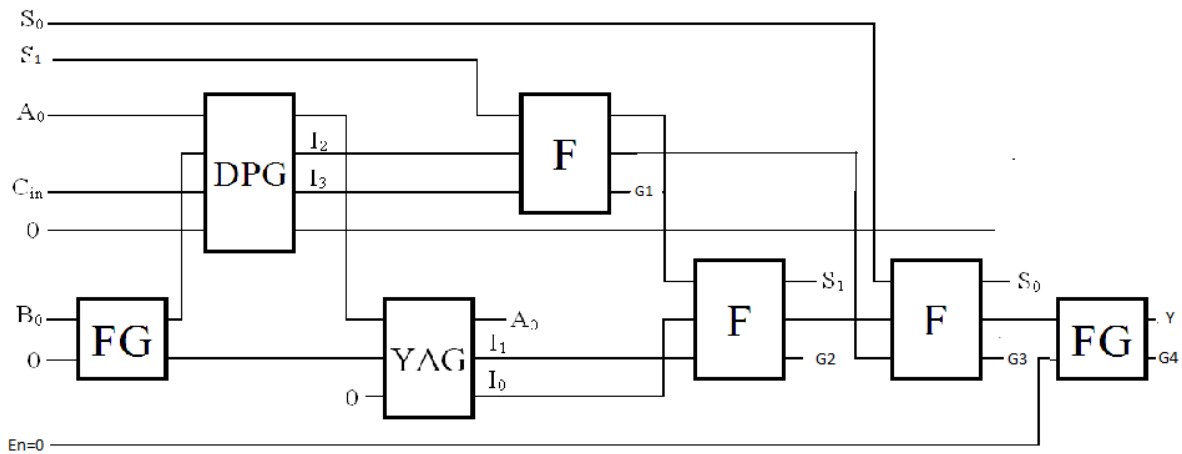


Figure 8: Reversible one bit ALU

The major parameters which determine the quality of a reversible design are number of gates, number of garbage outputs and quantum cost. Garbage output are the outputs which are not used for further calculations. Quantum cost is the number of 1x1 or 2x2 gates that are used in the circuit. For our design these parameters are Seven gates, four garbage outputs and the total quantum cost is 27. The main control bit is enable bit. For the proper operation of the circuit enable bit need to be set as logic zero.

IV. Comparison Study

We propose a new design by comparing it with a design from the design in [3]. The main design parameters that used for comparison study are number of gates, number of garbage outputs, and quantum cost. The comparison study reveals that our design is better than the previous design from [3] in terms of garbage outputs and quantum cost. The comparison study is shown in Table 1

Table 1: Comparison study.

Parameters	Previous design	New proposed design
Gate count	7	7
Garbage outputs	5	4
Quantum cost	30	27

V. Fpga Implementation And Simulation Results

Software tool Model Sim was used for simulation and verification of function of developed design. Simulation is oriented to Spartan 3 AN FPGA chip and hardware prototype of the computer is built-up with use of Xilinx Spartan 3 PCIe Starter board as the hardware platform of the prototype Fig. 9. There is an FPGA chip Xilinx Spartan 3 XC3S1000-4FG676 with 676 pins in FBGA package in the centre of development board and it works on 50 MHz clock frequency.

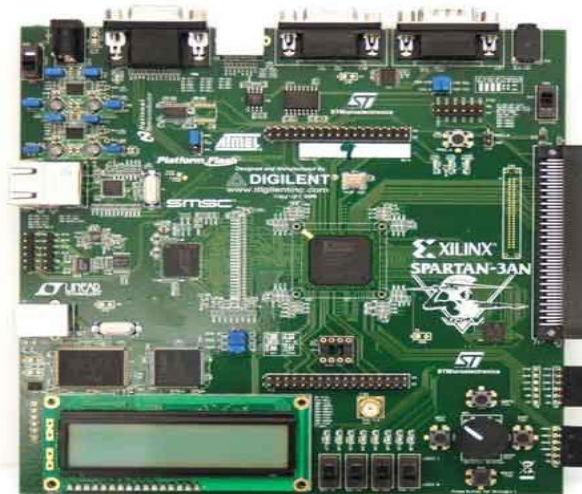


Figure 9: Spartan 3 PCIe Starter Board .

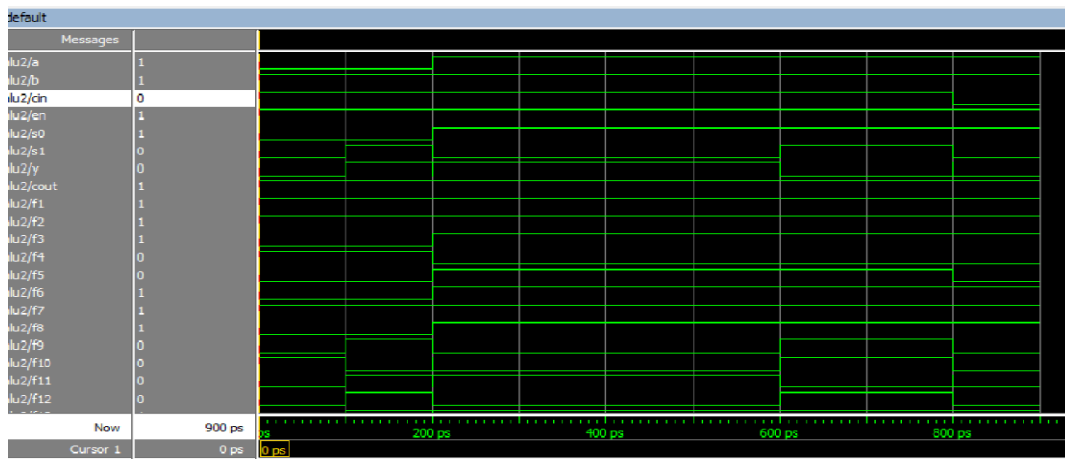


Figure 10:Simulation results of reversible ALU

VI. Conclusion

In this work reversible ALU for a computing device is designed for performing one arithmetic operation and three logic operation. Our design shows better quality in the design parameters like number of gates number of garbage outputs and quantum cost .The proposed ALU is expressed in VHDL hardware description language and in implemented on Spartan 3 FPGA.

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