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A Theoretical Study of Low Power Soi Technology

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***Abstract**: The paper introduces the SOI technology with brief design description and the factors that help in developing low power. The paper also presents the low power generation in partially and fully depleted SOI. And finally gives the superiority factors over bulk CMOS technology. The focus of this article is to present an overview of SOI technology applied to design of a special class of ultra low power devices supervisory circuits. Such circuits are emerging as prime candidates for development using advanced SOI technology processes.*
***Key Words**: Low power, SOI, Delays, Bulk CMOS*

I. Introduction

Rapid growth in technology leads to low power consumption and decrease in the area size with less delays. VLSI is the field of integrating number of transistors on a single chip, as we know that according to MOORE'S law the transistor count is doubled for every eighteen months. Increased demand for high performance, low power and smaller area among microelectronic devices is continuously pushing the fabrication process to go beyond ultra deep sub-micron (UDSM) technologies such as 45nm, 22nm. As the technology is decreasing, many factors affecting the design in which power is main consideration factor, because as the applied voltage is in milli volts if it is so the power consumed should also be in milli watts with less power dissipation and no delays. Considering SOI technology will give much more less power and reduces the leakage currents which are quite in appropriate to that of bulk CMOS technology.

Power is the amount of energy that transfers to load. In CMOSFET power is characterized as static power, dynamic power and short circuit power. In CMOS device static power is said when the transistor is in standby mode that is in ideal condition and anyone of the transistor is in off condition during switching condition, in this condition a small amount of leakage currents is developed across the junctions and which leads to the power dissipation $P_{Static} = I_{Static} V_{DD}$. Dynamic power is said when a capacitance is placed across the load and the capacitance charges and discharges, the capacitor start charging from V_{DD} to load and charged capacitance discharges from load to V_{SS}. One complete charging and discharging cycle, a total charge of Q=CV_{DD} is thus transfers from V_{DD} to GND $P_{Dynamic} = \propto C V_{DD} 2f$. And the total power is $P_{Total} = P_{Static} + P_{Dynamic}$. The short circuit power is obtained when both the transistors of CMOS is partially switched ON.

SOI (silicon on insulator) which means silicon substrate is fabricated on insulator using silicon dioxide, it is fabricated as three layered device such as the bottom most layer is the substrate which is lightly doped. The insulating layer is created by flowing oxygen onto a plain silicon wafer and then heating the wafer to oxidize the silicon, thereby creating a uniform buried layer of silicon dioxide which is called as buried oxide layer (BOX). The insulating layer increases device performance by reducing junction capacitance as the junction is isolated from bulk silicon. The decrease in junction capacitance also reduces overall power consumption. And the top most layer is same as bulk CMOS which help in channel creation. SOI is also a 4 terminal device source, drain, gate and the body; here source and drain terminals are interchange. The width of the silicon film laid over the insulating layer which is used for the formation of silicon device, decides whether the SOI is fully depleted or partially depleted. If the silicon film is thin then the device is said to be fully depleted and if the silicon film width is thick then it is said to be partially depleted. Silicon on Insulator fabrication process helps in achieving greater performance and offers less power consumption as compared to bulk CMOS process.

II. Soi Technology

2.1. Fabrication Process of SOI

Technology is a type of developing and innovating new concepts with which life becomes more Compaq and easier. In past, few decades before bulk CMOS was the leading technology which became a main source for an electronic industries, but due to the following reason which is discussed further SOI become superiority technology over BULK technology. SOI overcome the disadvantages of BULK CMOS technology. Therefore SOI technology will lead the present and future electronic boom. The active elements (e.g., transistors in a CMOS IC) of semiconductor devices are fabricated in the single-crystal silicon surface layer over the BOX. [2,1] The BOX layer provides robust vertical isolation from the substrate. Standard LOCOS (Local Oxidation of

Silicon) or STI (Shallow Trench Isolation) processes are employed to provide lateral isolation from adjacent devices. [3,4,5]Most of the early SOI devices were fabricated with SOS (Silicon-On-Sapphire) wafers.
The unique feature of today's SOI wafers is that they have a buried silicon oxide (Buried Oxide, or BOX) layer extending across the entire wafer, just below a surface layer of device-quality single crystal silicon. At the present time, most SOI wafers are fabricated by use of one of two basic approaches. SOI wafers may be fabricated with the SIMOXTM ([6,7] separation by Implanted Oxygen) process, which employs high dose ion implantation of oxygen and high temperature annealing to form the BOX layer in a bulk wafer.

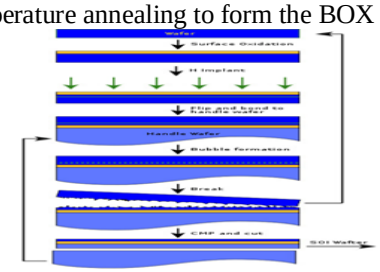

Figure 1. Fabrication process of SOI technology

Alternately, SOI wafers can be fabricated by bonding a device quality silicon wafer to another silicon wafer (the "handle" wafer) that has an oxide layer on its surface. [9,8] the pair is then split apart, using a process that leaves a thin (relative to the thickness of the starting wafer), device-quality layer of single crystal silicon on top of the oxide layer (which has now become the BOX) on the handle wafer. This [10,11,12] is called the "layer transfer" technique, because it transfers a thin layer of device-quality silicon onto an oxide layer that was thermally grown on a handle wafer. The "layer transfer" approach has lead to the development of at least three production methods for fabrication of SOI wafers; Smart cut TM (UNIBOND) SOI wafers, Nanocleave TM SOI wafers, and ELTRANTM

SOI wafers. The SmartcutTM and NanocleaveTM processes both employ high dose ion implantation (using hydrogen or other light species), either alone or in combination with other steps, to form a weakened silicon layer that splits (i.e., "peels off") the donor wafer, allowing the "layer transfer" to occur.
The ELTRANTM method (Epitaxial Layer Transfer) does not use ion implantation. It employs a layer of porous silicon, which is formed by anodic etching and annealing, to form the splitting layer. Recently, there is strong interest in SOI wafers for application to the fabrication of advanced CMOS ICs. [13]This is because SOI wafers provide a way to increase the speed performance of CMOS circuits, as well as reduce the power (and voltage) requirements to achieve high performance. The trade-off between performance and power dissipation is the most fundamentally challenging issue on the horizon for scaling of CMOS ICs.

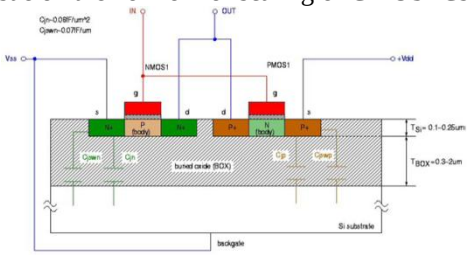

Figure 2. Cross-section of a thin-film SOI CMOS inverter

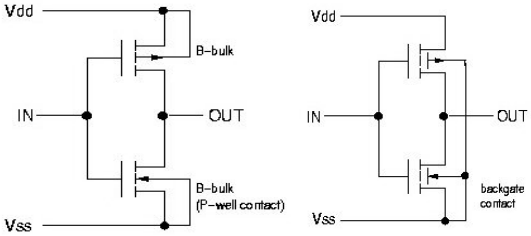

Figure 3. Electrical scheme of bulk (a) and CMOS (b) SOI inverter.

The figure 3b shows the CMOS SOI inverter, the working is same as that of bulk CMOS

2.2. Partially Depleted SOI

On the other hand, if the insulated layer of silicon is made thicker, the inversion region does not extend the full depth of the body. A technology designed to operate this way is called a "partially depleted" SOI technology. The undepleted portion of the body is not connected to anything. The exact voltage depends on the history of source, gate, and drain voltages leading up to the current time (the "history effect"). However, the voltage can be expected to fall within a known range. [14]. the body voltage affects the conduction of the channel and therefore the switching speed and parasitic capacitance of the circuit. In an NMOS transistor, a

lower initial body voltage results in a thinner inversion layer, lower conductivity, and slower switching. Conversely, a higher initial body voltage results in faster switching. In a PMOS transistor, the opposite is true; a lower initial body voltage results in faster switching. Fig 4a Charging of the transistor body (floating body) leads to a change in the threshold voltage, if this is properly taken into account in the IC conception then the result is a faster switching, thus higher performance at same V_{DD}.

2.3. Fully depleted SOI

Fig 4b shows an NMOS transistor, applying a positive voltage to the gate depletes the body of P-type carriers and induces an N-type inversion channel on the surface of the body [14]. If the insulated layer of silicon is made very thin, the layer fills the full depth of the body. A technology designed to operate this way is called a "fully depleted" SOI technology. The thin body avoids a floating voltage. In 45nm and below CMOS, the V_t can be tuned by a midgap metal gate leaving the fully-depleted body undoped. Higher channel mobility and hence higher performance are achieved, as well as lower variability from one device to another. Fully Depleted SOI enables a CMOS LP technology with un-doped body. It gives the best performance - low leakage couple, a perfect choice for Low Power Applications.

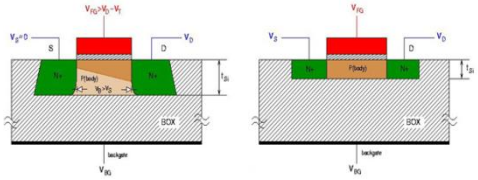

Figure 4. a) Partially depleted (thick film) SOI MOSFET with kink effect; b) fully depleted (Thin film) device.

Before showing the power analysis of SOI the SOI CMOS works in three operating regions cutoff, linear and saturation region. If the gate source voltage V_{gs} is less than threshold voltageV_t then the region is operated under subthreshold which is known as subthreshold region.

Table 3 Relations between voltages for the three regions of operation of CMOS inverter

	Cut-off	Non-saturated	Saturated
P-device	$V_{gsp}>V_{tp}$ $V_{in}>V_{tp}+V_{dd}$	$V_{gsp}<V_{tp}$ $V_{in}<V_{tp}+V_{dd}$ $V_{dsp}>V_{gsp}-V_{tp}$ $V_{out}>V_{in}-V_{tp}$	$V_{gsp}<V_{tp}$ $V_{in}<V_{tp}+V_{dd}$ $V_{dsp}<V_{gsp}-V_{tp}$ $V_{out}<V_{in}-V_{tp}$
N-device	$V_{gsn}<V_{tn}$ $V_{in}<V_{tn}$	$V_{gsn}>V_{tn}$ $V_{in}>V_{tn}+V_{dd}$ $V_{dsn}<V_{gsn}-V_{tn}$ $V_{out}<V_{in}-V_{tn}$	$V_{gsn}>V_{tn}$ $V_{in}>V_{tn}+V_{dd}$ $V_{dsn}>V_{gsn}-V_{tn}$ $V_{out}>V_{in}-V_{tn}$

III. Low Power In Soi Technology

In general when bulk CMOS circuit is replaced by a compatible SOI circuit, its speed performance can be improved 25%at reduced power dissipation. Along with the down scale of power supply voltage, both bulk and SOI CMOS technologies are targeted for low power consumption. Fig 5 shows the power consumption verses the power supply voltage of CMOS logic gate using bulk and SOI CMOS devices. The power consumption of CMOS logic is composed of static and dynamic portions. The static power consumption is referred as power consumption during standby, which is caused by leakage currents. The dynamic power consumption is related to power consumed during switching, which is a function of clock frequency, the load capacitance, and the supply voltage. Owing to buried oxide isolation, the source/drain capacitance of SOI device are 20% smaller as compared to bulk. Therefore, the dynamic power consumption is of SOI circuit is smaller. Along with shrinking of the power supply voltage is scaled down. Since the SOI devices have better subthreshold characteristics, their leakage currents are also smaller as compared to bulk.[15,16] Thus the static power consumption of SOI circuit is smaller than bulk counterpart.

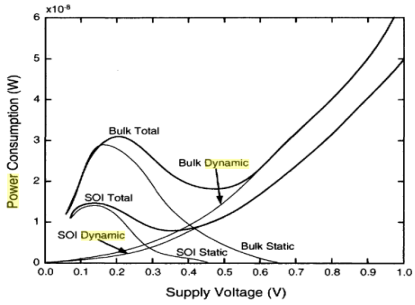

Figure.5. POWER consumption vs power supply voltage CMOS logic gate using bulk and SOI CMOS device

From the above reasoning, the total power consumption is smaller for SOI technology.

$P_{total} = P_{static} + P_{dyn} = I_{off} V_{DD} + \propto f C_L V_{DD}^2$ (2)

Where VDD is the supply voltage, f is the input frequency; CL is the load capacitance and $\propto$ is the degree of the activity of the gate. An activity of 1 % is assumed here, and both SOI and bulk device operate at the same frequency. The algorithm used for calculating the power consumption is the current I_{ON} required to discharge the load capacitor with time constant of 100psecis estimated. This current obtained from a gate voltage equal to V_{DD}, I_{OFF} be obtained. The threshold voltage need to active constant switching speed under varying V_{DD} condition can be extracted from the equation 2 above

3.1. Static Power Dissipation

Figure 3 shows the schematic of an inverter circuit consisting of P-channel and N-channel SOI DTMOS. The parasitic lateral bipolar inherent in the DTMOS will not turn on in the inverter circuit as it is not biased in the forward active mode, so in the following analysis only the two back-to-back parasitic diodes behavior of DTMOS is considered. When the input logic is low, both of the PMOS parasitic diodes D_p1 and D_p2 are forward biased by V_{dd}. As a result, there are two DC current paths as shown in Figure 3, one from V_{dd} through D_p1 to V_{in} (solid line), and the other from V_{dd} through PMOS channel and Dp2 to V_{in} (dotted line). Similarly, when the input is high, two current paths through NMOS parasitic diodes exist. Hence, the static power dissipation increases, compared with an inverter with conventional floating-body SOI CMOS, where the static power is mainly due to a small subthreshold leakage current of the device. The enhancement in the static power dissipation limits the range of the power supply of DTMOS circuit. Normally it should be kept below 0.7V to avoid large static body current.[17,18]

The static power dissipation is the sum of the power due to subthreshold leakage and that due to the forward biased parasitic diodes. Since there are two conductive parasitic diodes during each half-cycle as mentioned above, the average input cycle can be modeled as

$Pstatic = V_{dd} I_{SUb} + \left[V_{dd} (I_{SN} + I_{SP}) \left(e^{V_{dd}/V_T} - 1\right)\right]$ (1)

$$\left[V_{dd} (I_{SN} + I_{SP}) \left(e^{V_{dd}/V_T}\right)\right]$$

Where I_{SN} and I_{SP} are the reverse saturation currents of the parasitic diodes associated with NMOS and PMOS respectively.

3.2. Dynamic Threshold MOS Transistor

Fig. 5 shows the operation of the device in the standard MOSFET mode, or in DTMOS mode: the body is either floated or grounded in the MOSFET mode. Besides the four-terminal test device, DTMOS devices with hard local gate to- body connections are also fabricated [18]. This connection uses an oversized metal-to- P contact window aligned over a "hole" in the poly gate. The metal shorts the gate and the P region (for N-DTMOS). This contact requires minimal area and no additional processing steps.

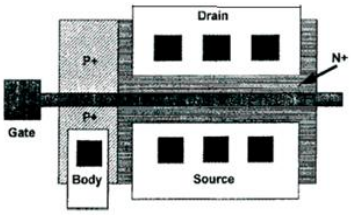

Figure.6. Schematic of Body Contact SOI NMOS Device

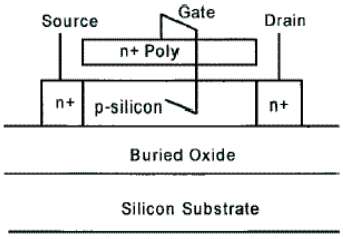

Figure.7. NMOSSOI with body and gate tied

The gate is tied to the body in the DTMOS mode, shown in Fig. 6. Besides the four-terminal test device,

DTMOS devices with hard local gate-to-body connections are also fabricated. This connection uses an oversized metal-to- P contact window aligned over a "hole" in the poly gate. The metal shorts the gate and the P region (for NDTMOS). This contact requires minimal area and no additional processing steps.

3.3. Power Dissipation during Switching

The power dissipation of DTMOS inverter circuit during switching consists of three components: charging and discharging power due to the load capacitance, short circuit power, and the parasitic diodes switching power

The first component, $C_L V_{dd}2/Tp$, is identical for both conventional CMOS and DTMOS circuits. The short circuit power dissipation will not be discussed in this work as it is normally overwhelmed by the first component. The power due to parasitic diodes, however, is in addition to the total dynamic power dissipation in the conventional CMOS circuit. This extra amount, which is of interest to this paper, stems from the transient behavior of parasitic diodes in DTMOS.[18]

Given a negative step input with fall time *Tf* (see

Figure 8), the body potential follows the gate input so that diode D_p1 and D_p2 are gradually turned on while diode D_n1 and D_n2 are gradually turned off. Similar diodes turning on/off behavior takes place for a positive step input. All these behaviors during the switching lead to an additional power dissipation in DTMOS inverter. The transient body current, which is essentially the sum of the back-to-back parasitic diodes current, is much larger than its steady-state value.

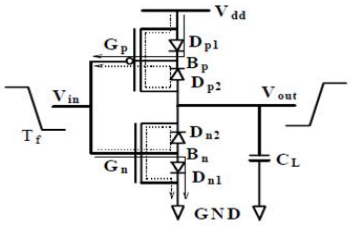

Figure.8. Inverter circuit CMOS SOI

IV. Calculation Of Delay And Power Consumption

Calculation of Delay: The propagation delay time τ_{phl} and τ_{plh} determine the input to output signal delay during V50% high to low and low to high transition of the output respectively. For full adder a pulse of rise time 10ps and 'on time' 100ps is set as a one input.[18]

The total delay is calculated as :

$\tau_P = (\tau_{Phl} + \tau_{Plh})/2$ (3)

3.3a. Calculation of Static Power Dissipation: It means to find power dissipation in standby mode. All the inputs are set to either '0' or '1' then corresponding Id is calculated. Static power is the multiplication of supplied voltage with current drawn from the biasing voltage.[21]

$P_{Static} = V_{dd} I_d$ (4)

3.3b. Calculation of dynamic power dissipation: A "Power Meter Method" is used for calculating the dynamic power dissipation. The average power dissipation (P_{avg}) of any circuit, which is driven by a periodic input waveform, can be found by integrating the product of its instantaneous voltage and its instantaneous terminal current over one period.

$V_y(T) = V_{dd} \, {}^1\!/_T \int_0^T i_{dd}(\tau) d\tau$ (5)

The equation (5) corresponds to the average power drawn from the power supply source over one period. Thus the value of node voltage V_y at t =T gives the dynamic power dissipation for one time period. The model also accounts for the parasitic capacitances associated with contacts

V. Advantages, Disadvantages And Factors That Effecting Low Power In Soi Technology

5.1. Hysteresis and Latch Effects

Hysteresis and latch effects in SOI MOSFET are observable while operating at the border between the weak and strong inversion region. It can be shown that for large V_{DS} voltage values observable hysteresis in gate characteristics occur. Moreover, in some rare cases, hysteresis is also supported by the memory effect. It means that the transistor does not turn off when the gate voltage goes to zero. This effect is related to the parasitic bipolar structure in SOI and can be avoided with some advanced technology procedures. [19]

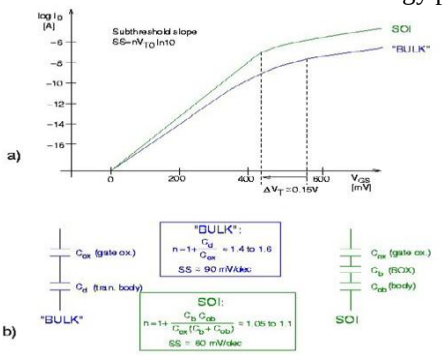

Figure.8. Comparison of SS and V_T for "bulk" and SOI: a) sub-threshold gate characteristics; b) corresponding equations

5.2 SOI Floating Body

In a standard Bulk CMOS process technology, the P-type body of the NMOS Transistor is held at the ground voltage, while in the Bulk CMOS process technology, a PMOS Transistor is fabricated in an N-well, with the transistor body held at the V_{DD} supply voltage by means of a metal contact to the N-well. [14]

In Silicon-On-Insulator process technology, the source, body and drain regions of transistors are insulated from the substrate. The body of each transistor is typically left unconnected and that results in a floating body. The floating body can get freely charged/discharged due to the transients (Switching) and this condition affects threshold voltage (V_t) and many other device characteristics.

The transistor area in SOI process is less because there is no need for metal contacts to Wells that are used for making MOS transistors.

5.3 Latchup Elimination

Bulk CMOS relies on junction isolation between devices, while SOI uses dielectric isolation to surround the entire device sides and bottom. SOI has no wells into the substrate and therefore has no Latchup or leakage paths. It eliminates the need for guard rings, thus smaller area for same function.[14]

5.4 Kink Effect

Kink effect belongs to the so-called floating body effects. Except for some special cases3, there is no equivalent effect in bulk because of connected transistor body either to the substrate or a well.[19]

Consider the thick film PD SOI MOSFET depicted in Figure 9. From the impact ionization caused by high electric field near the drain region, a part of the majority carriers (holes) can migrate to the transistor body. This is due to the potential of V_B being, originally, very close to V_S, which corresponds to zero.

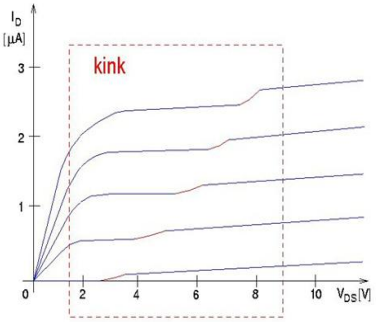

Figure.9. Kink Effect

Nevertheless the whole migration results in a local increase of the body potential V_B. In the case where the voltage drop across the body-source diode is high enough, the junction may be turned on, giving rise to a decrease of the transistor threshold voltage. However, it results in a current drop called "kink" in the drain device characteristics (Figure 9). The mechanism described above is the so-called "first kink" in a SOI device. This can be a serious disadvantage in precision analog design as well as in low power digital design.
In practice, there are several ways to avoid the kink effect in PD SOI. The most common one is to create the so-called body contact. Fortunately, it can be shown that FD SOI devices do not suffer from the kink effect, which is a primary advantage of the fully depleted SOI processes.

5.5 History Effect

The body of the NMOS or PMOS Transistors in the SOI is floating instead of tie to Ground (NMOS) or V_{DD} (PMOS) as in bulk CMOS. This floating body can change the MOS Transistor Threshold voltage due to differences in the Body voltages [14]. This could cause variation in the circuit delay and mismatch between two identical devices. As the SOI circuit switches, the Body Voltages of the switching transistors will change from their previous steady state condition. This is called the History Effect. A SOI logic circuit can have different (shorter) delay if switching regularly verses a circuit that has been inactive for a long time and then switches. If a circuit is not active for long enough time to be in a steady state and then switches, this switching activity is called ***first switch***. If the circuit is switching more regularly, this is called ***second switch***. Typically, second switch has shorter delay than first switch due to the body to source voltage of the second switch is higher than first switch, which lowers the V_t of the second switch transistor. This is one of the most interesting circuit design issues in SOI but it is also a benefit of SOI which contributes to SOI performance advantage over bulk CMOS. Modeling Timing Parameters of the Transistor and Circuit considering the History Effect is critical for successful for Silicon Success.

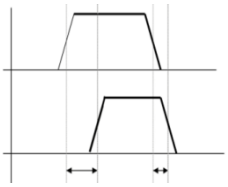

Figure.10. History effect

5.6 Bi-polar currents

There is a low gain parasitic bipolar transistor on every floating body SOI FET transistors. This bipolar transistor is in parallel with the FET transistor and could cause false switching to the off FET transistor. In general pass gate circuit has the highest bipolar current effect.

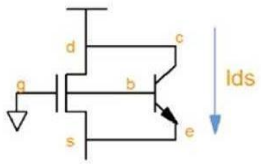

Figure.11. Bipolar Drain Current

When both Source and Drain of Transistor are at High and Gate is at Low (in the case of a Pass Gate), the floating body will couple to high. When Source or Drain goes to Low then we will see a current pulse even when the gate is low. However over the years of the technology scaling, this bipolar current effect has been pretty much eliminated due to the reduction of the operating voltage of the 90nm node and beyond. In some extreme case, where the design has many transistors connected in parallel, the designer needs to verify the bipolar current to ensure the functionality of the circuit. This is particularly important if the design requires functional burn-in at a much higher voltage than the typical operating voltage condition.[14]

5.7 Self-Heating

The insulation layer of the SOI wafer creates a potential temperature delta between devices called local (self) heating. Self-heating is evident at the high power regions. May not have huge impact on Digital circuits; however this effect must be considered for analog type of circuits. [14]

5.8 Temperature Sensitivity

SOI CMOS is much less sensitive to temperature than bulk. In all SOI processes, the leakage to the substrate is obviously suppressed. Furthermore in FD SOI, the V_t varies by about 2x less with temperature than in bulk.[14]

5.9 Body Contacts

In the digital circuits, the transistor operates as a switch and remains in a steady state most of the times. Modeling switching characteristics with Floating Body effects are slightly complicated, but it can be modeled. Where as in the Analog/Mixed/IO design modeling the behavior of linear characteristics circuit is very difficult with varying potential of the Floating Body as it changes the output impedance of the device and it's V_t-matching to the next device. A Body Contact Transistor can be used as the current source or as any matching transistors designs to eliminate the floating body effect in the SOI technology. However Body Contact has RC delay associated with it, and shows poor transient response due to high capacitance and resistance. Also Body Contacts do not scale with the Gate Length, and requires bigger Transistor size and Low density. Body contacts are used only where needed because they increase the layout area and decrease performance.[14]

VI. Conclusion

Finally the paper concludes by presenting brief description of SOI technology with leading factors, factors that effecting in obtaining low power with delay descriptions and shows the superiority issues of SOI over bulk technology. After studying about both the technologies SOI will lead with the future technologies and become the targeting factor for low power industries.

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