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Design of Low Power Quaternary Adders in Voltage Mode Multi-Valued Logic

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Abstract: *This paper presents design of quaternary half adder and full adder based on multi valued logic.Adders are one of the important part of the processing element and hence it has a focus of research.Therefore implementation of adders using multi valued logic can prove to be very useful.The proposed half adder and full adders are designed with the help of transmission gate. These half adder and full adder are verified by simulation and appear to have very low power dissipation.*
Keywords -*Multi-Valued Logic, Quaternary Logic,Adders*

I. Introduction

Multi-valued logic is very beautifully defined by "EleanDubrova"aslike painting a picture having all possible colors available[1].Multi-value logic is defined as a non-binary logic and involves the switching between more than two states. Multi-valued logic means instead of assuming one of the two states as per in binary logic , signal may assume one of more than two states , for instant 4 states. Binary values take only values {0,1}.Multi-valued synthesis take multivalued variables Xi can take values Pi={0,…pi-1}.Multi-valued logic offers important advantage like more information can be processed over a given set of lines to reduce the burden of interconnections and thereby switching[2].

The advantage of Multi-valued logic are the use of fewer operations potentially fewer gates and reduction in number of interconnections and switching. The reduction of dynamic power dissipation is VLSI applications is the major challenge for today's engineersas major portion of the power is consumed by interconnect and switching[3].

Adders form the basic part of processing element. Adders is basically a circuit which is used in variety of applications. So, if we create an optimized adder simultaneously the processing elements will be improved. This will fasten the calculation of arithmetic Logic Unit which further improves and fasten the performance of the unit. Using an optimized adder using Multi-Valued logic will lessen the space required. Optimized adders will prove to be useful in other Digital Signal Processing as adders are the basic part of Digital Signal Processing.

Basic feature of multi-valued logic over binary logic is multivalued logic requires fewer interconnections, more information can be processed over a given sets of lines, area is reduced, gives faster results, low power dissipation and low cross talk noise.

II. Design Techniques

Severaldesigning methods have been proposed in the recent papers to realize the Multi-valued logic circuits.[4,5].They can be fundamentally categorized as current –Mode, voltage mode and mixed mode circuits. Several prototype chips ofcurrent-mode CMOS circuits have been fabricated, showing somewhat better performances compared to the corresponding binary circuit[6-9]. Even thoughcurrent-mode circuits have been popular and offer severalCMOS binary logic circuits from the perspective of dynamic switching activity. Voltage-mode circuits consume a large majority of power only during the logic level switching.Hence, voltage-mode circuits do offer lesser power consumption which has been the key benefit of traditional CMOS binary logic circuits from the perspective of dynamic switching activity. [7-12] Quaternary logic (radix-4-valued) is chosen as the base radix. Using a quaternary radix offers all the benefits of MVL with the important advantage of being able to easily interface with traditional binary logic circuits.

III. Design Of quaternary Adder

There are many ways in which quaternary adders using multivalued logic can be design.Ricardo has designed quaternary MUX as the basic building block for design of adders[17].Quaternary adders are also designed by usingconverters from quaternary to binary and binary to quaternary converters with computation done in binary[22].

The proposed quaternary half adder andquaternary full adder is design using CMOS transmission gate or pass transistor as a basic building block. The pass transistor is a simple switch circuit. It consist of one P-MOS and one N-MOS connected in parallel.

The CMOS implementation of transmission gate is shown in Fig.1. The N-MOS switch is open if control signal of the N-MOS switch is 0 and is closed if control signal of the N-MOS switch is 1 shown in Fig.1 (a).Similarly for P-MOS switch of is open if control signal of the P-MOS is 1 and is closed if control signal of P-MOS is 0 shown in Fig.1 (b). From Fig.1 (c) and 1(d), input of the N-MOS switch is denoted as C and C for P-MOS switch. The input to both is available through the binary inverter. If the input of the inverter logic 1 and inverted output C is 0.C and C given to N-MOS and P-MOS switch respectively which is shown in Fig.1 (c). If the input of the inverter C is 0 and inverted output c is 1.C and C given to N-MOS and P-MOS switch respectively which is shown in Fig.1 (d).

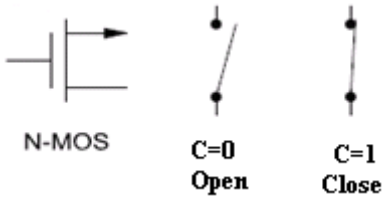

Fig..1 a

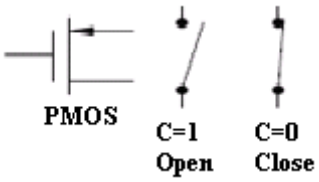

Fig..1 b

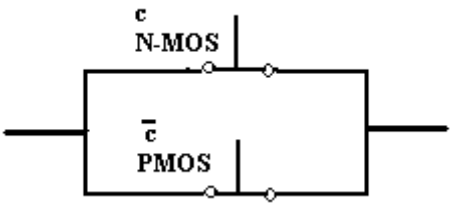

Fig..1 c

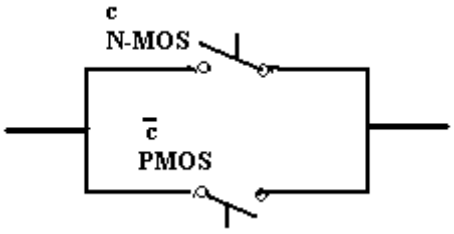

Fig..1 d

III. A.Design Of Proposed Half Adder

The proposed quaternary half adder is designed using CMOS transmission gate as the basic building block. For design of half adder the combination of the quaternary input voltages taken are (0V,1V,2V,3V). The maximum voltage applied is 3V with operating frequency 50MHz.

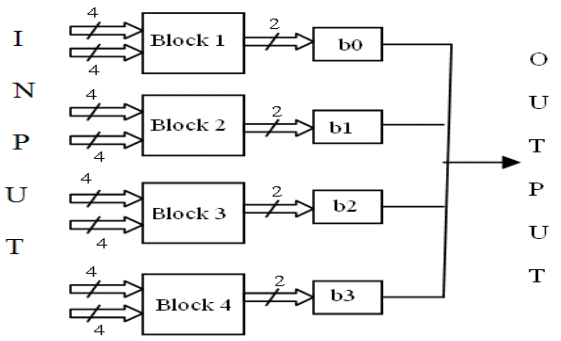

Fig. 2 a.Proposed Quaternary half adder Sum Block

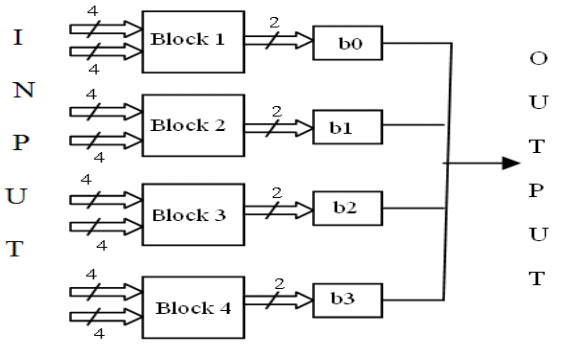

Fig.2.b.Proposed Quaternary half adder Carry Block.

The Fig 2.a. and Fig. 2.b. shows the block diagram of quaternary half adder sum and carry block respectively. Each block consists of combination of CMOS transmission gates. Block 1to 4 has total eight inputs applied out of which four input are the combination of quaternary input signal applied i.e(0,1,2,3)V and other four input are the combination of the enabled signal which is applied to enable the CMOS transmission gate.The behavior of quaternary half adder can be explained with help of truth table.

TABLE 1

TRUTH TABLE OF QUATERNARY HALF ADDER

Input		Output	
X	**Y**	**Sum**	**Carry**
0	0	0	0
0	1	1	0
0	2	2	0
0	3	3	0
1	0	1	0
1	1	2	0
1	2	3	0
1	3	0	1
2	0	2	0
2	1	3	0
2	2	0	1
2	3	1	1
3	0	3	0
3	1	0	1
3	2	1	1
3	3	2	1

As shown in the table 1 Input X and Input Y are the quaternary inputs and we obtained the Output in the form of Sum and Carry.From the truth table we can generate the quaternary inputs X and Y.The input X which is the quaternary input is generated usingX= PWL(time 0s 0v 19.9ns 0v 20ns 1v 39.9ns 1v 40ns 0v 59.9ns 0v 60ns 1v 79.9ns 1v 80ns 0v);

The quaternary input Y =PWL(time 0s 0v 4.9ns 0v 5ns 1v 9.9ns 1v 10ns 0v 14.9ns 0v 15ns 1v 19.9ns 1v 20ns 0v 24.9ns 0v 25ns 1v 29.9ns 1v 30ns 0v 34.9ns 0v 35ns 1v 39.9ns 1v 40ns 0v 44.9ns 0v 45ns 1v 49.9ns 1v 50ns 0v 54.9ns 0v 55ns 1v 59.9ns 1v 60ns 0v 64.9ns 0v 65ns 1v 69.9ns 1v 70ns 0v 74.9ns 0v 75ns 1v 79.9ns

1v 80ns 0v). As per voltage level the corresponding input select , is shown in simulation resultFig. 4.a and 4.b This new proposed design of half adder has very low total power dissipation measured by Spice element printpower.

III.B. Design Of Quaternaryfull Adder

The proposed quaternary full adder is constructed using quaternary half adder.The block diagram of quaternary full adder is shown in the Fig.3

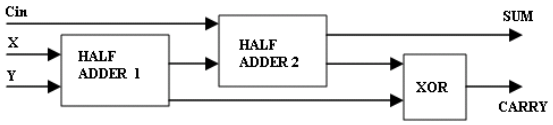

Fig. 3 Proposed Quaternary Full Adder

The Full adder is constructed by using two half adders and one XOR gate. The first quaternary half adder is given with the two quaternary inputs X and Y. The second quaternary half adder is given one input Cin and the other input is the output of the first full adder. The other output of the first full adder is given as input to XOR gate. The other input of the XOR gate is the output of the second full adder. The sum and the carry outputs of the quaternary adder is taken fromOutput of second full adder and output of XOR gate respectively.
The behavior of Quaternary full adder can be explained with the help of truth table shown in Table2 and Table 3 which is constructed for Cin =0 and Cin =1 respectively.

TABLE 2
TRUTH TABLE OF QUATERNARY FULL ADDER with Carry =0

Cin	X	Y	S	Carry
0	0	0	0	0
0	0	1	1	0
0	0	2	2	0
0	0	3	3	0
0	1	0	1	0
0	1	1	2	0
0	1	2	3	0
0	1	3	0	1
0	2	0	2	0
0	2	1	3	0
0	2	2	0	1
0	2	3	1	1
0	3	0	3	0
0	3	1	0	1
0	3	2	1	1
0	3	3	2	1

TABLE 3
TRUTH TABLE OF QUATERNARY FULL ADDER with Carry =1

Cin	X	Y	S	Carry
1	0	0	1	0
1	0	1	2	0
1	0	2	3	0
1	0	3	0	1
1	1	0	2	0
1	1	1	3	0
1	1	2	0	1
1	1	3	1	1
1	2	0	3	0
1	2	1	0	1
1	2	2	1	1
1	2	3	2	1
1	3	0	0	1
1	3	1	1	1
1	3	2	2	1
1	3	3	3	1

As shown in the Table 2 and Table 3 Input X and Input Y are the quaternary inputs and we obtained the Output in the form of Sum and Carry with Cin =0 or Cin=1. This new proposed designof half adder has very low total power dissipation measured by Spice element printpower.

IV. Simulation Results

The simulation results is shown in the Fig. 4.a which verifies the Table 1. In the simulation result the quaternary inputs corresponds to 0v,1v,2v and 3v respectively. As we see from the simulation results when the input for example is x=2 and y=2 observed output is Sum=0 and carry =1 which verifies the truth table.The simulation results for the quaternary full adder with carry = 0 is shown in the Fig. 4.b which verifies the Table 2. In the simulation result the quaternary inputs corresponds to 0v,1v,2v and 3v respectively. As we see from the simulation results when the input for example is x=3 and y=3 observed output is Sum=2 and carry =1 which verifies the truth table.

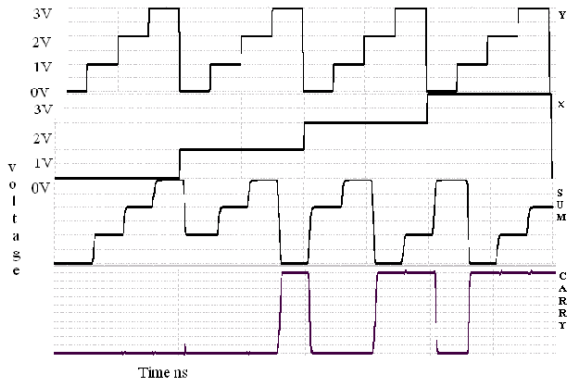

Fig. 4.a Simulation result of quaternary Half Adder

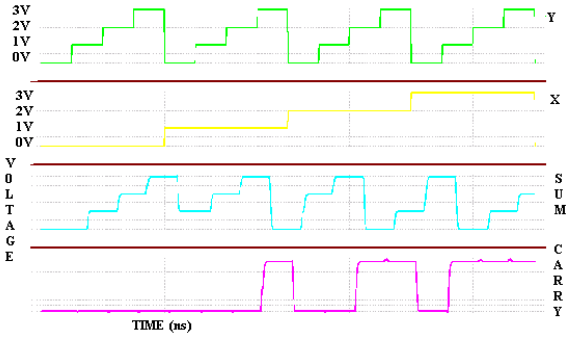

Fig. 4.b Simulation result of quaternary full Adder with Carry =0

Transient Analysis gives the maximum average power consumed by half adder and full adder.

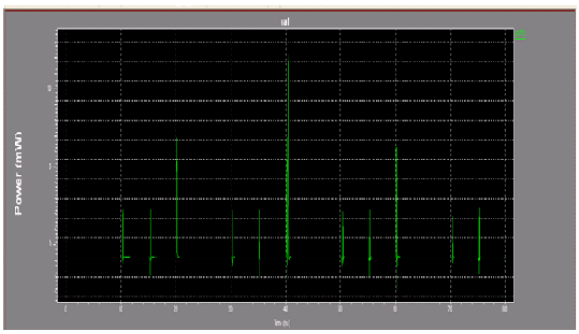

Fig. 5. Power consumed by half adder

Fig. 5.shows the maximum power required by half adder using T gate.The power consumed by T gate is 0.023microWatt.

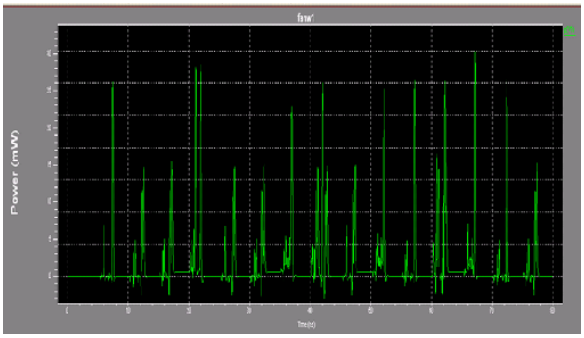

Fig. 6. Power consumed by half adder

Fig. 6.shows the maximum power required by half adder using T gate. The power consumed by CMOS transmission gate is 0.832microWatt.

V. Conclusion

We have proposed quaternary multi valued logic half adder using CMOS transmission gate.Using this quaternary half adder we have constructed quaternary full adder.The quaternary system is capable of transmitting more information than the binary systems.Low power dissipation is the major advantage offered by the proposed adder.The simulation results are verified at frequency upto50Mhz, input supply voltage of maximum 3 Volts. The average power dissipation obtained is 0.023 micro watt for half adder and 0.832 micro watt for full adder. These circuits hasbeen verified for high frequency with low voltage.As adders form the basic computing element , design of quaternary adders using multi valued logic has several advantages in the particular area like communication ,memory and digital signal processing.

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