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Digital Clock Synchronization with Cyclic Rotation Algorithm

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Abstract: *This paper proposes Digital clock synchronization using cyclic rotation algorithm (CRA). By using cyclic rotation algorithm we can adjust the clock delays. The dynamic locking is done through clock synchronization, it means matching the clock frequencies. It consist cyclic shift register(CSR). Its operating frequency range is 50MHz and 300MHz.*

Keywords: cyclic shift register(CSR), conventional synchronous mirror delay (CSMD), clock synchronizing, dynamic phase error.

I. Introduction

Every digital system require a clock signal to operate the specified block. For this we require clock generating circuits with high efficiency. we do not design separate clock circuit for each and every block. We design one master clock and from that we distribute to every block in the system. When the frequency of a system clock increases in system-on-chip (SoC), micro-processors and memory interfaces, the efficiency of clock synchronization affects the normal motion of the entire circuit. Fig. 1 shows the clock distributing network in a SoC system. The clock signal in a system might be disabled in hibernation mode in order to save power.

Phase locked loop(PLL)& delay locked loop(DLL) are used in SoC for suppress the clock skew. By using these circuits require more power to lock the clocks. The other approach is synchronous mirror delay SMD[3-8] used for fast clock synchronization . It consume low power but it takes only narrow pulse clock signals.

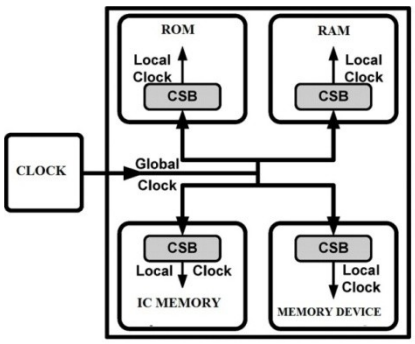

fig. 1 Clock distribution in an SoC

This paper proposes an Digital clock synchronization with CSR algorithm. It is a part of a fine-tune control circuit and designed for CSB. This manuscript is organized as follows. Section II describes architecture of proposed CSB. section III describes the architecture of CSR circuit and its algorithms. section IV contains experimental results and conclusions are detailed in section V

II. Architecture Of Proposed CSB

Before CSB we have a conventional synchronous mirror delay circuit (CSMD) and SMD. These circuits are used to synchronous the clocks, but works for narrow pulse only. Then we go for CSB-clock synchronous buffer circuit[1]. It contain the blocks like coarse delay path, coarse tune control, fine delay path, fine tune control. The proposed architecture of CSB is shown below figure 2,here main block is Fine tune control.

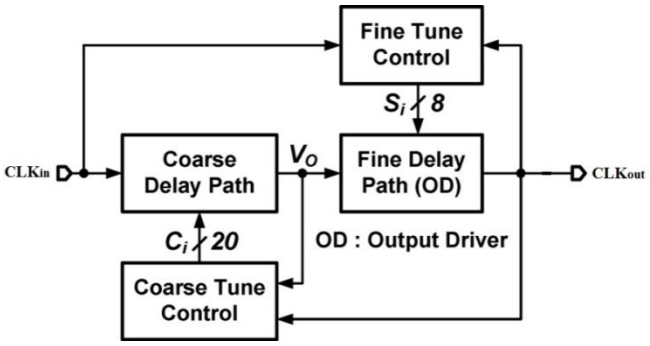

fig.2. proposed architecture of CSB

The coarse delay path consist of buffer and variable delay line. The coarse-control circuit consist of buffer and improved mirror control circuit, and measurement delay line . The fine delay line is also the output driver . The fine tune circuit contain eight bit cyclic shift register. From the figure.2 the clock is input given to coarse delay path circuit , then it applied to fine delay path and coarse tune control circuit to compare error in clock. The clock input is also given to fine tune control circuit , other input is clock output. The working of fine tune control circuit is to check any clock error present at output compare to input .

After comparing the two clocks the fine tune circuit can adjust the output signal . The fine tune circuit can adjust the clocks in two way either in forward or backward delay in clocks. If any delay in output clock then the fine tune circuit can adjust the clock respect to input . The output driver is also named as fine delay path. The output of fine tune circuit is given to fine delay path or output driver. Any error correction in clocks are done through fine tune circuit. The output driver can acts as buffer to store the value of clock state .

III. The Architecture Of CSR And Its Algorithms

From the proposed circuit ,the Fine tune control circuit plays important role for synchronizing the clock pulses. The fine tune control consist of CSR cyclic shift register[1-2] of an eight bit ,which can detect or correct the difference in the clock signals. The fine tune control circuit contain two parts, one 8-bit CSR register and phase detector. The phase detector is used to detect the change / delay in the clocks. The diagram for fine tune circuit is shown in figure .3.

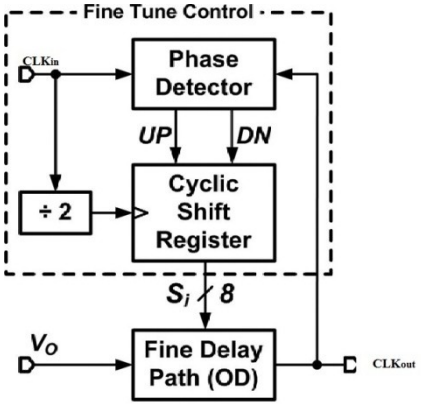

fig.3 Block diagram for fine tune control

3.1 Synchronization of clocks:

The clock synchronizing is matching the frequency of different clocks. Here the figure 4 shows the clock synchronizing of clock input and delay of clock then the output is adjusted and synchronized with respect to input.

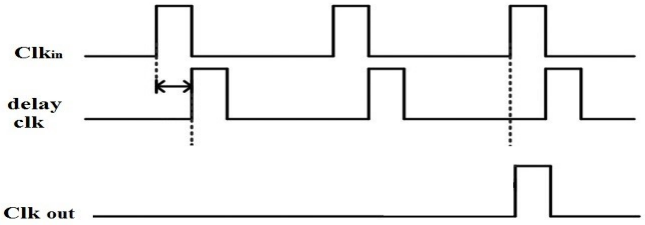

fig.4 synchronization of two clocks

3.2 SAR Algorithm:

The algorithms to implement the fine tune control are two ways, 1.SAR Algorithm, 2.Cyclic Rotation Algorithm. These two algorithms are used to synchronizing clocks, the SAR algorithm refers to Successive approximation register algorithm. The conventional SMD[8] uses SAR Algorithm to decrease static phase error. After fine locking, the SAR sends signal to lock the output. Here the timing resolution needs to be operated as dynamic locking process. For this reason the SAR circuit cannot operate backwards. It means any error regarding backward operation it cannot works well, this is shown in figure 5.

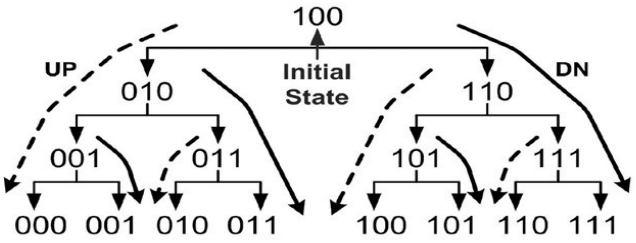

fig.5. SAR algorithm

From the above figure ,the dotted line indicates forward shift or up shift. In the forward sift we don't get any error, but the backward or down shift operation we cannot find in SAR algorithm. This is drawback of SAR algorithm. To eliminate this error we go for Cyclic Rotation Algorithm.

3.3 Block diagram of CSR-Algorithm:

The cyclic rotation algorithm is used to implement the fine tune circuit. The main block diagram of CSR cyclic shift register is shown below figure 6. In this up, down signals are control signals to perform the shift operation to match the frequency of clocks. The signals dm,dp are used to perform shifting operation. From the figure s3 is assumed initial state, then after locking the two clocks then the respected shift operation is performed to match the clocks.

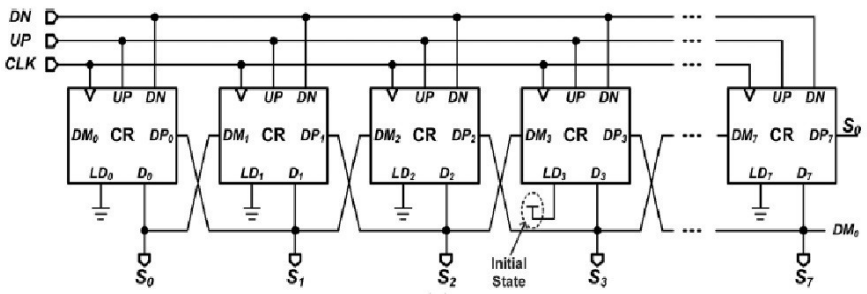

fig.6. CSR block diagram

Each flip-flop having the control signals like ld,data(d). The data stored in each flip-flop is assumed as the clock period. When the clock is having phase difference then the signals up or dn are activated with respect to input. If we have phase difference is forward we have to perform shift left operation to match the clock output with input clock. If we have the phase difference is backward ,then we have to perform shift left operation. Finally we have the output matches with input clock. From the above figure initial state assumed s3

(state) . If both clocks are same then output is in lock range means synchronous stage. If any change of clock with respect to input then shift operation will perform

IV. Experimental Results

The clock synchronization through Cyclic Rotation Algorithm is shown in fig.6. The operating frequency of this circuit is 50M-250MHz. The result in below wave form has calculated when duty cycle is 20%. To get exact results the duty cycle always take below 50%.

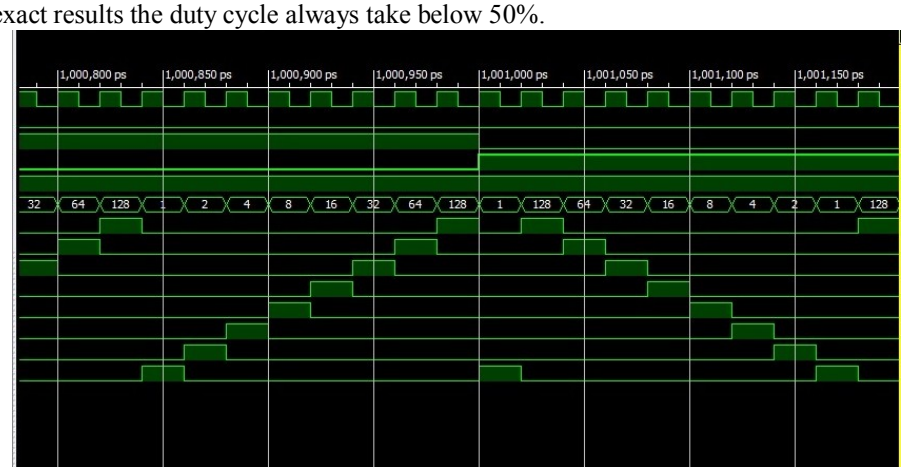

fig.7. clock synchronizing

V. Conclusion

This work proposes digital clock synchronizing through CRA algorithm. This circuit can synchronize the clocks when the duty cycle is less than 50%. The operating frequency range is 50MHz to 300MHz. After locking range the fine tune circuit minimizes the static phase error.

VI. Acknowledgements

Siruvolu Venkata Krishna Rao was born in Wardhannapet, Warangal, India in 1969. He received **A.M.I.E** in **E**lectronics and **C**ommunication **E**ngineering from the **I**nstitution **O**f **E**ngineers (India), Kolkata, India, in 2004 and the M.Tech degree in **VLSI** & **E**mbedded **S**ystems from Kakatiya University, Warangal, Andhra Pradesh, India in 2010. Adding His interest in Personnel management He studied MIRPM(Industrial Relations and Personnel Management) from Alagappa University, Karaikudi, Tamil Nadu during 2004-2006. He worked for Indian Air Force in the Radar Division for considerable period. He has been working as an Assistant Professor in the department of **E**lectronics and **I**nstrumentation **E**ngineering in Kakatiya Institute of Technology and Science, Warangal, Andhra Pradesh, India since Jun 2008. His research interests include VLSI and Embedded Systems design, Networks On Chip Design for Testability

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