A 12-bit Hybrid DAC with Swing Reduced Driver

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Abstract: *This work presents a glitch improved design of a 12-bit fully differential current source resistor string hybrid digital-to-analog converter (DAC) achieved by incorporating a swing reduced driver (SRD) circuit in the existing design. The results show that this design achieves a 13.26 % improvement in glitch reduction in comparison with the original version. The physical layout of the glitch improved design DAC is accomplished within a design area of 489.4 μm x 117 μm or 57260 μm².*
Keywords: *Hybrid DAC, Glitch*

I. INTRODUCTION

As the semiconductor industry moves towards low power and low voltage processes, the glitch occurrence occupy more significance as the phenomenon become more pronounced, and greatly affect the design of high speed DACs. The biggest glitches tend to occur at major code transitions. The major code transition is the point where the most significant bit (MSB) changes from low to high and all other bits change from high to low, and vice versa. Ideally, glitches in these DACs should be as small as possible, especially in high resolution applications.

The hybrid architecture will get the most advantages from different segments such as better Differential Nonlinearity (DNL) and Integral Nonlinearity (INL), while consuming less area and complexity [1]. The basic principle of n-bit current steering DAC is n current sources connected in parallel. The digital input controls which source that is connected to the load. Large input values require more current sources in parallel, which then results in large output current. The current sources must be well matched to obtain improved static linearity performance [2]. Indrit and Ali [3] introduced a new swing reduced driver (SRD) circuit to serve as a gate driver for steering switches of high speed current steering DAC. Peiman and Nasser [4] presented another type of SRD circuit. Joo,Kim and Yoon [5] introduced a SRD circuit which minimizes clock feedthrough effect and prevents the degrading of the dynamic performances due to switching noise. In another approach, degenerated switches are used to reduce glitches. Santanu and Swapna [6] used differential NMOS transistors as current switches. Cheng, Wang and Huang [7] presented another type of degenerated switch.

In this paper a SRD is incorporated in the DAC as an attempt to reduce the glitches, and improve the performance of the DAC. Furthermore, this is an attempt to implement a switch driver in a DAC that has no internal register. The system is designed using SilterraC13 0.13μm 1.8V CMOS technology process parameters and Spectre and Calibre simulations are performed to verify the circuits and layouts.

The paper is organized as follows: Section II introduces the DAC architecture. In Section III, the implementation of the SRD is discussed. The simulation results of the Original@0.13μm and glitch improved version DACs are given in Section IV. Section V summarizes the conclusion
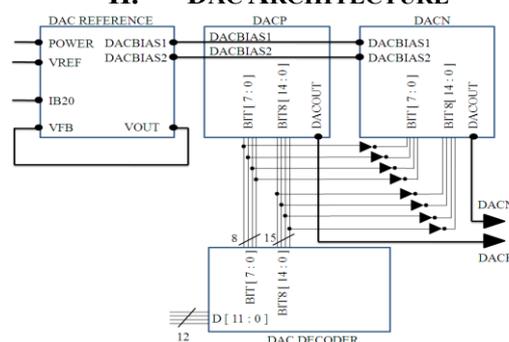
II. DAC ARCHITECTURE

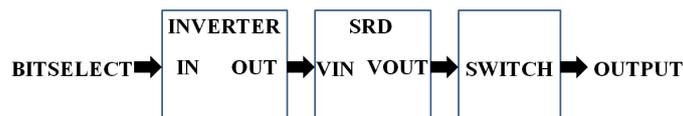Fig. 1 12-Bit Fully Differential Hybrid DAC Architecture

Fig. 1 shows the overall block diagram and its interconnections. The DAC Reference is the most important block that is used to provide constant biasing voltages to DACP and DACN blocks. The DAC Decoder is used to decode 12-bit digital input to appropriate code for both DACs simultaneously. The outputs from the decoder are given directly to DACP, whilst an inverted input is given to DACN. Sum of currents flowing through binary-weighted resistors produce the voltage level which is measured at the output. The outputs of the DACs are obtained from the DACOUT pins. The design is composed of two single-ended DACs and each is referenced to ground. The DAC input is controlled by a 12-bit D[11:0] input. As D[11:0] increases from 0 to 4095, the DACN output decreases respectively from its maximum value to zero Volt, while the DACP output increases respectively from zero Volt to its maximum value. The maximum value in this case is the reference voltage, which is fixed at 1.2V for this DAC [1].

III. METHODOLOGY

Glitch is a phenomenon that occurs when the switching time instants of different bits in a DAC are unmatched. For a short period of time a false code could appear at the output. A SRD circuit is incorporated into the DAC to reduce the glitches. The SRD functions to reduce the swing of the incoming control signals to the inputs of the switches. In normal operation, the control signal swings from V_{DD} to GND. With the usage of SRD, the control signal swing is now reduced. Now, the output swings from V_{OL} (output's low level) to V_{OH} (output's high level), where $V_{OL} >$ GND and $V_{OH} < V_{DD}$ [2].

BITSELECT ➡ SWITCH ➡ OUTPUT

(a) Original@0.13μm DAC configuration

BITSELECT ➡ | INVERTER — IN OUT | ➡ | SRD — VIN VOUT | ➡ | SWITCH | ➡ OUTPUT

(b) Glitch Improved Version DAC configuration

Fig. 2 Block diagram of the proposed method

The SRD block is placed between decoder block and switches, as shown in Fig. 2. An inverter is added before the SRD block to invert the incoming signal beforehand, as the SRD gives an inverted output signal. The reduced voltage swing minimizes the coupling of the switching control signals through the gate-drain capacitance (C_{GD}) to the output node, thus reducing greatly the clock feedthrough effect (CFT) [2], [8]. Fig. 3 shows the circuit diagram of the SRD. The circuit consists of a PM0-NM0 inverter pair and NM1 NMOS and PM1 PMOS diode-connected transistors. NM1 and PM1 transistors functions to maintain the output swing values. The operation of the circuit is as follows: When Vin represents logic '1', or high voltage, NM0 transistor switches on, while PM0 remains off and majority current flows from supply rail through NM1 and NM0 transistors to ground pulling the output to low level. When Vin represents logic '0', or low voltage, PM0 transistor switches on, while NM0 remains off and majority current flows from supply rail through PM0 and PM1 transistors to ground pulling the output to high level [2].
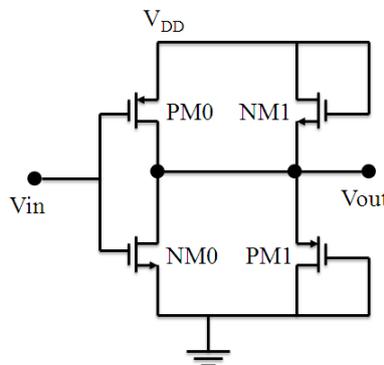
Fig. 3 Swing Reduced Driver Circuit [2]

The SRD circuit gives several design advantages. Firstly, the design of the switches can be relaxed. Usually, switches are required to be designed with minimum length to reduce CFT effect and to maximize the transconductance. By using SRD, the rule is no more compulsory, as SRD is now taking care of the CFT effect.

Secondly, the switching speed is increased. This is because by selecting the difference between switching control signals, the switching times are greatly reduced [2].

IV. RESULTS AND DISCUSSION

The simulations were performed using nominal case models of SilterraC13 0.13μm 1.8 V CMOS process technology. The design was done using Cadence Virtuoso Analog Design Environment Version IC 6.1.4 Schematic and Layout editors, and the results were verified using Spectre and Calibre simulators. Hereafter, to enable easy comparison, the design version without SRD of DAC will be known as Original@0.13μm DAC, whilst the SRD included DAC will be known as glitch improved version DAC.

a. Original@0.13μm DAC
The Original@0.13μm switch circuit and its dimensions are as shown in Fig. 4 and Table 1 respectively [1]. The full scale output voltage is 1.2377 V, with 0.38 μV offset error.
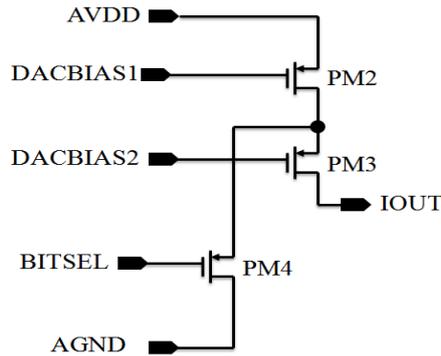

Fig. 4 The Original@0.13μm switch circuit

Table 1: Aspect ratios of switching transistors

Transistor	Width (m)	Length (m)
PM2	4.3 μ	1.8 μ
PM3	4.3 μ	0.6 μ
PM4	2.9 μ	0.6 μ

Fig. 5 shows the glitch occurrence during the transition from 011111111111 (code of bit 2047) to 100000000000 (code of bit 2048) of the Original@0.13μm DAC. The glitch magnitude is 0.6033 V and the glitch impulse area is ≈ 2.11 ns V [9].
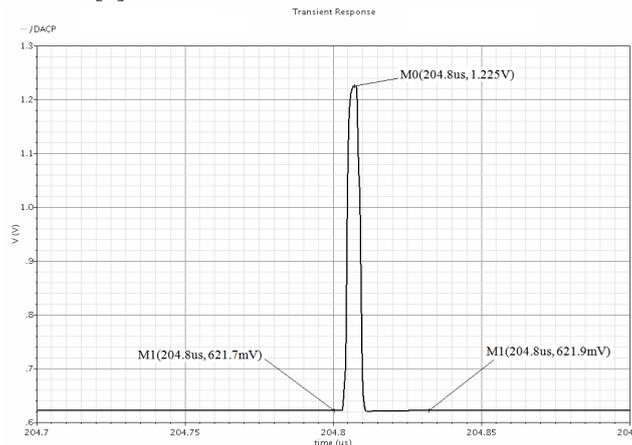

Fig. 5 Glitch occurrence during the transition from 011111111111 (code of bit 2047) to 100000000000 (code of bit 2048) of the Original@0.13μm DAC
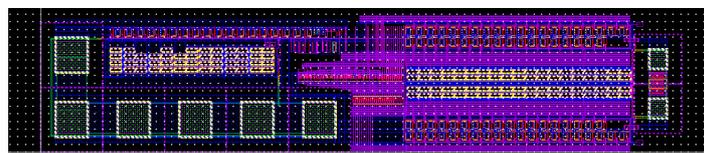

Fig. 6 Layout of the Original@0.13μm DAC

Fig. 6 shows the layout of the Original@0.13μm DAC. Overall layout dimension is 415.7 μm x 89.3 μm = 37122 μm^2.

b. Design of the Glitch Improved Version DAC

The glitch improved version switch circuit diagram and its dimensions are as shown in Fig. 7 and Tables 2, 3 and 4 respectively. Fig. 8 shows the SRD circuit diagram. The full scale output voltage is 1.2377 V, with 4.09 mV offset error.
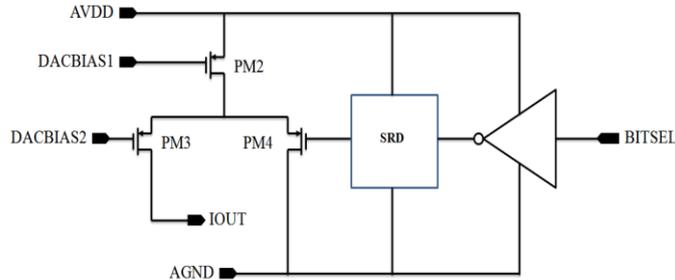

Fig. 7 The glitch improved version switch circuit diagram

Table 2: Aspect ratios of switching transistors

Transistor	Width (m)	Length (m)
PM0	4.3 μ	1.8 μ
PM1	4.3 μ	0.6 μ
PM2	2.9 μ	0.6 μ

Table 3: Aspect ratios of transistors in SRD circuit

Transistor	Width (m)	Length (m)
PM0	6.3 μ	0.35 μ
PM1	4.55 μ	0.35 μ
NM0	4.55 μ	0.35 μ
NM1	6.3 μ	0.35 μ

Table 4: Aspect ratios of inverter

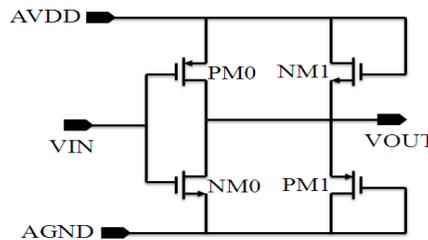| Transistor	Width (m)	Length (m)
PM3	1.45 μ	0.4 μ
NM3	0.7 μ	0.4 μ

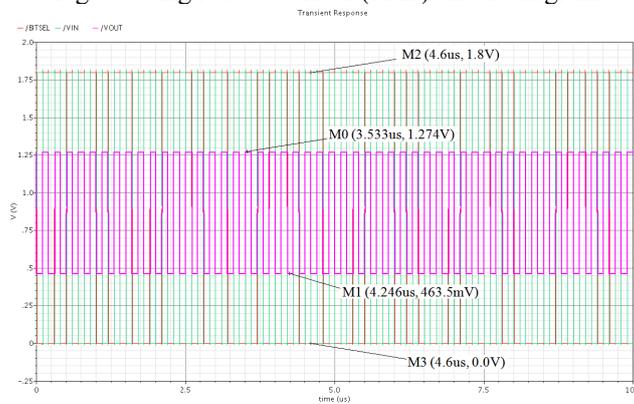Fig. 8 Swing reduced driver (SRD) circuit diagram

Fig. 9 SRD output and Input

Fig. 9 shows the SRD output obtained after implementing the circuit. The output voltage swing is between 1.274V and 463.5 mV. The magnitude of output voltage swing, VOUT, is now 810.5 mV.
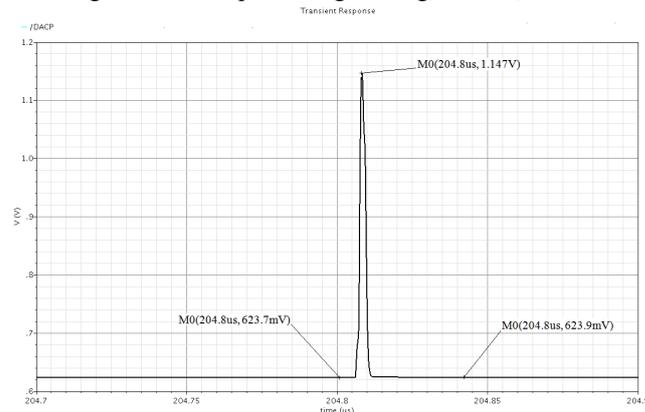

Fig. 10 Glitch occurrence during the transition from 011111111111 (code of bit 2047) to 100000000000 (code of bit 2048) of the glitch improved version DAC

As shown in Fig. 10, the glitch magnitude is 0.5233 V and the glitch area is ≈ 1.047 ns V [9]. It is a 13.26 % improvement in terms of the peak value of the glitch when compared to the Original@0.13μm version DAC. Fig. 11 shows the layout of the glitch improved version DAC. The overall layout dimension is 489.4 μm x 117 μm = 57260 μm^2. The area increase is 54.2 % compared to Original@0.13μm DAC.
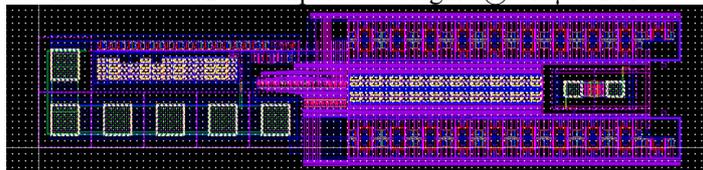

Fig. 11 Layout of glitch improved version DAC

V. CONCLUSION

A glitch improved version design of a 12-bit fully differential current source resistor string hybrid DAC is presented. The proposed DAC incorporates a SRD circuit which is implemented in front of the switches of the current-steering DACs. By doing this, decreased voltage swing reduces the digital signal feedthrough to the output nodes. In addition, the switching times of the transistors are reduced and this would enable possible high speed operation of the switchable current sources. The physical layout of the DAC has been implemented in SilterraC13 0.13μm 1.8V CMOS process by incorporating good layout techniques to produce optimum performance.

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