IOSR Journal of VLSI and Signal Processing (IOSR-JVSP)
Volume 3, Issue 6 (Nov. – Dec. 2013), PP 32-36
e-ISSN: 2319 – 4200, p-ISSN No. : 2319 – 4197
www.iosrjournals.org

Traffic and Power Reduction Routing Algorithm for Noc Cores

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Abstract: *With the progress of VLSI technology, the number of cores on a chip multiprocessor keeps increasing, Now a days we are increasing the processing level of the chip ,NOC is a best method to interconnect the core with each other core on the chip, In this paper we are creating a network concept on a chip by interconnecting the core with each other core. Then we are reducing the overall chip power and Traffic level by sharing the work load with other cores on the chip, And Dynamic Voltage Frequency Scaling (DVFS) is the technique for monitoring the Frequency/Voltage level of each core on the chip and providing sufficient power to the cores, Application Traffic Prediction Table(ATPT) is a Table that having (low and high) Frequency level table of the Each core. ATPT has very high prediction accuracy. Depends upon the ATPT table voltage/frequency is given to the cores by DVFS.*

Keyword: Network On Chip, Traffic prediction, Dynamic voltage frequency scaling, Application traffic prediction table Table

I. Introduction

increasing the clock frequency to increase performance is no longer an option due to, amongst others, energy consumption, heat developments and the enormous costs for new technologies. Power and thermal distribution are two critical problems in current chip design. With the progress of VLSI technology, the number of cores inside one chip is still increasing, so from multi core to many-core, the Network-on-Chip (NoC) is the most widely used solution to interconnect the cores. For example, Tilera's TILE64 uses a 2D mesh network to interconnect64 general purpose tiles, and explicit tile-to-tile communication is supported. When cores are interconnected by the NOC, additional problems need to be considered, such as power consumption and heat from switches the control of traffic and intercommunication timing between tasks. Apparently, the NoC plays an important role in the many-core design, The increasing number of cores requires a communication system different from a conventional bus system, since a bus quickly becomes the bottleneck of the system. One approach is to employ a Network on Chip (NoC). With the ongoing trend to increase the number of cores on CMPs, the NoC becomes an essential part of the system.There are many NoC topologies such as meshes, trees, multistage interconnection networks (MINs), and many more. NoCs have several advantages such as scalability and modularity.

According to this observation, in this paper we propose a novel application-driven approach for predicting traffic in NoC and performing DVFS on communication links. We consider message-passing many-core architectures, in which cores communicate with each other directly through explicit message passing. The basic idea is to capture the communication patterns between parallel tasks, i.e., the end-to-end traffic, by using a small table in the network interface (NI) of each core to record the outgoing messages from that core. The novel data structure is called the *Application-driven Traffic PatternTable* (ATPT).

With the support of ATPTs, the amount of data injected into the NOC from each core can be predicted. Once the predictions are made, the utilization of each individual link can also be derived. The voltage/frequency (VF) level of the link can thus be adjusted proactively based on the predicted link utilization. In comparison to previous studies that make the DVFS decision based on the hardware status, our approach uses the data transmission behavior of the application as the VF scaling reference. The data transmission behavior is a better guide, because it is more predictable and the repetitive behavior exists in the execution phase.

II. Traffic And Power Reduction Technique

NOC system is the best method for interconnecting the core with each other cores, The main contribution is power and traffic, In this proposed system we are reducing the overall traffic level and overall power consumption of the chip .Here the End to End data transmission has monitored by Dynamic Voltage Frequency Scaling(DVFS),Depends upon the data transmission rate the power has given to the cores, this is the method to manage the wastage power ,so the total chip power as reduced. If the data rate is high that core considering as a overload system, that time the data's are shared with other core on the same chip, By sharing

the data's with other core,we can manage the traffic level. So there is no need to give more power to the core like the existing system.

MERITS

- By Sharing the overload data's with other core, We can manage the traffic level. So the overall chip traffic level is reduced.
- Depends upon the data rate the power as given to the cores.
- If the core has been idle for a while, Then the core is set to be a low power mode.

Various architectures and routing algorithms have appeared in the last two decades in order to decrease the overhead to both the data rate as well aship size. This document contains an overview of popular tactics devised for adaptive routing on multiprocessor microchips

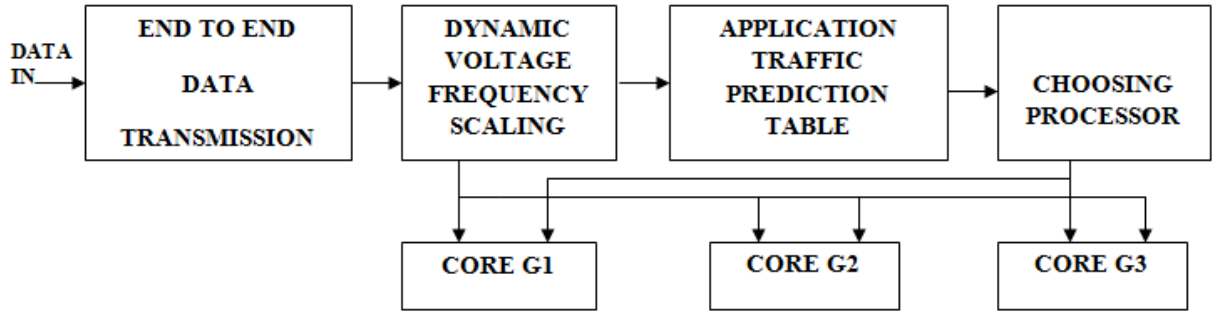


Fig:Block Diagram of Traffic and power prediction

The above Block is representing the technique of predicting and reducing the power and traffic level of the chip(processor),

III. End-To-End Traffic Prediction

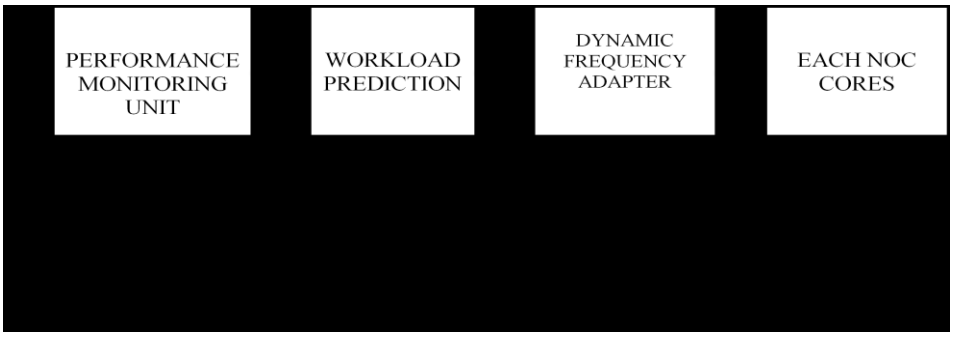
Normally it is important to know the specific NoC topology to be able to analyze it. In order to generalize our method we do not consider the specific network topology. Instead, our goal is to predict end-to-end communication. This means that we do not consider the switching elements between the nodes. It is also irrelevant which type of components (e.g. core, memory, I/O) is connected to the NoC. Every component is simply seen as a node. The NoC is considered as black box to which several node are connected. The structure of the model is depicted. For the communication between nodes it is important to know which nodes want to exchange information between them and when. Therefore the point of time at which communication takes places and the amount of data that is transmitted are needed. With these assumptions the problem of predicting traffic in NoCs is similar to predicting a time series.The End to End is nothing but,The Data transmitting from one core to another Core,The all core of the processor is connected by the Routers,

- ROUTER (i1) to Core G1 (j) ===> (i1--->j)
- ROUTER (i2) to Core G2 (k) ===> (i2--->k)
- ROUTER (i3) to Core G3 (l) ===> (i3--->l)

IV. Dynamic Voltage Frequency Scaling

DVFS techniques may be used to reduce the energy consumption of an executed task while ensuring that the task meets its deadline. However, these techniques are not directly applicable to general-purpose operating systems because they assume that critical information about all tasks, such as the task arrival time, deadline, and workload, are known in advance. Moreover, the workload of a task is often represented by the number of clock cycles required to complete the task regardless of whether the workload consists of mainly memory-bound instructions. The latter information is, of course, critical in determining the idle time of the Chip.

In this paper, we propose an intra-process DVFS technique for non real-time operation in which finely tunable energy and performance trade-off can be achieved. The main idea is to lower the frequency during the idle times, which are, in turn, due to external memory stalls. Now if the task execution time is dominated by the memory access time, then the speed can be slowed down with little impact on the total execution time. This could, however, result in potentially significant savings in energy consumption.



PERFORMANCE MONITORING UNIT:

- Monitoring the Core performance (Bits/sec)

WORKLOAD PREDICTION :

- Checking the Traffic level of each and every core of the system

DYNAMIC FREQUENCY ADAPTER :

- It's the unit of giving the capable frequency to the cores

The main contributions of this work are as follows:

1. We explore the energy savings offered by implementing both temporally fine-grained and per-core DVFS in a 4-core CMP system using an offline DVFS algorithm.
2. We present a detailed on-chip regulator model and design space analysis that considers key regulator characteristics—DVFS transition times and overheads, load current transient response, and regulator losses.
3. We combine the energy savings with the on-chip regulator cost models and come to several conclusions. For a single power domain, on-chip regulator losses offset the gains from fast DVFS for many workloads. In contrast, fast, per-core DVFS can achieve energy savings (>20%) when compared to conventional, single power domain, off-chip regulators with comparatively slow DVFS.

Since traffic predictions and DVFS adjustments are both based on a single time interval, the VF level of a link, should be set to complete the transmissions of all the predicted workload from all the end-to-end transmissions passing through in one interval. The problem is that DVFS and traffic predictions affect each other. In the following, we examine the effects. Consider a link in the NoC.

There are two cases:

1) The utilizations of all these links are correctly predicted. The VF level of *ei*can then be set accordingly, which should satisfy the required bandwidth. Thus, no congestion will be created.

2) The utilizations are predicted wrongly (either over- or under-estimated) in some of these links. The ATPT predictors will detect the errors and refine their predictions. In addition, ATPTs use hybrid predictors. When the POP predictor fails to find patterns, ATPT will switch between POP and LVP to better match the actual traffic. One may argue that the correcting process maybe too slow and delayed data may be accumulated to cause congestion. This is actually a matter of how aggressively we adjust the VF level on mispredictions. In Section VII-B4, we will examine the effects of different strategies to DVFS adjustment.

V. Atpt-Based Predictor

The basic idea is to capture the communication patterns between parallel tasks, i.e., the end-to-end traffic, by using a small table in the network interface (NI) of each core to record the outgoing messages from that core. The novel data structure is called the *Application-driven Traffic PatternTable* (ATPT). With the support of ATPTs, the amount of data injected into the NOC from each core can be predicted.The ATPT is a two-level table for predicting the end-to-end traffic between the local tile with other tiles in the next time interval [11]. The design is inspired by the branch prediction. Figure 2 shows the high level design. An ATPT sits besides each network interface card (NIC) for monitoring the amount of data transmitted out of the NIC in a time interval.

- End-to-end flow control for controlling the injection rate.
- Controlling the power mode of switches.
- Modeling the thermal distribution of a chip while taking both cores and switches into consideration simultaneously.

The ATPT can be applied in the following scenarios:

CORE G1,G2,G3	G1 (0 – 50) Bits/Sec	G2 (50 – 100) Bits/Sec	G3 (100 – 150) Bits/Sec
CORE G1 (0 – 50)	G1 Is Running	IDEAL	IDEAL
CORE G2 (0 – 100)	G1 Is Running	G2 Is Running	IDEAL
CORE G3 (0 – 150)	G1 Is Running	G2 Is Running	G3 Is Running

- Optimizing the inter-communications of the application at runtime.
- Three different strategies on DVFS in communication links are proposed that satisfy different optimization goals.

VI. Concept Of Atpt

An ATPT Table having two type of Data's
i. Low Frequency Value.
ii.High Frequency Value.
Inside the processor each core having some working frequency range. Depends upon the ATPT table the core can be operates in low power mode and normal mode. ATPT Table is shown above, Here we are considering CoreG1,G2,G3,Each core is capable to run in the range of (0-50),The core Running Functions are Bellow

RUNNING FUNCTION OF CORES:

I.TRANSMISSION RANGE (0-50)Bits/Sec :

Core G1 is Running at the Range of (o – 50) Bits/Sec
Core G2 and G3 Is IDEAL when the Transmission Range is 0 – 50 Bits/Sec

II.TRANSMISSION RANGE (0-100) Bits/Sec :

When the data transmission is crossed above 50 Bits/Sec , The Data has been shared to Core G2
So Core G1 & G2 Is Running at the Range of (0-100)Bits/Sec
Core G3 is IDEAL on that stage

III.TRANSMISSION RANGE (0-150)Bits/Sec :

When ever the data transmission is above 100Bits/Sec , The Data has sharing with G3
Core G1,G2&G3 is Running in the particular Range of (0-150)Bits/Sec

VII. Related Works

One way to model power consumption of an NoC is to derive detailed capacitance equations for various router and link components, assuming specific circuit design for each component. These equations are then plugged into a cycle accurate simulator so that actual network activity triggers specific capacitance calculations and derives dynamic power estimates. The capacitance for each network component is derived based on architectural parameters. The other approach is to evaluate the energy and power consumption of each component by using gate level simulation with technology libraries. There have been several power estimation approaches for network components in NoC..first noted the need to consider over constraints in interconnection network design, and proposed an analytical power model of switch and link. Wang et al. presented the architectural-level parameterized power model named Orion by combining parameterized capacitance equations and switching activity estimations for network components. These analytical models are based on evaluation of switching capacitance and estimate dynamic power consumption.

Chen and Pehextended the Orion by adding the leakage power model, which was based on empirical characterization of some frequently used circuit components. Ye et al. analyzed the power consumption of switch fabric in network routers and proposed the bit-energy model to estimate the power consumption. However, the models are tightly coupled with circuit implementations. As such, these models cannot be migrated to different technology libraries without a large amount of re-modeling. Moreover, low level of abstraction (i.e. gate and device level) and the extremely slow simulation make it definitely unsuitable to face with system level SW/HW exploration task.

Power Management for NoC. In the power consumption of the interconnection network has been addressed. Servers are not only energy drains; research on the chip level multiprocessor found that the network-on-chip consumes around 36% of the whole energy of the system. In the architectural power model for an on-chip network has been proposed for estimating and evaluating the design of the network-on-chip. Also, the

power model has been ported into a full-system simulator. In frequency tuning for on-chip networks is well addressed.

In comparison to the previous work on this topic, our study is the first one to take advantage of the real application behaviors, not only to monitor and predict the NoC, but also to control the link VF by the application behaviors

VIII. Conclusion

In this paper we are reducing the Traffic and power level of the chip, By using DVFS technique,And there are two types of (high and low) frequency table for predicting the Data rate of each cores, If the data rate is high that time the data has been shared with other core so the traffic level is reduced, To solve the power consumption problem in NoC, previous works have proposed techniques such as *dynamic voltage/frequency scaling* (DVFS) to adjust the power mode of the switches and links to match the traffic flows.The challenge is to predict the traffic flowing through the switches and links in the next time interval. For example, if a switch or a link can be predicted to be idle for a while, then it can be set to a low power mode by lowering its voltage or frequency.

Reference

[1]. S. Bell, B. Edwards, J. Amann, R. Conlin, K. Joyce, V. Leung,J. MacKay, and M. Reif. TILE64 Processor: A 64-Core SoC withMesh Interconnect. In *IEEE International Solid-State CircuitsConference*, February 2008.

[2]. U. Nawathe, M. Hassan, K. Yen, L. Warriner, B. Upputuri, D. Greenhill,A. Kumar, and H. Park. An 8-Core 64-Thread 64b Power-EfficientSPARC SoC. In *IEEE International Solid-State Circuits Conference*,

[3]. February 2007.

[4]. S. Bell, B. Edwards, J. Amann, R. Conlin, K. Joyce, V. Leung,J. MacKay, M. Reif, L. Bao, J. Brown, M. Mattina, C.-C. Miao,C. Ramey, D. Wentzlaff, W. Anderson, E. Berger, N. Fairbanks,D. Khan, F. Montenegro, J. Stickney, and J. Zook. Tile64 -processor: A 64-core soc with mesh interconnect. In *Solid-StateCircuits Conference, 2008.ISSCC 2008. Digest of TechnicalPapers. IEEE International*, pages 88–598, Feb. 2008.

[5]. A. B. Kahng, B. Li, L.-S. Peh, and K. Samadi. Orion 2.0: Afast and accurate noc power and area model for early-stage

[6]. design space exploration. In *Proc. DATE '09.Design,Automation. Test in Europe Conference. Exhibition*, pages423–428, Apr. 20–24, 2009.

[7]. T. Ishihara and H. Yasuura, "Voltage scheduling problem fordynamically variable voltage processors," Proc. *Int'l Symp.on Low*

[8]. *Power Electronics and Design*, 1999, pp.197-2026. I. Hong, G. Qu, M. Potkonjak, and M.B. Srivastava, "Synthesistechniques for low-power hard real-time systems on variable voltageprocessor," *Proc. of the IEEE Real-Time Systems Symp*. December 1998,

[9]. pp.178-187

[10]. C. Isci, G. Contreras, and M. Martonosi.Live, runtime phase monitoring and prediction on real systems with application to dynamic power management. In *MICRO 39: Proceedings of the 39th Annual IEEE/ACM International Symposium onMicroarchitecture*, pages 359–370, Washington, DC, USA, 2006. IEEE Computer Society.

[11]. S. Sarangi, B. Greskamp, R. Teodorescu, J. Nakano,A. Tiwari, and J. Torrellas. VARIUS: A model of process

[12]. variation and resulting timing errors for microarchitects.*IEEE Transactions on Semiconductor Manufacturing*, 21(1), 2008.

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