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Standard Cell Library Design and Characterization using 45nm technology

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Abstract: *Producing designs based on sub-micron technologies at a competitive cost has always been a challenge for the manufacturers. Different Integrated Circuit (IC) implementation approaches have been adopted to reduce the design time and improve manufacturing costs. One of the methods is to use a 'Cell-Based' IC implementation approach using Standard Cell Libraries However, the cost associated with the design or purchase of Standard Cell Libraries (Non-Recurring Expense (NRE)) has been increasing consistently with the shortening of device technology. In this paper we present the development of submicron CMOS Standard Cell Library that is suitable for 45nm CMOS process The intent was to generate a comprehensive library containing core number of necessary cells, providing detailed layout and transistor-level schematic views of every cell, with characterization under the 45nm process, in order to utilize them as a fully synthesizable library. The library is designed using Cadence.*

Index Terms: *standard cell library, 45nm process, layout design, characterization*

I. Introduction

Integrated Circuit (IC) technology has gone through a spectacular revolution in the last two decades. The number of transistors that can be integrated on a single die has been exponentially increasing with time following the Moore's Law. Present day microprocessors have more than one million transistors and are clocked at Giga Hertz (GHz) clock speeds. Bringing these high development cost associated high performance designs to the market at a competitive cost and in a lesser design time has always been a challenge for IC manufactures. To meet these challenges, different IC implementation approaches have been adopted ranging from custom design approach, used for microprocessors and memories to the fully programmable designs for medium – to – low performance applications

A. Cell Based Semi-Custom Design

With the advancement of design automation, Cell Based Semi-Custom IC implementation approaches have been introduced to shorten and automate the design process. The idea behind 'Cell Based' design is to reduce the design cost and design time by reusing a library of cells called Standard Cell Library. The disadvantage is that the cells in the library decide the integration density and/or performance reducing the ability to fine-tune the IC design.

B. Standard Cell Library

The Standard Cell Library contains a collection of logic gates over a range of fan-in and fan-out. Besides the basic logic function, such as inverter, NAND, NOR, XOR and Flip- Flops, a typical library also contains more complex functions such as Multiplexers, Full-Adder, Comparator, etc. As shown in Fig 1, the Standard Cell Library is used in the Semi-Custom Design Flow to shorten the design process.

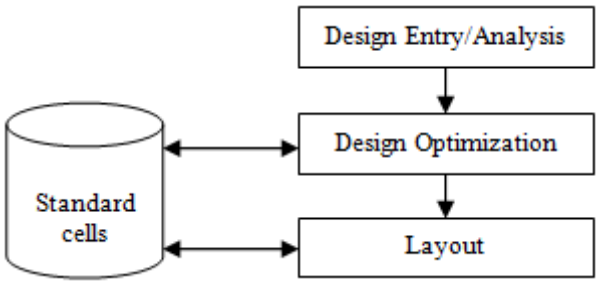

Fig 1: Semi–Custom Design Flow

It should be noted that a successful and efficient implementation of a Semi-Custom Design depends on the standard cells in the library. Therefore, it is important to have a 'high quality cell library'.
A 'high quality cell library' possesses many common characteristics including:
• Cells functionality being correct.
• Cells timing performance claimed in the data sheet being accurate enough.
• Cells having no design rule violations in their layouts.
• Cells can be utilized in the best way using a synthesizer.
• Cells can optimize placement and route of a large design.
These characteristics help in an efficient integration of Standard Cell Library into a Semi- Custom Design Flow.
A typical standard-cell library contains two main components:
1. Library Database - Consists of a number of views often including layout, schematic, symbol, abstract, and other logical or simulation views. From this, various information may be captured in a number of formats including the Cadence LEF format, and the Synopsys Milky way format, which contain reduced information about the cell layouts, sufficient for automated "Place and Route" tools.
2. Timing Abstract - Generally in Liberty format, to provide functional definitions, timing, power, and noise information for each cell.
A standard-cell library may also contain the following additional components:
- A full layout of the cells
- Spice models of the cells
- Verilog models or VHDL Vital models
- Parasitic Extraction models
- DRC rule checks

II. Standard Cell Library Design

The 'Cells' or logic gates selected to build the library depends on the design requirement. These cells when used in the Semi-Custom Design Flow have to meet certain functions and performance. The cells are either area optimized or speed optimized. The area optimized cells uses minimum sized transistors while the speed optimized cells uses larger transistors to provide good driving capabilities. The Standard Cell Library development process can be depicted using a flow chart as shown in Fig 2.

The design specification of a particular cell in the library is decided and the initial design is done. It is checked whether the design meets the required specification. After this, the 'Layout' of the designed cell is carried out and a netlist is extracted from the 'Layout'. The netlist obtained from the 'Layout' is compared with the initial design. If the results match, then the design cycle is complete else, redesigning has to be carried out and the cycle is repeated.

The sizes of PMOS (Wp) and NMOS (Wn) of the transistors in the Cells are selected to meet design specifications such as power dissipation, delay, noise immunity and area. Therefore, the sizing constraint for Standard Library Cells is similar to any MOS circuit design requirement of minimum area subject to delay less than or equal to the required timing specification. Therefore, Wp and Wn are determined by
• DC switching point.
• Drive capability of the cell.

It should be noted that while designing the cells and deciding the 'sizes' of the cells, process variations should also be considered for proper functioning cells at the end of fabrication. After the cells have been designed and simulated, to ensure proper functionality and timing, cells have to be characterized to obtain different parameters (power, timing, etc.). This requires multiple executions of circuit simulators for each cell. An 'automatic cell characterization tools' are used for this purpose. The final requirement is documentation that summarizes the functionality and timing of each cell.

III. Design Flow Adopted For The Standard Cell Library Development

Each cell in the library was developed using the Bottom-Up design flow. The Bottom-Up Design flow is given in Fig 2. Each block in the figure can be described as follows.

A. Design Specifications

The Bottom-Up design flow starts with a set of design specifications. The "specs" typically describe the expected functionality of the designed circuit as well as other properties like delay times, area, etc. To meet the various design specifications certain design trade offs (area verses delay) are required.

B. Schematic Capture

A Schematic Editor is used for capturing (i.e. describing) the transistor-level design. The Schematic Editors provide simple, intuitive means to draw, to place and to connect individual components that make up the design. The resulting schematic drawing must accurately describe the main electrical properties of all components and their interconnections. Also included in the schematic are the supply connections (Vdd and Gnd), as well as all pins for the input and output signals of the circuit. From the schematic, a netlist is generated, which is used in later stages of the design. The generation of a complete circuit schematic is therefore the first important step of the transistor-level design.

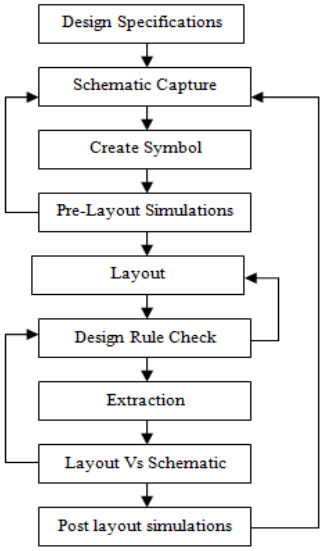

Fig 2 design flow of standard cell library

C. Symbol Creation

A symbol view of the circuit is also required for some of the subsequent simulation steps or for documentation purposes. Thus, the schematic capture of the circuit topology is usually followed by the creation of a symbol to represent the entire circuit. The shape of the icon to be used for the symbol may suggest the function of the module (logic gates – AND, OR, etc.), but the default symbol icon is a simple rectangular box with input and output pins. The symbol creation will also help the circuit designer to create a system level design consisting of multiple hierarchy level.

Table 1: switching characteristics of 2 input XOR gate of different drive strengths

	PMOS width(nm)	NMOS width(nm)	Tplh (ps)	Tphl (ps)	Tr (ps)	Tf (ps)	CL (Load Capacitance)
Xor2_1x	590	240	21.313	22.712	23.639	25.334	Cinv
Xor2_2x	1180	480	21.242	23.200	22.425	22.902	2 Cinv
Xor2_4x	2400	960	21.300	23.503	21.138	22.776	4 Cinv
Xor2_8x	4900	1800	25.560	24.728	22.283	23.504	8 Cinv

D. Pre-Layout simulation

After the transistor level description of a circuit is completed using the schematic editor, the electrical performance and the functionality of the circuit must be verified using a simulation tool. Based on simulation results, the designer usually modifies some of the device properties in order to optimize the performance. The initial simulation phase also serves to detect some of the design errors that may have been created during the schematic entry step. Table 1 shows the switching characteristics of 2 input xor gate of different drive strengths for pulse input (Ton=Toff=10ns, Tr=Tf=50ps, Cinv=0.3fF)

E. Layout

The creation of the mask layout is one of the most important steps in the full-custom design flow, where the designer describes the detailed geometrics and the relative positioning of each mask layer to be used in actual fabrication, using a Layout Editor. Physical layout design is very tightly linked to overall circuit performance since the physical structures determines the transconductances of the transistors, the parasitic capacitances and resistances, and obviously the silicon area which is used to realize a certain function. But the process is very intensive and time-consuming design effort. It is also extremely important that the layout design

must not violate any of the layout design rules, in order to ensure a defect free fabrication of the design. Fig 3 shows the layout of 3 input XOR gate of 4x drive strength.

The layout process can be a manual process, in which layout of each design is done manually or an automatic process using a CAD tool. But the quality of the layouts produced using automatic processes are still far from hand optimized layouts.

F. Design Rule Check (DRC)

The created mask layout must conform to a complex set of design rules, in order to ensure a lower probability of fabrication defects. A tool built in to the layout editor called Design Rule Checker, is used to detect any design rule violations during and after the mask layout design. If errors are detected, they should be removed from the mask layout, before the final design is saved.

G. Circuit Extraction

After the mask layout has been made free from design rule errors, circuit extraction is performed to create a detailed netlist for the simulation of the circuit. The circuit extractor identifies the individual transistors and their connections as well as the parasitic capacitances and resistances that are inevitably present. The extracted netlist can give a very accurate estimation of the device dimensions and device parasitics that ultimately determine the circuit performance. The extracted netlist are used in transistor level simulations and in Layout Verses Schematic comparison.

H. Layout VS Schematic Check

After the mask layout design of the circuit is completed, the design should be checked against the schematic circuit description created earlier. The 'Layout Verses Schematic (LVS) Check' will compare the original network with the one extracted from the mask layout. The LVS step provides an additional level of confidence for the integrity of the design, and ensures that the mask layout is a correct realization of the intended circuit topology. Also it should be noted that a successful LVS would not guarantee that the extracted circuit would actually satisfy the performance requirements since LVS check guarantees only a topological match. If any errors show up during LVS, then it should be corrected before proceeding to post layout simulation.

I. Post-Layout Simulation

The electrical performance of a full custom design can be best analyzed by performing a post-layout simulation on the extracted circuit netlist. The detailed simulation performed using the extracted netlist will provide a clear assessment of the circuit speed and the influence of circuit parasitics. If the results of the post-layout simulation are not satisfactory, the designer should modify the transistor dimensions or the circuit topology, in order to achieve the desired circuit performance. Thus, it may require multiple iterations on the design, until the postlayout simulation results satisfy the original design requirements. Finally, it should be noted that a satisfactory result in post-layout simulation is still no guarantee for a completely successful product, since the actual performance of the chip can be only be verified by testing the fabricated prototype.

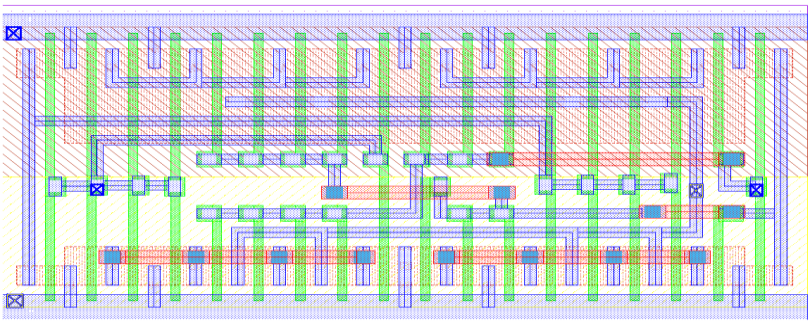

Fig: 3 input XOR gate of drive strength 4X

IV. Characterization Process

The cells are simulated to ensure proper functionality and timing. The results from the initial design and extracted values are compared. There are many models which we can use to simulate the nominal process from the fabrication. Measurements of all delay times are at 50% to 50% Vdd values. All rise/fall times are 10% to 90% Vdd values. To obtain realistic manufacturing process characteristic, circuit simulation is performed with temperature, voltage and process parameter over the range of values that are expected to occur. The critical values at process comer are simulated with minimum and maximum condition. To exercise all input-to-output

paths through the cells, input stimulus will be provided to the circuit simulator. Since many repetitive executions of the circuit simulator are required for each cell, the characterization is done using an automatic cell characterization tool. Table 2 shows characterization values of inverter for process=TT, voltage=1.1v and temperature= -40 degree centigrade.

Table 2: characterization table of inverter

C_L (Ff) SLEW(ps)		C1=0.3	C2=0.6	C3=1.2
5	**Tplh**	6.7475	9.7600	15.594
	Tphl	5.6518	8.0261	12.858
	Tf	7.7848	12.745	23.081
	Tr	10.298	17.035	30.377

After characterizing, the cells functional description and timing data are transformed to the format required by a specific design tools. Most design tools utilize special-purpose model formats with syntax for explicitly describing propagation delays, timing checks, and other aspects of cell behavior that are required by the tool. The final requirement is a documentation that summaries the functionality and timing of each cell. The functionality is frequently described with truth table, and timing data is presented in a simple format in the datasheet. The documentation for each library contains:

• Setup and hold times
• Operating range of temperature and voltage
• Fan-in and fan-out
• Variation of timing due to temperature and
• Voltage
• Path delays
• Library cell symbol
• Timing diagrams.

V. Conclusion And Future Works

Digital standard cell library is very useful in ASIC design. Standard library cells improve designer's productivity through reduced design time and debugging. Implementing this flow using CAD tools available in market, you can design standard cell library.

In future more investigations have to be done on the behavior of transistors in series. To improve the efficiency of the library for building complex design, mega cells such as: 1 bit register file slice, a 1 bit ALU, p-decoder, UART, PIO/PIA microcontroller core, fixed point DSP core, FIFO, SRAM should be included in the existing library. To achieve higher speed and lesser area transistors can be scaled and single and double height cells can be implemented. Few analog cells and filler cells can be included.

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References

[1] Jan M. Rabaey et al., "Digital integrated circuit – A Design Perspective", Second Edition, Prentice Hall, 2003.
[2] HSPICE® Reference Manual: Commands and Control Options Version B-2008.09, September 2008 (Synopsis)
[3] Ashral bin Bahari Tambek, Ahmad Raif bin Mohd Noor Beg, Mohd Rais Ahmad, "Standard Cell Library development", in Proceedings of the 11th International Conference on Microelectronics, 1999, pp.22-24.
[4] Weitong Chuang, Sachin S. Sapatnekar, Ibrahim N. Haji, "Timing and area optimization for Standard-Cell VLSI circuit design", IEEE Trans. on Computer-Aided Design of Integrated Circuits and Systems, vol. 14, March 1995.
[5] CMOS IC LAYOUT Concepts, Methodologies, and Tools by Dan Clein
[6] Ron Wilson, EE Times, May 2000.
[7] www.InnovationRevolution.com
[8] Microelectronics Group at Worchester Polytechnic Institute, "Cadence Design Tools Tutorial", October 1999, http://www.vlsi.wpi.edu/cds/explanations.
[9] Masakazu Shoji, "CMOS Digital Circuit Technology", Prentice Hall, 1988.
[10] CMOS VLSI Design: A Circuits and Systems Perspective by Neil H.E. Weste, David Harris, Ayan Banerjee, Wesley, 1993.
[11] R. Jacob Baker et al., "CMOS – Circuit Design, Layout and Simulation", Wiley-IEEE Press, 1997.
[12] www.mosis.org