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A Fault Analysis in Reversible Sequential Circuits

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Abstract: *In this paper,the researchers propose the design of reversible circuits using reversible gates.Reversible logic is implemented in reversible circuits.Reversible logic is mostly preferred due to less heat dissipation.Conservative logic gates can be designed in any sequential circuits and can be tested using two test vectors.The significance of proposed work lies in the design of reversible sequential circuits and their equivalent circuits for maximum fault coverage.The design of reversible sequential circuits using Toffoli gate and Peres gate is proposed in this literature.The design of Toffoli and Peres equivalent circuits is proposed first time in this literature, in order to achieve maximum fault coverage. The proposed Toffoli and Peresgates surpass the Fredkin gate and MXCQCA gate in terms of area, number of gates and timing. The simulation and coding is performed using cadence tool.*

Keywords: *Reversible logic, Peres gate, Toffoli gate, Feynman gate, latches.*

I. INTRODUCTION

Reversible logic is one of the property in which there exists the one-one mapping between input and output. Reversible logic has the same number of inputs and outputs.It produces the output pattern for each input. Energy loss is avoided by reversible logic.Various scientists have undergone research on reversible logic like Landeuer's and Benett. Landauer has undergone research on irreversible logic where each bit of information generates KTln2 Joules of heat energy. Benett proved that KTln2 energy dissipation would not occur if a computation takes place in a reversible way. Reversible logic is suitable for many applications like Low Power Consumption, Quantum computers, Nanotechnology and Speedimprovement. Fanouts are not allowed in the reversible logic synthesis. Reversible logic synthesis differs from irreversible logic synthesis.

Various definitions can be formed using reversible logic. They are reversible function, reversible logic gate, garbage, Quantum cost, gate levels or logic depth, Flexibility and gate count. Reversible logic can be synthesized using Combinational and sequential logic. Most of the researchers took place on combinational logic, but in Sequential logic require the memory cells and feedback in a circuit.

In this Paper, we propose a design of Reversible Sequential circuits using Toffoli gate and Peres gate.Toffoli equivalent circuit and Peres equivalent circuit are proposed in order to attain maximum fault coverage.This paper is organized as follows:Section III presents the proposed Reversible Toffoli and Peres gate.Section IV describes the design of Reversible latches usingToffoli and Peres gate.Section V describes the design of Negative enable Reversible D latch using Toffoli and Peres gate.Section VI presents the design of master slave flipflops using Toffoli and Peres gate.Section VII demonstrates the design of Reversible DET flipflops using Toffoli and Peres gate.Section VIII presents the design of Toffoli equivalent circuit. Section IX describes the design of Peres equivalent circuit. Section X provides the results and conclusion.

II. BACK GROUND

A gate is said to be reversible if only it satisfies the function is bijective. It is mapping from input function to the output function.Few objectives need to satisfy the reversible circuit. There are number of gates; minimize the number of garbage outputs and Synthesis. Various researches had been studied in reversible logic. Feynman gate, New gate and Fredkin gate are used for reversible logic synthesis [3].

Piston and Frank introduced their reversible logic operations [4]. In reversible gates, any Boolean function can be utilized [5].

A. Related work.

Reversible logic is used for many applications like quantum computing. Algorithm is presented to synthesize reversible functions. In reversible functions, the algorithm was positive polarity reed Muller expansion to synthesize the function of Toffoligates [6]. Few problems faced by reversible logic synthesis are fanouts not allowed and feedback from gate output to inputs is not allowed.CMOS implementations of reversible gates are proposed[7].The designs of reversible sequential circuits are introduced to minimize the

quantum cost and delay number of garbage outputs[12]. Various New reversible logic gates are introduced using Boolean expansion [12].

III. PROPOSED REVERSIBLE TOFFOLI AND PERES GATES

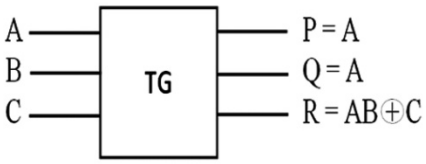

Fig 1 Toffoli gate

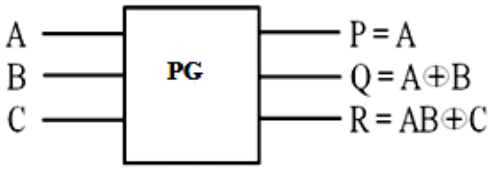

Fig 2 Peres gate

Table 1
Truth Table of Toffoli Gate

Input			Output		
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
1	0	0	1	0	0
1	0	1	1	0	1
1	1	0	1	1	1
1	1	1	1	1	0

Table 2
Truth Table of Peres Gate

Input			Output		
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	1	0
1	0	1	1	1	1
1	1	0	1	0	1
1	1	1	1	0	0

Toffoli gate inverted by Tommaso Toffoli is one of the universal reversible logic gate. A, B, and C are the inputs to Toffoli gate and P, Q, R are the outputs. When two bits are set, it alters the third bit otherwise all remain the same.Peres gate has three inputs and outputs. Each input is mapped to the each output (P=A, Q = A XOR B R = AB XOR C). It has the quantum cost of 4.

IV. DESIGN OF REVERSIBLE LATCHES USING TOFFOLI AND PERES GATE

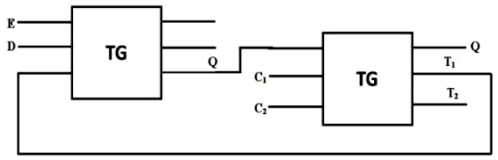

Fig 3 Design of Reversible D latch with Control signals signals Using Toffoli gate

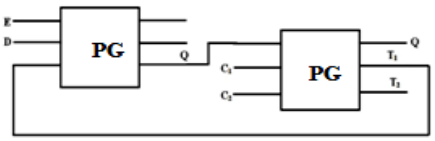

Fig 4 Design of Reversible D latch with Control Using Peres gate

Enable e and d are the input signals to the D latch in Toffoli gate and P, Q, R are the output signals.When the enable is zero the value of d is passed to the output q and r.When the enable is one, the value of d is passed to the output p and q (latch maintains the previous state of q). Latch is tested with control signals C1, and C2, when C1C2 = 01, the latch works as fault free mode in Toffoli and Peres gate. When C1C2 = 00 or 11, the latch works as test mode in Toffoli and Peres gate. In both these modes, there is a shift in the output waveform and latch is tested for various modes of operations.

V. DESIGN OF NEGATIVE ENABLE REVERSIBLE D LATCH USING TOFFOLI AND PERES GATE

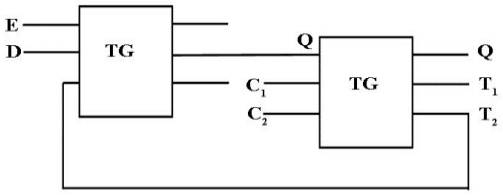

Fig 5 Design of Negative enable Reversible D latch Using Toffoli gate

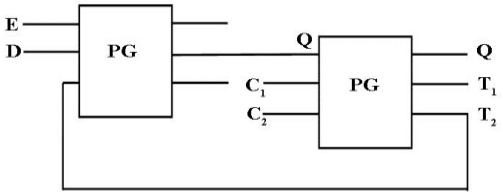

Fig 6 Design of Negative enable Reversible D latch Using Peres gate

Toffoli gate and Peres gate are tested in Negative D latch. The latch is tested with various values of enable, D signals latch works in normal mode or test mode depends upon the value of control signal.

VI. DESIGN OF MASTER SLAVE D FLIPFLOPS USING TOFFOLI AND PERES GATE

In Existing Literature, master slave flipflops are designed using Fredkingate. In this paper, the researchers have proposed the design of master slave D flipflops using Toffoli and Peres gate.

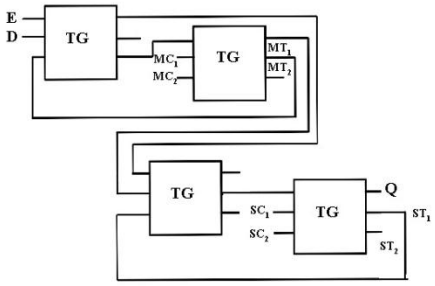

Fig 7 Design of Master slave D flipflops Using Toffoli gate

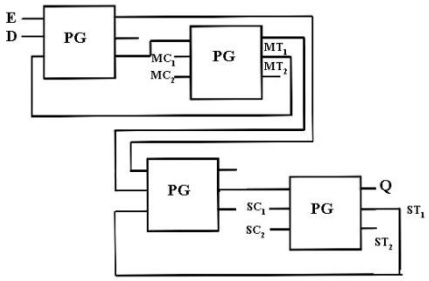

Fig 8 Design of Master slave D flipflops Using Peres gate

Four Peres gate and Toffoli gate are used in master slave D Flip-flops. When enable is zero, the value of d is passed to output Q otherwise it maintains the previous state. mC1, mC2, SC1, SC2 are the control modes for the master latch and slave latch. In normal mode, when enable and d value are one, output of d is passed to Q. In test mode, when all control signals are zero, when enable is one, the value of d is reflected to the output q. Master slave flipflop is tested for two modes of operations.

VII. DESIGN OF DETFLIPFLOPS USING TOFFOLI AND PERES GATE

Four Toffoli gates or Four Peres gates are used two Toffoli or Peres gate acts as master latch, while lower two Toffoli or Peres gate acts as a slave latch. mC1 mC2,sC1,sC2 form the control signals for master latch and slave latch. Latch is tested under the fault free mode and test mode. Toffoli or Peres gate at the end acts as the 2:1 MUX.

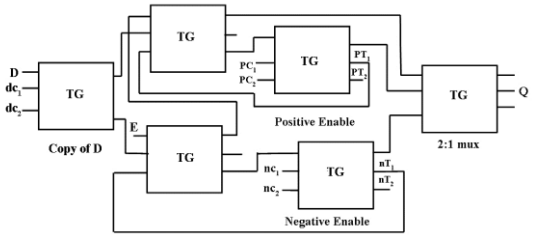

Fig 9 Design of DET flipflops Using Toffoli gate

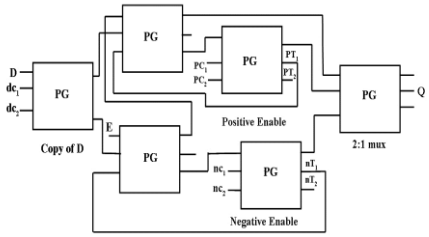

Fig 10 Design of DET flipflops Using Peres gate

DET based Toffoli gate or Peres gate works in two modes operation. In normal mode, the value of nc1 and nc2 is 0 and 1. In test mode, the value of pc1 and pc2 is either 0 or 1. By setting all control signals as zero, when enable is one, the output Q is zero. When enable and d value are one, all control signals as zero, the output Q is one. Latch is tested for various combination of control signals and enable values.

VIII. DESIGN OF TOFFOLI EQUIVALENT CIRCUIT

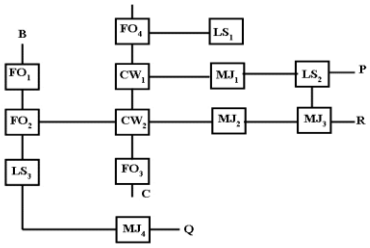

Fig 11 Toffoli equivalent circuit

In the existing work, equivalent circuit is drawn from QCA layout to obtain the maximum fault coverage. In this paper, the researchers propose the equivalent circuit obtained from Boolean expression of Toffoli gate.

Fanout (FO) are the components used in equivalent circuit. Cross wire (CW), L-shaped wire (LS), Majority voter (MJ), are the components used in equivalent circuit. Cross wire (CW) is to combine two variables by AND operation. Fanout (FO) is provided in order to drive the output. L-shaped wire (LS) perform the operation in which signal is passed from in and out. Majority voter (MJ) are provided to perform the AND operation. All components combined together in order to perform the maximum fault coverage.

IX. DESIGN OF PERES EQUIVALENT CIRCUIT.

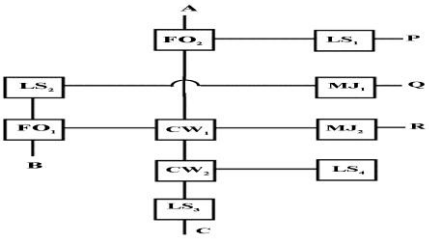

Fig 12 Peres equivalent circuit

In Existing work, MXCQCA and Fredkin gates are drawn in equivalent circuit, from QCA layout. In this paper, the researchers propose the equivalent circuit drawn from Boolean expression of Peres gate, Fan out(FO), L-shaped wire (LS), Majority voter (MJ), Cross wire (CW) are the components used. Crosswire (CW) is to combine two variable by AND operation. Fanout (FO) is provided to drive the output. Fanout is designed if the fault is 1, the output is inverted. L-shaped wire is to pass the signal from in and out, L-shaped wire is designed in such a way if fault is 1, output is inverted. In Majority voter, the output is fault free if the fault is zero, otherwise stuck at fault exists. The output is tested for various combinations of faults in Toffoli gate and Peres gate. Faults are introduced to attain the maximum fault coverage.

X. RESULTS AND DISCUSSION

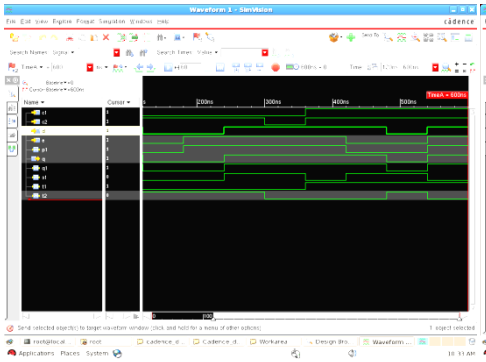

Fig 13 Output waveform of Reversible D latch with Control signals using Toffoli gate

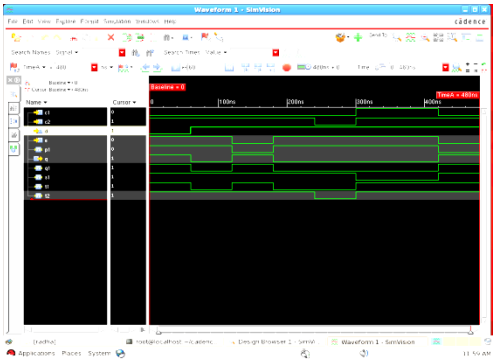

Fig 14 Output waveform of Reversible D latch with Control signals using Peres gate

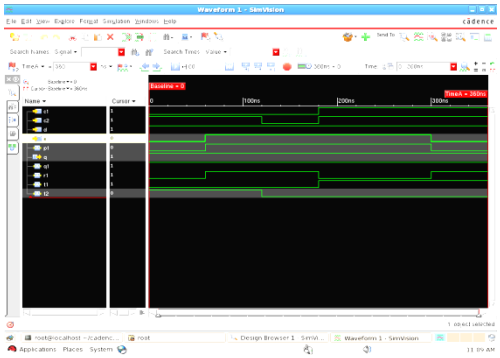

Fig 15 Output waveform of Negative enable D latch using Toffoli gate

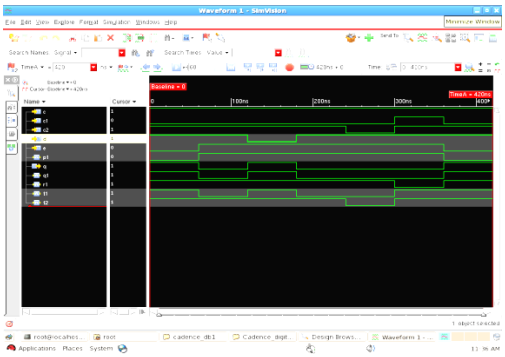

Fig 16 Output waveform of Negative enable D latch using Peres gate

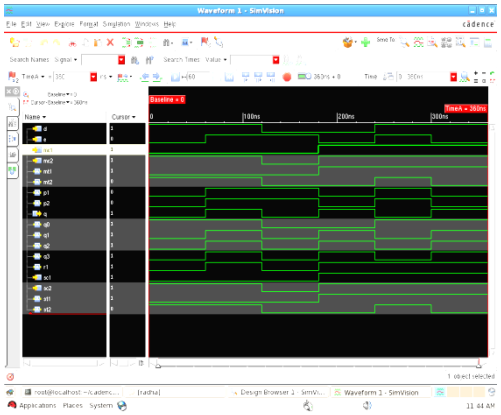

Fig 17 Output waveform of master slave D flipflop using Toffoli gate

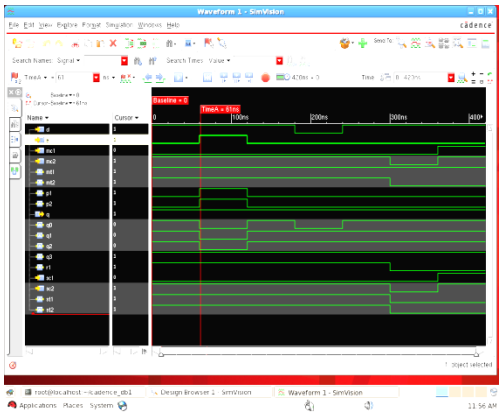

Fig 18 Output waveform of master slave D flipflop using Peres gate

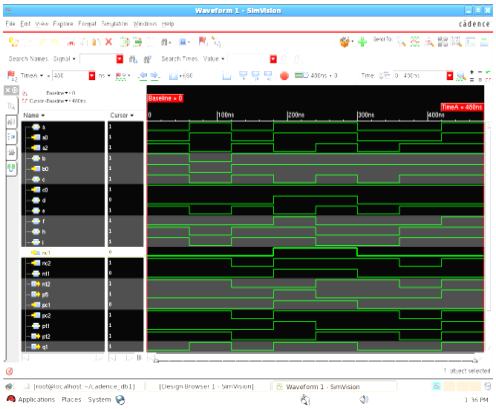

Fig 19 Output waveform of DET using Toffoli gate

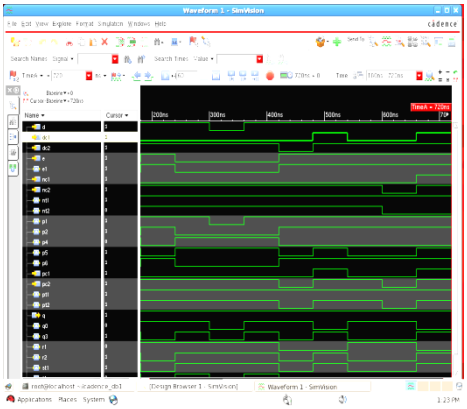

Fig 20 Output waveform of DET using Peres gate

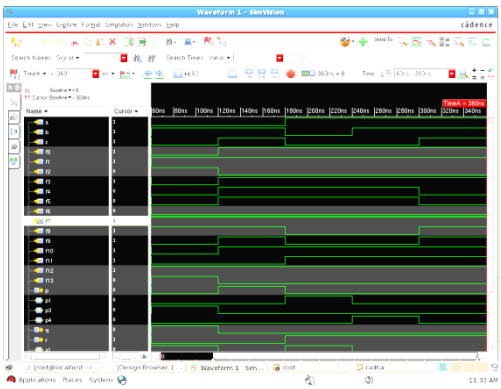

Fig 21 Output waveform of Toffoli equivalent circuit

Fig 22 Output Waveform of Peres equivalent circuit

Table 3 Existing Block and Proposed Block

PARAMETERS	EXISTING SYSTEM (Fredkin)	PROPOSED SYSTEM 1 (Toffoli)	PROPOSED SYSTEM 2 (Peres)
NO OF GATES	2	2	2
AREA	53	33	60
TIMING	88	118	98

Table 4 Existing D Latch Control and Proposed D Latch Control

PARAMETERS	EXISTING SYSTEM (Fredkin)	PROPOSED SYSTEM 1 (Toffoli)	PROPOSED SYSTEM 2 (Peres)
NO OF GATES	4	2	1
AREA	93	33	27
TIMING	268	2	131

Table 5 Existing Negative Enable D Latch and Proposed Negative Enable D Latch

PARAMETERS	EXISTING SYSTEM (Fredkin)	PROPOSED SYSTEM 1 (Toffoli)	PROPOSED SYSTEM 2 (Peres)
NO OF GATES	7	2	5
AREA	160	33	100
TIMING	415	118	378

Table 6 Existing Master Slave D Flipflop and Proposed Master Slave D Flipflop

PARAMETERS	EXISTING SYSTEM (Fredkin)	PROPOSED SYSTEM 1 (Toffoli)	PROPOSED SYSTEM 2 (Peres)
NO OF GATES	4	3	1
AREA	93	67	27
TIMING	266	97	131

Table 7 Existing DET Flipflop and Proposed DET Flipflop

PARAMETERS	EXISTING SYSTEM (Fredkin)	PROPOSED SYSTEM 1 (Toffoli)	PROPOSED SYSTEM 2 (Peres)
NO OF GATES	50	16	18
AREA	888	316	336
TIMING	1220	586	586

Table 8 Existing Equivalent Circuit and Proposed Equivalent Circuit

PARAMETERS	EXISTING SYSTEM (Fredkin)	PROPOSED SYSTEM 1 (Toffoli)	PROPOSED SYSTEM 2 (Peres)
NO OF GATES	9	11	5
AREA	213	193	100
TIMING	372	118	378

In Fig 13 and Fig 14, output is tested for D latch by giving enable signal and analyzed the operation of two modes
In Fig 15 and Fig 16, output is tested for negative enable D latch by giving enable and d values.
In Fig 17 and Fig 18, output describes how Master and slave circuits works by giving enable values and tested for two modes of operation.
In Fig 19 and Fig 20, output is tested for fault free mode and test mode by giving control signal values.
In Fig 21 and Fig 22, output is tested for 13 fault values, and analyzed fault in each component.
Table 3 summarizes the Area, Number of gates and Timing in Existing system is better than proposed system.
Table 4 describes the Area, Number of gates and Timing in Existing system is better than proposed system
Table 5 demonstrates the Area, Number of gates and Timing in Existing system is better than proposed system
Table 6 analyzes the Area, Number of gates and Timing in Existing system is better than proposed system
Table 7 summarizes the Area, Number of gates and Timing in Existing system is better than proposed system
Table 8 describes the Area, Number of gates and Timing in Existing system is better than proposed system

XI. CONCLUSION

This paper describes the design of reversible sequential circuits based on two gates, namely Toffoli gate and Peres gate. We have proposed the equivalent Circuit for Toffoli gate and Peres gate in order to less area, computation time and maximum fault coverage. Area, number of gates and timing are analyzed in these gates. Toffoli gate is better in terms of power consumption compared to fredkin gate. In proposed work, Area, number of gates and timing are reduced compared to existing work. In future work, Ultra low power memory circuits and Digital circuits can be designed.

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