IOSR Journal of VLSI and Signal Processing (IOSR-JVSP)
Volume 4, Issue 2, Ver. IV (Mar-Apr. 2014), PP 17-21
e-ISSN: 2319 – 4200, p-ISSN No. : 2319 – 4197
www.iosrjournals.org

A Literature Review on Design Strategies and Methodologies of Low Power VLSI Circuits

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Abstract: *Low power came in to limelight in the current generation of electronic design. Earlier area and performance and cost were the priority of design engineers overlooking power. However trade off exist between area, performance and power. Overall performance of the circuit is affected by its components. Optimization of the design is accomplished by compromising design issues and components. With the shrinking technology below 90 nm power dissipation and its management has been critical for designer .Importance for optimization has been drawn from extended battery life and lowering package cost. This paper presents a literature review upon the strategies and methodologies in designing low power VLSI circuits.*

Keywords: *VLSI circuits, Low power management, Low power strategies, power dissipation, Power optimization.*

I. Introduction

Digital circuits simplify transistor operation that allows devices to be conceived as switches. Advent of Vacuum tube created a huge impact on electronics industry but had certain hindrances like high power and hundreds of anode voltage. The invention of transistor was a revolutionary step in microelectronics industry consuming few watts of power. This was the foundation stone for low power devices.The integration of numerous functions into a single chip and improvement in the performance of the circuits has led to shrinkage of feature size and resulted in the growth of power per unit area that in turn accompanied a requirement of heat removal and cooling system. Low power is now a principal them in VLSI domain. Three most important factors now days to be optimized are area, power and performance. In the past area, reliability, cost and performance was given utmost importance and power reduction was negligible. Requirement for low power has been increased with remarkable growth in battery powered, complex functional device like PC, wearable devices, mobile phones, implantable medical instruments, multimedia portable devices that demand low power consumption and high speed computation. High power system exacerbates numerous silicon failures due to operation in high temperature.

Rise in 10^{o} C temperature component failure rate doubles. Some of the key design issues in the VLSI industry are thermal and electrical limits determination, impact cost, size, weight, battery size, components, heat sink and system packaging. Excessive power consumption is circumscribing factor in integrating more transistor on a single chip. With lesser power dissipation, less amount of heat is produced in the room, lower is the consumption of electricity and lesser requirement of heat removal equipment and thus impact on global environment is trimmed helping in saving environment. Low power strategies are application specific. Goal of micro powered, battery operated gadgets like cell phones, laptops is to increase the battery life, decreasing weight and cutting off packaging cost. Plastic packaging is used for the circuits with power level of 1-2W. The goal of battery powered, high performance system alike tablets and laptops is reduction in power dissipation to half of total power consumption. For high performance, non battery operated devices achievement of reduced power dissipation with the maintenance of reliability is an objective.

The paper is organized in the following manner. Section II explains major source of power dissipation. Low power design space has been detailed in the section III. Section IV elaborates power minimization techniques while section V and section VI explains CAD methodologies and power management strategies respectively. The paper concludes in section VII.

II. Sources of Power dissipation

Power dissipation is the amount of power that is converted into heat and radiated away from the electrical system. Measurement of power dissipation is in watts. Three major sources of power dissipation in CMOS circuit are:

i) Leakage current: It happens when input(s) and output(s) are stable i.e. not changing.
ii) Short circuit current: It occurs when N-MOS and P-MOS of a CMOS circuit conduct simultaneously allowing current to flow directly from source to ground.
iii) Logic transitions: Nodes in a digital CMOS circuits oscillates between two logic levels ('0' and '1') that in turn charges and discharges the capacitance. This charging and discharging causes the Current to flow from channel resistances of the transistor and phenomenon of power dissipation comes into the picture.

Leakage current fall under the category of static power dissipation while short circuit current and logic transitions are categorized under dynamic power dissipation. Leakage current depends on fabrication technology that includes reverse bias current and subthreshold current in parasitic diodes. The formation of the reverse bias current takes place between drain, source and bulk region in MOS transistors while subthreshold current arises from the inversion charge existing at gate voltage below threshold voltage. If feature size is 1 micrometer then a diode leakage of 1 picoA takes places.

If a dc path is formed between supply rails and ground during input and output transition then short circuit current takes places. Short circuit current is referred to as crow bar current. For an inverter gate, crow bar current is proportional to gain of inverter gate, supply voltage cubic power, subthreshold voltage, operating frequency and as well as on input rise/fall time. During logic transitions capacitive loads are charged and discharged and thus causes power dissipation. In case of absence of load maximum short circuit current is observed that decreases as load is increased.

Short circuit power consumption is less than 15% of dynamic power consumption if rise and fall time of input(s) and output(s) are equivalent. Exploitation of appropriate circuit and device designing techniques can endeavor in bogging down the short circuit and leakage current. However charging and discharging of load capacitance dominates power consumption and is given by equation 1:

$$P = 0.5CV_{dd}^2E(sw)\ f_{clk} \quad (1)$$

Where C is the physical capacitance of the circuit, V_{dd} is the power supply, $f_{clk}$is the clock frequency and E(sw) is the switching activity that describes average number of transitions per 1/ f_{clk} period. Total power is given in the equation 2 as:

$$Ptotal = Pdynamic+ Pstatic + Pshortcircuit \quad (2)$$

III. Low Power Design Space

Low power can be accomplished by reducing one of the following factors:

1. **Voltage**: One of the best method for reduction of power in the circuits. Voltage and power relationship is described by following equation

$$P = \frac{V^2}{R}$$

If V is reduced then power is also reduced. Now consider V as $\frac{V}{2}$ then a power reduction of one fourth is Observed. Its effect is globally on the circuit. Designers often sacrifice increased physical capacitance and data activity for reduced voltage. Although this design space have few disadvantages of lower speed and increased delay as V_{dd} approaches V_t.

2. **Physical capacitance**: Dynamic power dissipation is dependent on switching of physical capacitance. Determination of physical capacitance is arduous task before routing and mapping. Thus with complete information about placement, routing and mapping precision of estimation of capacitance is high. With lesser logic, shorter wires and smaller devices capacitance can be curtailed. An important factor while designing a circuit is interconnects capacitance. Interconnects affect chip area, power dissipation and delay thus during design processing interconnects shall be estimated. Calculation of interconnect capacitance is becomes easy after layout designing. Register sharing, extraction of common sub-functions and information about placement and routing helps in reducing interconnect capacitance.
3. **Logic transitions**: Logic transitions or switching activity influences dynamic power dissipation. In the absence of switching activity power dissipation is zero even on a chip having large number of capacitance. Logic transitions determines switching that has two components namely $f_{clk}$and E(sw). f_{clk} estimates the average period of data arrival while E(sw) determines number of transition each arrival generate.

IV. Power Minimization technique

i) Reducing chip area and capacitances with techniques such as SOI (Silicon on insulator) with partially or fully depleted wells or by scaling CMOS to submicron device size. It is an efficient technique but financially too expensive.

ii) Advanced interconnect substrates like multi chip module MCM. It is highly efficient technique but cost heavily.
iii) Supply voltage scaling: It requires new fabrication technique and support circuits such as DC/DC converters and level converters for operation low voltage environment. It is a cheap technique but handling of signal to noise ratio is critical.
iv) Better design technique: Investment for the reduction of power by employing a better design technique is small and has a very high potential.
v) Appropriate power management strategies.

V. CAD Methodologies

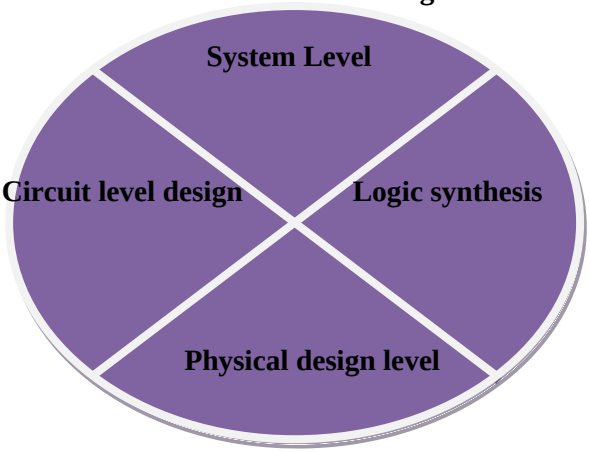

Figure1. Different CAD Methodologies

EDA tools bolster power savings during implementation. Four level of abstraction are logic synthesis level, system level, physical design level and circuit level. This is achieved at above various level of abstraction.

3.1 System level :

At system level design, the hardware modules that are inactive is turned off automatically in order to husband power. A designer can provide minimum supply voltages to modules and implant them with level converters. Thus utilization of this technique will cycle back the energy to save power.

3.2 Logic synthesis:

This level of abstraction fits between register transfer level and netlist of gate specification. Various techniques are employed for the transformation and optimization of RTL description depending upon input target implementation, delay model and objective functions. After the system level, architectural implementation and technological choices are made the switched capacitance of logic determines the power consumption.

3.3 Physical design level:

It fits between netlist gate specification and layout that depends on target design technology, packaging technology and objective functions. Numerous optimization technologies are used for partition, place, resize and route gate. Under zero delay model switching activity of gate is constant during layout optimization therefore to reduce the power decrease the load on high switching activity gate by appropriate netlist portioning, gate placement, gate and wire resizing.

3.4 Circuit level design:

This utilizes adiabatic switching principle where speed is traded for low power. Other techniques that are employed are based on self timed circuits and are based on partial transfer of energy stored on a capacitance to a charge sharing capacitance. DC/DC level converters and energy efficient level converters are required for circuit level design power reduction.

VI. Power Management strategies

Power management strategies play a key role in lowering the power dissipation in digital circuits. Some of the strategies that are discussed in this paper for power reduction are multiple threshold voltage, clock gating, multiple supply voltage, power gating, dynamic voltage scaling and substrate biasing.

6.1 Multiple threshold voltage:

Threshold voltage is an important factor in the reducing of power. This method assist in reducing both dynamic and leakage power. Using different threshold voltage according to the mode of operation the goal is

easily achieved. For leakage power reduction implantation of high threshold voltage is useful. During active mode of operation low threshold voltage is employed for accomplishing low power with high performance. As threshold voltage increases, subthreshold current starts coming down with an increase in propagation delay of the gate. Thus leading to little penalties on speed and area. This is a very useful strategy for reduction of glitches power.

6.2 Multiple supply voltage:

In this technology lower supply voltages and high supply voltage are implanted according to the modes of operation. Non critical path are employed with low supply voltage and higher supply voltage is used for critical paths. Higher supply voltage with critical path helps in attaining performance while lower supply voltage in non critical path helps in accomplishing lower power dissipation. Each tier in a chip is parted into many grids. In these grids higher and lower voltages are fabricated depending upon operational mode. Multiple supply voltage is used in digital signal processors. It helps in achieving latency constraints in critical path. Some of the disadvantages with it are isolation requirement, little increment in the area and difficulty in testing.

6.3 Power gating:

In power gating methodology a sleep transistor is introduced between actual ground and virtual ground when device is turned off in sleep mode in order to cut off leakage path. This technique cut short leakage power without impacting performance. Two types of power gating techniques are fine graining and coarse graining. Design architecture is more than clock gating technique. The disadvantage of this strategy is increased area and delay. Better power efficiency is an advantage of this technique.

6.4 Body biasing:

Body biasing decreases power dissipation by enhancing threshold voltage of individual transistor thereby curtailing leakage current. Two most commonly used techniques are Swapped body biasing (SBB) and dynamic threshold voltage MOS biasing scheme. In SBB propagation delay is short. This technique tends to propose slight penalty on delay and area. RFID, biomedical devices and sensor networks are some example where body biasing is employed.

6.5 Dynamic voltage and frequency scaling:

Most commonly used power management strategy. In this technique clock frequency is reduced causing a reduction in supply voltage. It has the ability to reduce power consumption of CMOS IC like modern computers and laptops.

$$P= cfv^2 + P_{static} \quad (3)$$

Voltage required depends upon the frequency at which it is clocked and thus if frequency is trimmed then voltage can be reduced. By this technique 34% of power is saved. The reduction in frequency increases speed, thus a biggest advantage of this technique. It also offers high performance. It is employed for microprocessors, multimedia interface system and battery powered electronic devices.

6.6 Clock gating:

This technique reduces clock signal resulting in switching power reduction of flip flop. As feature size had shrink clock frequency of IC has increased thus power consumption takes place. Power dissipation is highest due to clock net as it has higher switching activity. In clock gating technique clock is stopped in parts of the circuits. Clock gating occupies large chip area. Some clock gating techniques are AND gate. NOR gate, Latched AND and latched NOR clock gating.

Table 1. Showing comparison between various power management techniques

S.no	Power Management techniques			
	Power reduction technique	Power saving	Delay Penalty	Area
1	Multiple Threshold voltage	Medium	Little	Medium
2	Multiple supply voltage	High	Medium	Medium
3	Power gating	High	Small	Little
4	Body biasing	Medium	Small	Little
5	Dynamic voltage and frequency scaling	High	Small	Medium
6	Clock gating	High	Medium	Large

VII. Conclusion

In this paper various strategies and methodologies for reduction in power has been discussed. This paper has successfully reviewed the CAD methods for power optimization keeping pace with area, delay and performance. This works elaborated the need for low power VLSI circuits and suggested various design techniques currently in practice in microelectronics industry. This paper will help the designers to understand the basics of low power. The major design issues were briefly explained and presented for better clarity to anyone looking to grasp good knowledge about the subject.

Acknowledgment

First author Anuj expresses deep sense of gratitude towards his late grandparents for the shower of blessings. He would take this opportunity to kind heartedly thanks his Mother and Father **Mrs Neeta** and **Mr Avinash Chander** for their continuous encouragement and help. Further he is thankful to his Sister **Swati Misra** and brother- in-law **Ashish Misra** for being such a great support to him. Without these people accomplishment of this paper would have been a dream.

Second author **Divya Khanna** extends gratitude to her grandmother, **Smt. Sarla Khanna**, Father, **Shri Ramesh Khanna**, Mother **Mrs. Vandana Khanna** and brother **Amit Khanna** who never ceased in helping until the paper was structured.

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