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Design of an accurate NoC for Multiprocessor SoC

Archana H R[1], Dr. K S Vasundara Patel[2]
[1]*Assistant Professor, Dept of ECE, BMSCE, Bangalore*
[2]*Assistant Professor, Dept of ECE, BMSCE, Bangalore*

Abstract: *Any integrated system consists of a host processor, memory and peripheral elements which are interconnected through a bus interface. The synchronization of these basic blocks with internal and external environment is achieved by means of an I/O buffer. The work is intended to develop a self-reconfigurable channel data buffering form and circuit design for network-on-chips (NoCs). The design is optimized for power efficiency and data throughput, from system to circuit level. The adaptive flow control enables to control the congestion by reconfiguration of channel through adaptive techniques. Here we design a NoC on a SoC to meet the electrical specifications dictated by industry standards.*
Keywords: *NoC, SoC, NoC architectures, switch fabric, multicore*

I. Introduction

In order to meet the intensive computation applications and the need for low power, high performance requirements, it is necessary to increase the number of computing resources on a single chip. By the addition of various resources such as CPU, DSPs, ASICs etc to build a System on Chip (SoC) it is necessary to focus on the interconnections between these elements. Most of the System-on-Chip applications has a shared bus interconnection which needs an arbitration logic to serialize several bus access requests, to communicate with each integrated processing unit because of its low-cost and simple control characteristics. Such shared bus interconnection has a limitation in its scalability because only one master at a time can utilize the bus which means all the bus accesses should be serialized by the arbitrator. Therefore, in such an environment where the number of bus requesters is large and their required bandwidth for interconnection is more than the current bus, a different interconnection method should be designed.

II. Layout Of General Soc

Any integrated system consists of a host processor, memory and peripheral elements which are interconnected through a bus interface as shown in fig1. The synchronization of these basic blocks with internal and external environment is achieved by means of an I/O buffer. The work presents a self-reconfigurable channel data buffering scheme and circuit design for next-generation network-on-chips (NoCs). The design is optimized for power efficiency and data throughput, from system to circuit level. During network congestion, the buffering scheme realizes adaptive flow control by reconfiguring the channel buffers for online data storage. Here we design a NoC on a SoC to meet the electrical specifications dictated by industry standards.

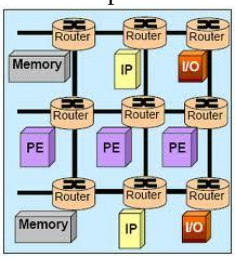

Fig1: Network connecting the resources

III. Drawbacks Of Conventional Soc Architectures

1) Under various large-scale heavy-traffic conditions, conventional NoC channel buffering schemes tend to be inefficient.
2) Traditional designs utilize software-based flow control algorithms, such as credit-based flow control or on/off flow control, to prevent the loss of data during congestion.
However, such algorithms require considerable computation and communication overhead, due to continuous exchange of control signals. The transmission of these signals leads to significant power increase and throughput reduction.

Network on Chip (NoC) concepts have evolved to provide an interesting alternative to more traditional intrachip communication architectures (e.g. shared busses) for the design of complex Systems on Chip (SoCs). A considerable number of NoC proposals are available, focusing on different sets of optimization aspects, related to specific classes of applications. Each such application employs a NoC as part of its underlying implementation infrastructure. Many of the mentioned optimization aspects target results such as Quality of Service (QoS) achievement and/or power consumption reduction. On the other hand, the use of NoCs brings about the solution of new design problems, such as the choice of synchronization method to employ between NoC routers and application modules mapping.[1]

PROPOSED BLOCK DIAGRAM OF NOC IN A SOC

Network on Chip (NoC) concepts have evolved to provide an interesting alternative to more traditional intrachip communication architectures (e.g. shared busses) for the design of complex Systems on Chip (SoCs). A considerable number of NoC proposals are available, focusing on different sets of optimization aspects, related to specific classes of applications. Each such application employs a NoC as part of its underlying implementation infrastructure.

Any NoC network or proposal could comprise of the following basic entities shown in fig2:

- Resources/nodes
- Links/wires
- Switches/routers
- Switching algorithm

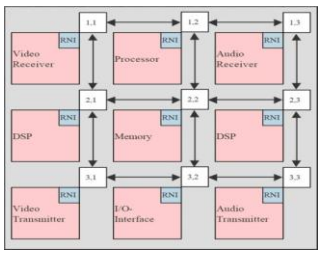

Fig2:Resources in SoC with routing

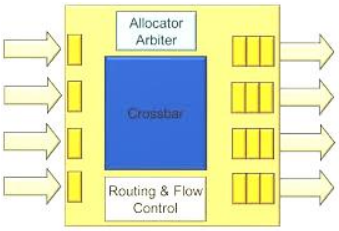

Fig3: Crossbar to be designed for routing the resources

The switches and resources can be connected through links to form a switching and live on-chip interconnection network called NoC. The sending resource can use different paths through the switches to send its messages to the desired destination. The crossbar switch designed as shown in fig3 helps in routing the traffic effectively. These messages can be considered as traffic between this sender/target pair[2]. Chip-level multiprocessors (CMPs) feature up to a hundred discrete cores, and with increasing levels of integration, CMPs with hundreds of cores, cache tiles, and specialized accelerators are anticipated in the near future[3]. Power and wire design constraints are forcing the adoption of new design methodologies for system-on-chip (SoC), namely, those that incorporate modularity and explicit parallelism. Communication-centric interconnect fabrics are characterized by different trade-offs with regard to latency, throughput, energy dissipation, and silicon area requirements. [4].Data transmission and on-chip global communication schemes have undergone a revolutionary paradigm shift due to the development of modular and scalable packet-switched network-on-chips (NoCs) [5]. A NOC platform, consisting of architecture and design methodology, which scales from a few dozens to several hundred or even thousands of resources is designed. A resource may be a processor core, a DSP core, an FPGA block, a dedicated HW block, a mixed signal block, or a memory block of any kind such as RAM, ROM or CAM.[6] When compared to traditional data buffering designs that employ dedicated wires for each signal, NoCs establish a structured and layered communication network that is more efficient, reliable, and scalable. On-chip interconnects carrying signals between different blocks will be the bottleneck for system performance and reliability. To tackle this problem, an on chip communication infrastructure based on a network-on-chip architecture with a hybrid mechanism to transfer data among IP cores by taking advantages of both wired

and wireless communications is necessary [9]. Different Network-on-Chip architectures like mesh, torus, and hypercube-topologies can be generated, based on this switch. The proposed framework can be used for exploration and optimization of Network-on-Chip architectures, by comparing Network-on-Chip architectures with different topologies and routing algorithms [8]. Multicore platforms are emerging trends in the design of System-on-Chips (SoCs).

Interconnect fabrics for these multicore SoCs play a crucial role in achieving the target performance. The Network-on-Chip (NoC) paradigm has been proposed as a promising solution for designing the interconnect fabric of multicore SoCs. But the performance requirements of NoC infrastructures in future technology nodes cannot be met by relying only on material innovation with traditional scaling. The continuing demand for low-power and high-speed interconnects with technology scaling necessitates looking beyond the conventional planar metal/dielectric-based interconnect infrastructures. Among different possible alternatives, the on-chip wireless communication network is envisioned as a revolutionary methodology, capable of bringing significant performance gains for multicore SoCs. Wireless NoCs (WiNoCs) also can be designed by using miniaturized on-chip antennas as an enabling technology. The design methodologies and technology for scalable WiNoC architectures to evaluate their performance is necessary[10]. Notion of a network on a chip as a programmable asynchronous VLSI architecture for fast and efficient simulation of wireless networks is to be taken care [11] while designing.

A mathematical model for on-chip routers is obtained and which can be utilized for NoC performance analysis. This model can be used not only to obtain fast and accurate performance estimates and also to guide the NoC design process within an optimization loop [12]. However, the development of advanced integrated architectures, such as system-on-chip and chip-level multiprocessors, has placed considerable challenges on the NoC designs [14].

IV. Objective Of The Research Work

A. Propose a new design for crossbar switching fabric with optimized routing with all the resources.
B. Another objective of this work is to study the NoC architectures through AXI4 and compare with the AXI3 protocol.
C. Verification and validation of the design through simulation.

V. Possible Outcomes Of The Research Work

A. To achieve optimization in delay, with lower power dissipation.
B. To develop a consistent evaluation methodology to compare the performance characteristics of a variety of NoC architectures (mesh, torus, star etc)
C. Schedule the routing between the communicating resources depending on the traffic.

VI. Tools Used

1) Questasim (Front End Designing)
2) Perl And Toolkit (For Automation)

References

[1] Everton Carara, Ney Calazans, Fernando Moraes; Journal Integrated Circuits and Systems 2008; v.3 , "A New Router Architecture for High-Performance Intrachip Network"
[2] Sheraz Anjum, Ehsan Ullah Munir,Waqas Anwar and Nadeem Javaid, Research Journal of Applied Sciences, Engineering and Technology 5(2): 353-356, 2013, "Object Oriented Model for Evaluation of On-Chip Networks"
[3] Boris Grot, Joel Hestness, Stephen W. Keckler, Onur Mutlu. Computer Architecture (ISCA), 2011 38th Annual International, Symposium on Publication Year: 2011, "Kilo-NOC: A Heterogeneous Network-on-Chip Architecture for Scalability and Service Guarantees"
[4] Partha Pratim Pande, Cristian Grecu, Michael Jones, André Ivanov, Resve Saleh, August 2005 (vol. 54 no. 8) pp. 1025-1040 , "Performance Evaluation and Design Trade-Offs for Network-on-Chip Interconnect Architectures"
[5] Wan-Ting Su ; Comput. Sci. & Inf. Eng., Nat. Chung Cheng Univ., Chiayi, Taiwan ; Jih-Sheng Shen ; Pao-Ann Hsiung, Automation Conference (ASP-DAC), 2011 , "Network on chip router design with buffer stealing"
[6] Kumar, S. ; Lab. of Electron. & Comput. Syst., R. Inst. of Technol., Stockholm, Sweden ; Jantsch, A. ; Soininen, J.-P. ,IEEE Computer Society Ann Published date 24 April 2014ual Symposium on VLSI,2002, " A network on chip architecture and design methodology"
[7] Kangmin Lee ; Dept. of Electr. Eng. & Comput. Sci., Korea Adv. Inst. of Sci. & Technol., Daejeon, South Korea ; Se-Joong Lee ; Hoi-Jun Yoo, IEEE Journals & Magazines Transactions Feb 2006, "Low power network on chip for high performance SOC design"
[8] Schonwald, T. ; FZI (Forschungszentrum Inf.), Karlsruhe, Germany ; Zimmermann, J. ; Bringmann, O. ; Rosenstiel, W. , 12th Euromicro Conference on Digital System Design 2009,"Network on chip architecture exploration framework"
[9] Chifeng Wang ; Dept. of Electr. Eng. & Comput. Sci., Univ. of California, Irvine, Irvine, CA, USA ; Wen-Hsiang Hu ; Bagherzadeh, ,.IEEE Conference Feb2011, A wireless network on chip design for multicore platforms"
[10] Ganguly, A. ; Dept. of Comput. Eng., Rochester Inst. of Technol., Rochester, NY, USA ; Chang, K. ; Deb, S. ; Pande, P.P.IEEE2011, "Scalable Hybrid Wireless Network-on-Chip Architectures for Multicore Systems"

[11] Manohar, R. ; Cornell Univ., Ithaca, NY, USA ; Kelly, C., IV,IEEE2001, "Network on a chip: Modelling wireless networks with asynchronous VLSI"
[12] Ogras, U.Y. ; Strategic CAD Labs., Intel Corp., Hillsboro, OR, USA; Bogdan, P. ; Marculescu, R.IEEE-2010, "An analytical approach for Network on Chip performance analysis"
[13] Rajdeep Bondade, Student Member, IEEE, and Dongsheng Ma, Senior Member, IEEE 2011, "Self reconfigurable channel data buffering scheme and circuit design for adaptive flow control in power efficient network on chip".
[14] Rana, Vincenzo; Atienza, David; Santambrogio, Marco D; Sciuto, Donatella; De Micheli, Giovanni, 16th IFIP/IEEE International Conference on Very Large Scale Integration, Rhodes, Greece, October 13-15, 2008, "A reconfigurable network on chip architecture for optimal multiprocessor SoC communication*"*
[15] Karam S. Chatha, Member, Krishnan Srinivasan, and Goran Konjevod, IEEE 2010, "Automated Techniques for Synthesis of Application-Specific Network-on-Chip Architectures"
[16] Senthilkuamr et al., International Journal of Advanced Research in Computer Science and Software Engineering 2 (9), September-2012, pp. 103-108, "A Heterogeneous Network-on-Chip Architecture for Scalability and Service Guarantees"