IOSR Journal of VLSI and Signal Processing (IOSR-JVSP)
Volume 4, Issue 3, Ver. III (May-Jun. 2014), PP 22-29
e-ISSN: 2319 – 4200, p-ISSN No. : 2319 – 4197
www.iosrjournals.org

Implementation of MSIC-TPG in BIST Scheme

Prasuna G .D, K .V Rajendra Prasad
(Ece, Sree Vidyanikethan College Of Engineering, India)
(Ece, Sree Vidyanikethan College Of Engineering, India)

Abstract : *This paper introduces a test pattern generator (TPG) in order to use in built-in self-test(BIST). MSIC TPG generates multiple single input change (MSIC) vectors in a pattern, i.e., each vector applied to a scan chain is an SIC vector. With the help of reconfigurable Johnson counter and a scalable SIC counter its easy to generate a class of minimum transition sequences. The proposed TPG is flexible to test-per-scan schemes. A theory is developed to represent and analyze the sequences and to extract a class of MSIC sequences. Analysis results show that the produced MSIC sequences have the favorable features of uniform distribution, minimum transitions, and low input transition density. The Performances of the designed MSIC TPG and the circuit under test are evaluated. Simulation results shows that it can save delay time and power. It also achieves the target fault coverage without increasing the test length.*
Keywords: *Built-in self-test (BIST), minimum delay, multiple single-input Change (MSIC), test pattern generator (TPG).*

I. INTRODUCTION

BUILT-IN SELF-TEST (BIST) techniques can effectively reduce the difficulty and complexity of VLSI testing, by introducing on-chip test hardware into the circuit-under-test (CUT). In conventional BIST architectures, the linear feedback shift register (LFSR) is commonly used in the test pattern generators (TPGs) and output response analyzers. A major drawback of these architectures is that the pseudorandom patterns generated by the LFSR lead to significantly high switching activities in the CUT [1], which can cause excessive power dissipation. They can also damage the circuit and reduce product yield and lifetime [2], [3]. In addition, the LFSR usually needs to generate very long pseudorandom sequences in order to achieve the target fault coverage in nanometer technology.

A. Prior Work

Several advanced BIST techniques have been studied and applied. The first class is the LFSR tuning. Girard *et al.* analyzed the impact of an LFSR's polynomial and seed selection on the CUT's switching activity, and proposed a method to select the LFSR seed for energy reduction [4]. Manuscript received July 18, 2011; revised April 5, 2012; accepted April 12, 2012. Date of publication May 14, 2012; date of current version March 18, 2013. This work was supported in part by the Fundamental Research Funds for the Central Universities under Grant xjj20100053 and the National Natural Science Foundation of China under Grant 61006033. The authors are with the School of Electronic and Information Engineering, Xi'an Jiao tong University, Xi'an 710049, China (e-mail: zhangguohe@mail.xjtu.edu.cn). Digital Object Identifier 10.1109/TVLSI.2012.2195689 the second class is low-power TPGs. One approach is to design low-transition TPGs. Wang and Gupta used two LFSRs of different speeds to control those inputs that have elevated transition densities [5]. Corno *et al.* provided a low power TPG based on the cellular automata to reduce the test power in combinational circuits [6]. Another approach focuses on modifying LFSRs. The scheme in [7] reduces the power in the CUT in general and clock tree in particular. In [8], a low-power BIST for data path architecture is proposed, which is circuit dependent. However, this dependency implies that non detecting subsequences must be determined for each circuit test sequence. Bonhomie *et al.* [9] used a clock gating technique where two non overlapping clocks control the odd and even scan cells of the scan chain so that the shift power dissipation is reduced by a factor of two. The ring generator [10] can generate a single-input change (SIC) sequence which can effectively reduce test power. The third approach aims to reduce the dynamic power dissipation during scan shift through gating of the outputs of a portion of the scan cells. Bhunia *et al.* [11] inserted blocking logic into the stimulus path of the scan flip-flops to prevent the propagation of the scan ripple effect to logic gates. The need for transistors insertion, however, makes it difficult to use with standard cell libraries that do not have power-gated cells. In [12], the efficient selection of the most suitable subset of scan cells for gating along with their gating values is studied. The third class makes use of the prevention of pseudorandom patterns that do not have new fault detecting abilities [13]–[15]. These architectures apply the minimum number of test vectors required to attain the target fault coverage and therefore reduce the power. However, these methods have high area overhead, need to be customized for the CUT, and start with a specific seed. Gerstendorfer *et al.* also proposed to filter out non

detecting patterns using gate-based blocking logics [16], which, however, add significant delay in the signal Propagation path from the scan flip-flop to logic. Several low-power approaches have also been proposed for scan-based BIST. The architecture in [17] modifies scan-path structures, and lets the CUT inputs remain unchanged during a shift operation. Using multiple scan chains with many scan enable (SE) inputs to activate one scan chain at a time, the TPG proposed in [18] can reduce average power consumption during scan-based tests and the peak power in the CUT. In [19], a pseudorandom BIST scheme was proposed to reduce switching activities in scan chains. Other approaches include LT-LFSR [20], a low-transition random TPG [21], and the weighted LFSR [22]. The TPG in [20] can reduce the transitions in the scan inputs by assigning the same 1063-8210/$31.00 © 2012 IEEE LIANG *et al.*: TEST PATTERNS OF MULTIPLE SIC VECTORS 615 value to most neighboring bits in the scan chain. In [21], power reduction is achieved by increasing the correlation between consecutive test patterns. The weighted LFSR in [22] decreases energy consumption and increases fault coverage by adding weights to tune the pseudorandom vectors for various probabilities.

B. Contribution and Paper Organization

This paper presents the theory and application of a class of minimum transition sequences. The proposed method generates SIC sequences, and converts them to low transition sequences for each scan chain. This can decrease the switching activity in scan cells during scan-in shifting. The advantages of the proposed sequence can be summarized as follows.

1) *Minimum transitions:* In the proposed pattern, each generated vector applied to each scan chain is an SIC Vector, which can minimize the input transition and reduce test power.

2) *Uniqueness of patterns:* The proposed sequence does not contain any repeated patterns, and the number of distinct patterns in a sequence can meet the requirement of the target fault coverage for the CUT.

3) *Uniform distribution of patterns:* The conventional algorithms of modifying the test vectors generated by the LFSR use extra hardware to get more correlated test vectors with a low number of transitions. However, they may reduce the randomness in the patterns, which may result in lower fault coverage and higher test time [23]. It is proved in this paper that our multiple SIC (MSIC) sequence is nearly uniformly distributed.

4) *Low hardware overhead consumed by extra TPGs:* The linear relations are selected with consecutive vectors or within a pattern, which has the benefit of generating a sequence with a sequential decompressor. Hence, the Proposed TPG can be easily implemented by hardware. The rest of this paper is organized as follows. In Section II, the proposed MSIC-TPG scheme is presented. In Section III, the properties of the MSIC sequences are analyzed. In Section IV,the implementation of MSIC TPG in BIST Architecture is shown. In Section V,the performance analysis is presented. Conclusions are given in Section VI.

II. PROPOSED MSIC-TPG SCHEME

This section develops a TPG scheme that can convert an SIC vector to unique low transition vectors for multiple scan chains. First, the SIC vector is decompressed to its multiple code words. Meanwhile, the generated code words will bit-XOR with a same seed vector in turn. Hence, a test pattern with similar test vectors will be applied to all scan chains. The proposed MSIC-TPG consists of an SIC generator, a seed generator, an XOR gate network, and a clock and control block.

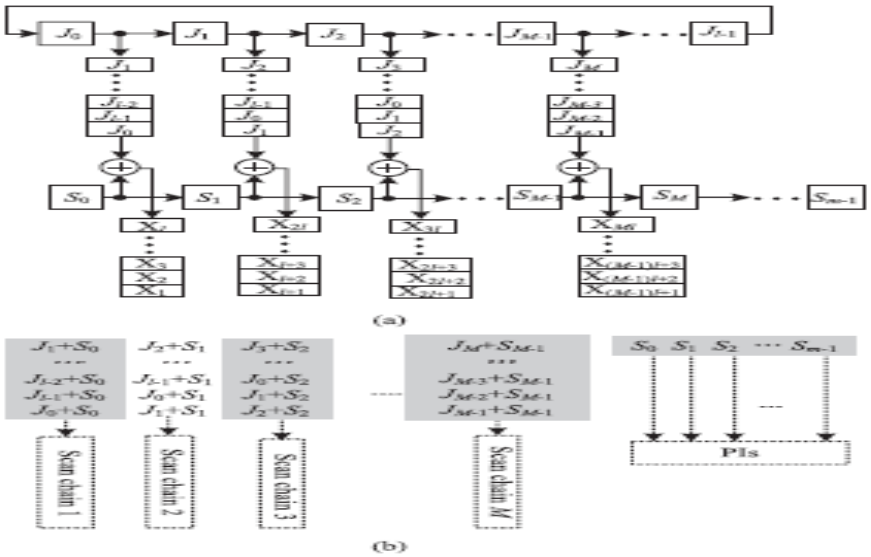


Fig. 1. (a) Symbolic simulation of an MSIC pattern for scan chains
(b) Symbolic representation of an MSIC pattern.

A. Test Pattern Generation Method

Assume there are *m* primary inputs (PIs) and *M* scan chains in a full scan design, and each scan chain has l scan cells. Fig. 1(a) shows the symbolic simulation for one generated pattern. The vector generated by an *m*-bit LFSR with the primitive polynomial can be expressed as $S(t) = S0(t)S1(t)S2(t), \ldots, Sm-1(t)$ (hereinafter referred to as the seed), and the vector generated by an *l*-bit Johnson counter can be expressed as $J(t) = J0(t)J1(t)J2(t), \ldots, Jl-1(t)$.In the first clock cycle, $J = J0\ J1\ J2, \ldots, Jl-1$ will bit-XOR with $S = S0S1S2, \ldots, SM-1$, and the results $X1Xl+1X2l+1, \ldots, X(M-1)l+1$ will be shifted into *M* scan chains, respectively. In the second clock cycle, $J = J0\ J1\ J2, \ldots, Jl-1$ will be circularly shifted as $J = Jl-1\ J0\ J1, \ldots, Jl-2$, which will also bit-XOR with the seed $S = S0S1S2, \ldots, SM-1$. The resulting $X2Xl+2X2l+2, \ldots, X(M-1)l+2$ will be shifted into *M* scan chains, respectively. After *l* clocks, each scan chain will be fully loaded with a unique Johnson codeword, and seed $S0S1S2, \ldots, Sm-1$ will be applied to *m* PIs. Since the circular Johnson counter can generate *l* unique Johnson code words through circular shifting a Johnson vector, the circular Johnson counter and XOR gates in Fig. 1 actually constitute a linear sequential decompressor.

***B. Reconfigurable Johnson Counter*:**

According to the different scenarios of scan length, this paper develops two kinds of SIC generators to generate Johnson vectors and Johnson code words, i.e., the reconfigurable Johnson counter and the scalable SIC counter.

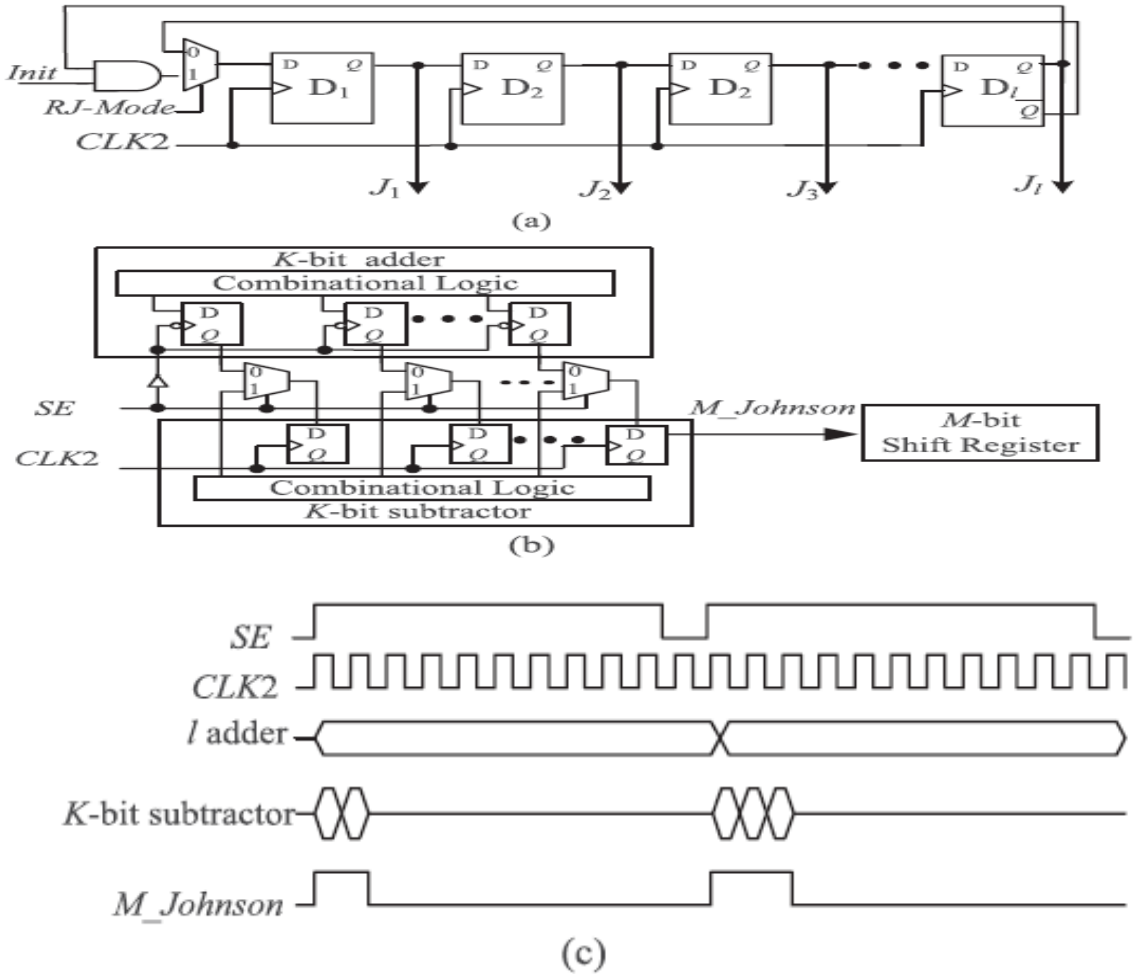


Fig. 2. SIC generators. (a) Recnfigurable Johnson counter. (b) Scalable SIC Counter. (c) Waveforms of the scalable SIC counter.

For a short scan length, we develop a reconfigurable Johnson counter to generate an SIC sequence in time domain. As shown in Fig. 2(a), it can operate in three modes.

1) *Initialization:* When RJ_Mode is set to 1 and *Init* is set to logic 0, the reconfigurable Johnson counter will be

initialized to all zero states by clocking CLK2 more than *l* times.

2) *Circular shift register mode:* When RJ_Mode and Init are set to logic 1, each stage of the Johnson counter will output a Johnson codeword by clocking CLK2 *l* times.
3) *Normal mode:* When RJ_Mode is set to logic 0, the reconfigurable Johnson counter will generate 2*l* unique SIC

vectors by Clocking CLK2 2*l* times.

C. Scalable SIC Counter

When the maximal scan chain length *l* is much larger than the scan chain number *M*, we develop an SIC counter named the "scalable SIC counter." As shown in Fig. 2(b), it contains a *k*-bit adder clocked by the rising *SE* signal, a *k*-bit subtractor clocked by test clock CLK2, an *M*-bit shift register clocked by test clock CLK2, and *k* multiplexers. The value of *k* is the integer of log2*(l − M)*. The waveforms of the scalable SIC counter are shown in Fig. 2(c). The *k*-bit adder is clocked by the falling *SE* signal, and generates a new count that is the number of 1s (0s) to fill into the shift register. As shown in Fig. 2(b), it can operate in three modes.

1) If *SE* = 0, the count from the adder is stored to the *k*-bit subtractor. During *SE* = 1, the contents of the *k*-bit subtractor will be decreased from the stored count to all zeros gradually.
2) If *SE* = 1 and the contents of the *k*-bit subtractor are not all zeros, *M*-Johnson will be kept at logic 1 (0).
3) Otherwise, it will be kept at logic 0 (1). Thus, the needed 1s (0s) will be shifted into the *M*-bit shift register by Clocking CLK2 *l* times, and unique Johnson code words will be applied into different scan chains.

For example, after full-scan design, ISCAS'89 s13207 has 10 scan chains whose maximum scan length is 64. To implement a scalable SIC counter as shown in Fig. 2(b), it only needs 6 D-type flip-flops (DFFs) for the adder, 6 DFFs for the subtractor, 10 DFFs for a 10-bit shift register for 10 scan chains, 6 multiplexers, and additional 19 combinational logic gates. The equivalent gates are 204 in total. For a 64-bit Johnson counter, it needs 64 DFFs, which are about 428 equivalent gates. The overhead of a MSIC-TPG can thus be effectively decreased by using the scalable SIC counter. Generally, the gate overhead of a MSIC-TPG can be estimated by the number of DFFs (*N*DFF) used *N*DFF = $m + M + 2\log 2l = (m + M)\ 1 + 2\log 2lm + M$_(1) where *m*, *M*, and *l* are the seed number, scan chain number, and the maximum scan length, respectively. If *l* is doubled, the number of DFFs is only increased by 2*/(m + M)* times. If $2i-1 < l < 2i$ (*i* is a natural number), the number of DFFs does not vary with the CUTs' sizes.

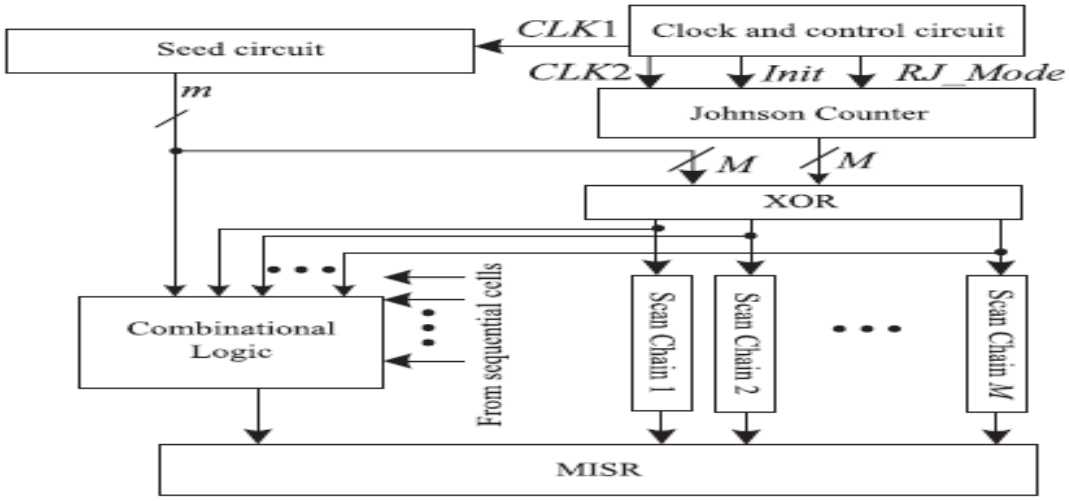
D. MSIC-TPGs for Test-per-Scan Schemes

The MSIC-TPG for test-per-scan schemes is illustrated in Fig.3. The stage of the SIC generator is the same as the Maximum scan length, and the width of a seed generator is LIANG *et al*.: TEST PATTERNS OF MULTIPLE SIC VECTORS 617 Fig. 3. MSIC-TPGs for test-per-scan schemes. Not smaller than the scan chain number. The inputs of the XOR gates come from the seed generator and the SIC counter, and their outputs are applied to *M* scan chains, respectively. The outputs of the seed generator and XOR gates are applied to the CUT's PIs, respectively. The test procedure is as follows.

1) The seed circuit generates a new seed by clocking CLK1 one time.
2) RJ_Mode is set to "0". The reconfigurable Johnson counter will operate in the Johnson counter mode and generate a Johnson vector by clocking CLK2 one time.
3) After a new Johnson vector is generated, RJ_Mode and Init are set to 1. The reconfigurable Johnson counter Operates as a circular shift register, and generates *l* code words by clocking CLK2 *l* times. Then, a capture operation is

inserted.

4) Repeat 2–3 until 2*l* Johnson vectors are generated.
5) Repeat 1–4 until the expected fault coverage or test length is achieved.



Fig;3 MSIC-TPG Test per Scan Scheme

III. PROPERTIES OF MSIC SEQUENCES

A. Switching Activity Reduction

For test-per-clock schemes, *M* segments of the CUT's primary inputs are applied with *M* unique SIC vectors. The mean input transition density of the CUT is close to 1/*l*. For test-per-scan schemes, the CUT's PIs are kept unchanged during 2*l*2 shifting-in clock cycles, and the transitions of a Johnson codeword are not greater than 2. Therefore, the mean input transition density of the CUT during scan-in operations is less than 2/*l*.

B. Uniform Distribution of MSIC Patterns

If test patterns are not uniformly distributed, there might be some inputs that are assigned the same values in most test patterns. Hence, faults that can only be detected by patterns that are not generated may escape, leading to low fault coverage.

C. Relationship between Test Length and Fault Coverage

The test length of conventional LFSR methods is related to the initial test vector. In other words, the number of patterns to hit the target fault coverage depends on the initial vector in conventional LFSR TPGs. For MSIC sequences, the numbers of patterns to hit the target fault coverage with different initial seeds are nearly the same, as shown by curves marked with "Best case, MSIC" and "Worst case, MSIC." Also, the rate of growth of the fault coverage with the MSIC sequence is very close to that with the LFSR in the best case.

IV. IMPLEMENT OF MSIC TPG IN BIST ARCHITECTURE

The MSCI TPG which generates msic vectors i.e., patterns that should be given as input to the CUT as well as the reference circuit. The patterns should be unique and uniformly distributed among them. The circuit which intakes the vectors of TPG it generates the output responses and that responses are equal to the reference circuit output responses. The resultant of both responses gets compared to each other at comparator circuit i.e., TEST RESPONSE ANALYZER (TRA) and delivers the result. Like this, the testing of CUT'S are easily done with the help Of TPG'S.One more factor MISR'S plays a major role in the BIST ARCHITECTURE which stores the output responses of CUT and Reference Circuit. A typical BIST architecture which is shown in fig (4) consists of Test Pattern Generator (TPG) usually implemented as a LFSR, Test Response Analyzer (TRA), Multiple Input Signature Register (MISR), CUT and BIST control unit. SIC technique is a low power approach which greatly decreases the transitions of inputs to reduce the internal switching activities. In SIC the number of bits in sequence will change only one but we need more vectors requires to test CUT, which needs more time for testing. MSIC has multiple chain vectors, each chain will change one bit we need minimum number of vectors requires in the CUT testing, by using this method we can improve the power dissipation, speed, yield and life time.

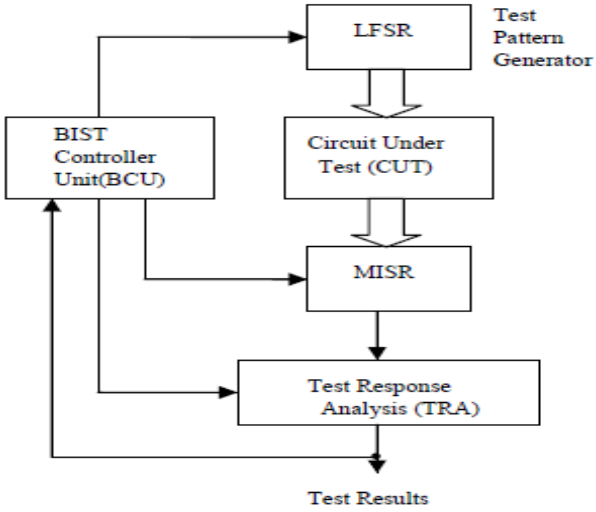


Fig 4.) BIST ARCHITECTURE

The blocks of BIST ARCHITECTURE is explain as follows:

- TPG: It generates the test patterns for the CUT. It is dedicated circuit or a microprocessor. The patterns may be generated in pseudorandom or deterministically.
- MISR: It is designed for signature analysis, which is a technique for data compression. MISR efficiently map different input streams to different signatures.
- TRA: It will check the output of MISR & verify with the input of LFSR & give the result as error or not.
- BIST Control Unit: Control unit is used to control all the operations. Mainly control unit will do configuration of CUT in test mode/Normal mode, feed seed value to LFSR, Control MISR & TRA. It will generate interrupt if an error occurs.
- CUT: It is the portion of the circuit tested in BIST mode. It can be sequential, combinational or a memory. Their Primary Input (PI) and Primary output (P0) delimit it.

Multipliers are widely used in DSP, DIP applications for convolution for filters, correlation and filter banks for multi- rate signal processing. Let's consider Array Multiplier as CUT in order to test with the MSIC-TPG scheme. An array multiplier a multiplication method in which an array of identical cells generates new partial product and accumulation of it at the same time. We can use pipelines at each level result from the adder can be latched at each level and used as input for next level adder circuit. The delay is logarithmically proportional to the bit size of multiplicand and multiplier if we use the high speed array multiplier circuit. Large number of logic gates required to design an array multiplier is the only disadvantage of array multiplier.

V1. PERFORMANCE ANALYSIS

The performance simulations of MSIC TPG along with CUT testing are carried out with MODELSIM ALTERA 6.5e Simulator. Synthesis has been carried out with XILINK ISE. The test frequency is 14.96 MHz, the power supply voltage is 1.1 V and delay of 66.82ns.The number of multiplier required is 1, registers and flip flops are 104, comparators 1,exor gates 993 and the number of IO's is 13. The CUT 32 bit array multiplier is successfully been tested by MSIC TPG of BIST Architecture. Whereas with LFSR TPG the accurate testing of CUT will not be occur because of high switching activities.

VI. FIGURES

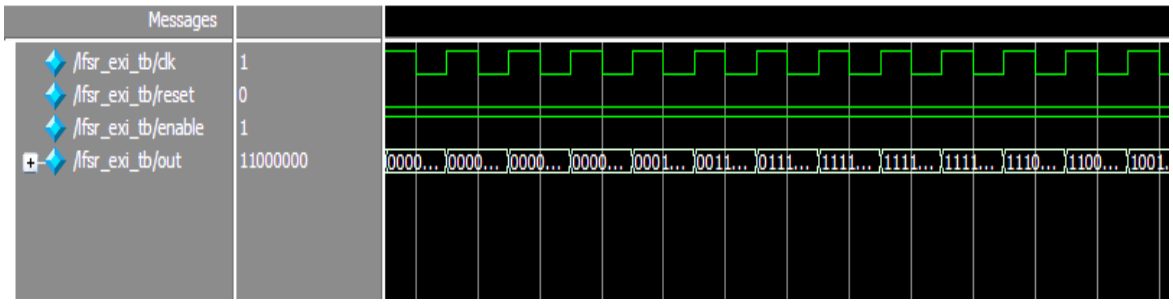


Fig 1) LFSR TPG PATTERNS

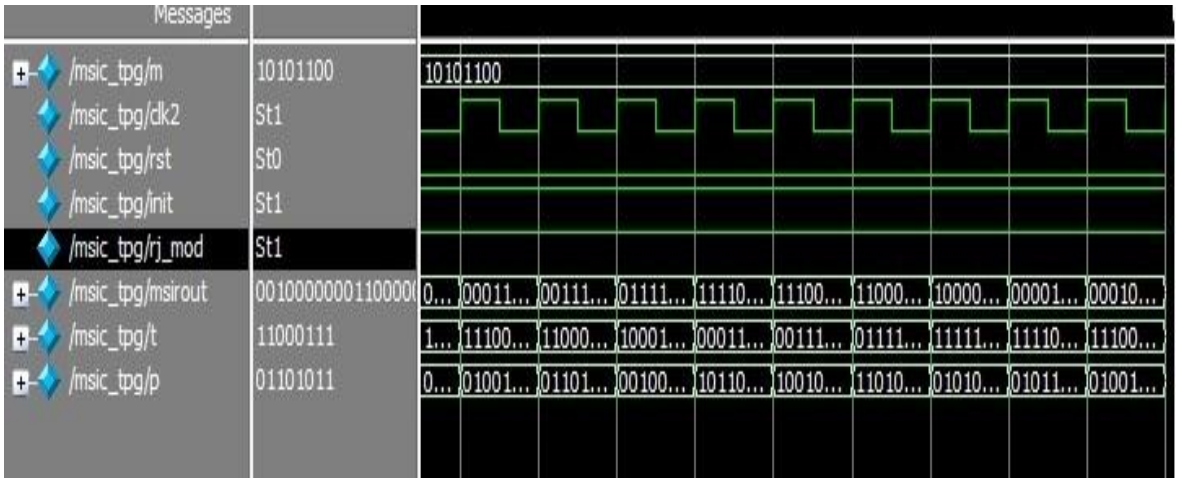


Fig 2) MSIC TPG PATTERNS

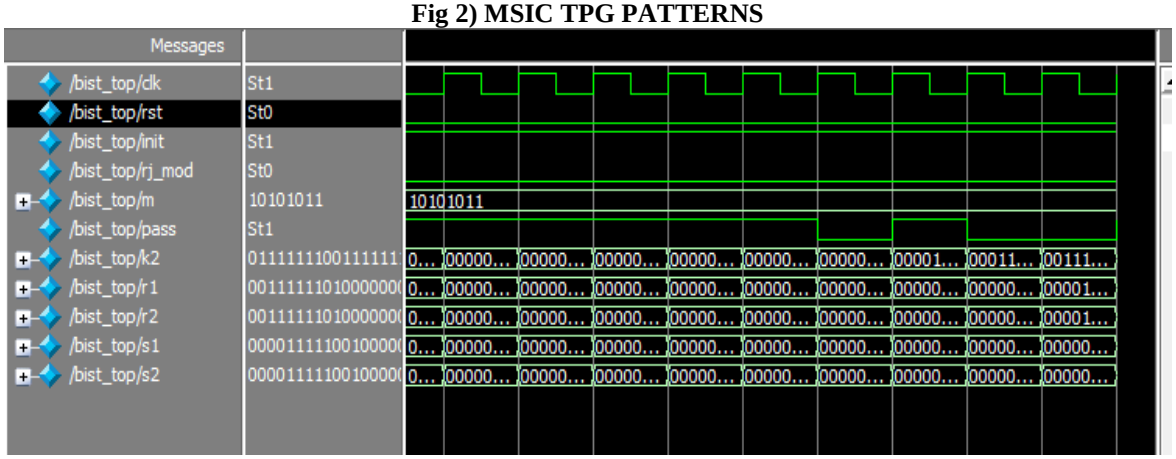


Fig 3) ARRAY MULTIPLIER TESTING RESULTS

VII. CONCLUSION

Analysis results showed that an MSIC sequence had the favorable features of uniform distribution, low input transition density, and low dependency relationship between the test length and the TPG's initial states. Combined with the proposed reconfigurable Johnson counter or scalable SIC counter, the MSIC-TPG can be easily implemented, and flexible to test-per-scan schemes. For a test-per scan scheme, the MSIC-TPG converts an SIC vector to low transition vectors for all scan chains. Experimental results and analysis results demonstrate that the MSIC-TPG is scalable to scan length, and has negligible impact on the test overhead.

REFERENCES

[1]. Y. Zorian, "A distributed BIST control scheme for complex VLSI devices," in 11th Annu. IEEE VLSI Test Symp. Dig. Papers, Apr. 1993,pp. 4–9.

[2]. P. Girard, "Survey of low-power testing of VLSI circuits," IEEE Design Test Comput., vol. 19, no. 3, pp. 80–90, May–Jun. 2002.

[3]. A. Abu-Issa and S. Quigley, "Bit-swapping LFSR and scan-chain ordering: A novel technique for peak- and average-power reduction in scan-based BIST," IEEE Trans. Comput.-Aided Design Integr. Circuits Syst., vol. 28, no. 5, pp. 755–759, May 2009.

[4]. P. Girard, L. Guiller, C. Landrault, S. Pravossoudovitch, J. Figueras, S. Manich, P. Teixeira, and M. Santos, "Low-energy BIST design:Impact of the LFSR TPG parameters on the weighted switching activity,"in Proc. IEEE Int. Symp. Circuits Syst., vol. 1. Jul. 1999, pp.110–113

[5]. S. Wang and S. Gupta, "DS-LFSR: A BIST TPG for low switching activity," IEEE Trans. Comput.-Aided Design Integr. Circuits Syst.,vol. 21, no. 7, pp. 842–851, Jul. 2002.

[6]. F. Corno, M. Rebaudengo, M. Reorda, G. Squillero, and M. Violante,"Low power BIST via non-linear hybrid cellular automata," in Proc. 18th IEEE VLSI Test Symp., Apr.–May 2000, pp.29–34.

[7]. P. Girard, L. Guiller, C. Landrault, S. Pravossoudovitch, and H. Wunderlich, "A modified clock scheme for a low power BIST test pattern generator," in Proc. 19th IEEE VTS VLSI Test Symp., Mar.–Apr. 2001,pp. 306–311.

[8]. D. Gizopoulos, N. Krantitis, A. Paschalis, M. Psarakis, and Y. Zorian,"Low power/energy BIST scheme for datapaths," in Proc. 18th IEEE VLSI Test Symp., Apr.–May 2000, pp. 23–28.

[9]. Y. Bonhomme, P. Girard, L. Guiller, C. Landrault, and S. Pravossoudovitch, "A gated clock scheme for low power scan testing of logic ICs or embedded cores," in Proc. 10th Asian Test Symp., Nov. 2001, pp253–258. LIANG et al.: TEST PATTERNS OF MULTIPLE SIC VECTORS 623

[10]. C. Laoudias and D. Nikolos, "A new test pattern generator for high defect coverage in a BIST environment," in Proc. 14th ACM Great Lakes Symp. VLSI, Apr. 2004, pp. 417–420.

[11]. S. Bhunia, H. Mahmoodi, D. Ghosh, S. Mukhopadhyay, and K. Roy, "Low-power scan design using first-level supply gating," IEEE Trans. Very Large Scale Integr. (VLSI) Syst., vol. 13, no. 3, pp. 384–395, Mar.2005.
[12]. X. Kavousianos, D. Bakalis, and D. Nikolos, "Efficient partial scan cell gating for low-power scan-based testing," ACM Trans. Design Autom. Electron. Syst., vol. 14, no. 2, pp. 28-1–28-15, Mar. 2009.
[13]. P. Girard, L. Guiller, C. Landrault, and S. Pravossoudovitch, "A test vector inhibiting technique for low energy BIST design," in Proc. 17th IEEE VLSI Test Symp., Apr. 1999, pp. 407–412.
[14]. S. Manich, A. Gabarro, M. Lopez, J. Figueras, P. Girard, L. Guiller, C. Landrault, S. Pravossoudovitch, P. Teixeira, and M. Santos, "Low power BIST by filtering non-detecting vectors," J. Electron. Test.-Theory Appl., vol. 16, no. 3, pp. 193–202, Jun. 2000.
[15]. F. Corno, M. Rebaudengo, M. Reorda, and M. Violante, "A new BIST architecture for low power circuits," in Proc. Eur. Test Workshop, May 1999, pp. 160–164.
[16]. S. Gerstendorfer and H.-J. Wunderlich, "Minimized power consumption for scan-based BIST," in Proc. Int. Test Conf., Sep. 1999, pp. 77–84.
[17]. A. Hertwing and H. Wunderlich, "Low power serial built-in self-test,"in Proc. Eur. Test Workshop, 1998, pp. 49–53.
[18]. S. Wang and W. Wei, "A technique to reduce peak current and average power dissipation in scan designs by limited capture," in Proc. Asia South Pacific Design Autom. Conf., Jan. 2007, pp. 810–816.
[19]. N. Basturkmen, S. Reddy, and I. Pomeranz, "A low power pseudorandom BIST technique," in Proc. IEEE Int. Conf. Comput. Design: VLSI Comput. Process., Sep. 2002, pp. 468–473.
[20]. S. Wang and S. Gupta, "LT-RTPG: A new test-per-scan BIST TPG for low switching activity," IEEE Trans. Comput.-Aided Design Integr. Circuits Syst., vol. 25, no. 8, pp. 1565–1574, Aug. 2006.
[21]. M. Nourani, M. Tehranipoor, and N. Ahmed, "Low-transition test pattern generation for BIST-based applications," IEEE Trans. Comput., vol. 57,no. 3, pp. 303–315, Mar. 2008.