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An Efficient Implementation of Downsampler and Upsampler Application to Multirate Filters

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Abstract: *ThePaper Presents efficient implementation of downsampler and upsampler using Multirate digital signal processing system which includes sampling rate conversion. The adder which is used in down and upsampler is replaced by modified carry select adder and the circuit obtained is verified and compared successfully to show low power and area consumption and the same is implemented for tunable band pass filter. A noised input speech signal is denoised after filtering in the multirate filter application. Reduction of power and area is important for VLSI system and also it becomes one of the most critical design parameter.*

Keywords**:** *VLSI-Very large scale integrated circuit, DSP-Digital signal processing, VHDL-Very high speed hardware description language, CSLA-Carry select adder, RCA- Ripple carry adder, BEC-Binary to excess 1 converter*

I. Introduction

In multirate DSP the sampling rate of a signal is changed in order to increase the efficiency ofvarious signal processing operations [1]. Down-sampling reduces the sampling rate whereas up-sampling increases thesampling rate. Basic operations of multirate processing are Upsampler, Downsampler, Decimation and Interpolation.

1.1 Upsampling: An Upsampler with sampling factor L, where L is a positive integer and every L^{th} sample is takenfrom x[n] with all others zero which develops an output sequence $x_e[n]$ with a sampling rate that is L times greater
than that of the input sequence.

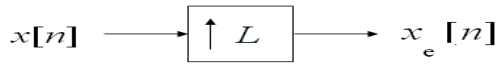

Fig. 1 Block-diagram representation

1.2 Downsampling:A down-sampler with a down-sampling factor M, where M is a positive integer [2], develops an output sequence y[n] with asampling rate that is $(1/M)^{th}$ of that of the input sequence x[n]. If the original sequence contains frequency componentsabove π / M, the downsampler should be preceded by a lowpass filter with cut off frequency π / M.

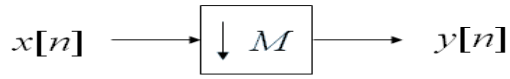

Fig.2 Block diagram representation

1.3 Decimation:Decimation is a technique for reducing the number of samples in a discrete-time signal [2]. The elementwhich implement this technique is referred to as a decimator.

1.4 Interpolation*:* Interpolation is a method of constructing new data points within the range of a discrete set of knowndata points. Interpolation increase sampling rate by integer factor.

II. Figures Of Samplers

The block diagrams of the samplers are structured depending upon the sampling factor. The sampling factor used in this paper is 3 for both upsampler and downsampler .

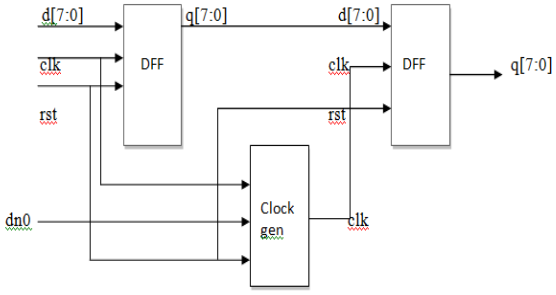

Fig. 3 Block diagram of downsampler

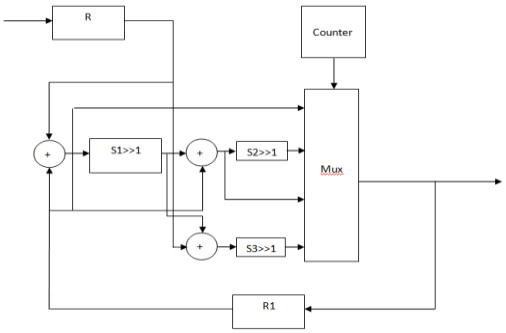

Fig. 4 Block diagram of upsampler

Carry Select Adder (CSLA) is one of the fastest adders used in many data-processing processors to perform fast arithmetic functions [5]

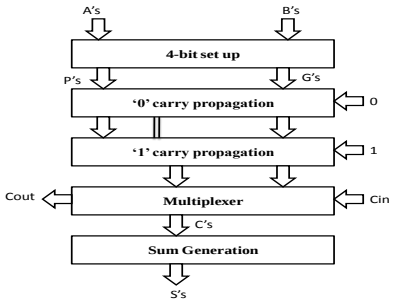

Fig. 5 Carry select adder

From the structure of the CSLA, it is clear that there is scope for reducing the area and power consumption in the samplers. CSLA is not more area efficient because it uses multiple pairs of Ripple Carry Adders (RCA) to generate partial sum and carry by considering carry input C_{in}=0 and C_{in}=1, then the final sum and carry are selected by the multiplexers (mux). The basic idea of this project is to use Binary to Excess-1 Converter (BEC) instead of RCA withC_{in}=1 in the regular CSLA to achieve lowerarea and powerconsumption [6]-[8]. The main advantage of this BEC logic comes from the lesser number of logic gates than the n-bit Full Adder (FA) structure.

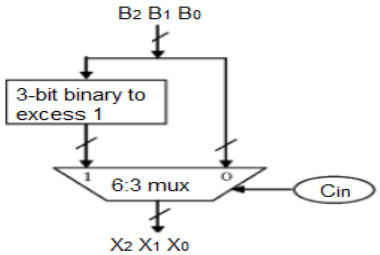

Fig. 6 3- bit BEC with 6:3 mux

The Boolean expression of the 3-bit BEC is as shown below:

$X_0 = \sim B_0$
$X_1 = B_0 \oplus B_1$

$$X_2 = B_2 \oplus (B_1 \times B_0)$$

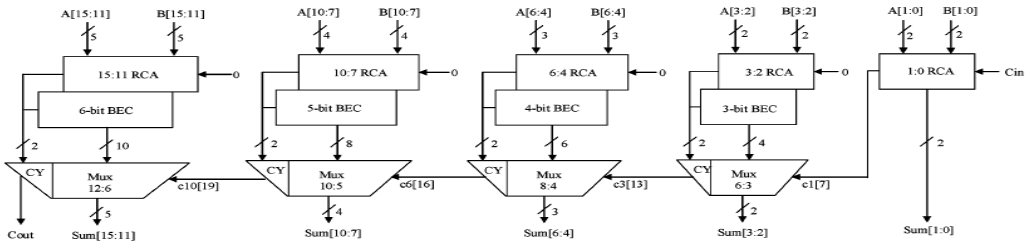

Fig. 7 Modified CSLA

A modified carry select adder is used in place of adders in the block diagram of upsampler and downsampler and hence the result is compared between the downsamplers and upsamplers to show the reduction of area.

Downsampler new				upsampler new			
Number of Slices	41	768	5%	Number of Slices	69	768	8%
Number of Slice Flip Flops	48	1536	3%	Number of Slice Flip Flops	36	1536	2%
Number of 4 input LUTs	67	1536	4%	Number of 4 input LUTs	133	1536	8%
Number of bonded IOBs	50	63	79%	Number of bonded IOBs	33	63	52%
Number of GCLKS	1	8	12%	Number of GCLKS	1	8	12%
Downsampler old				**upsampler old**			
Number of Slices	52	768	6%	Number of Slices	81	768	10%
Number of Slice Flip Flops	49	1536	3%	Number of Slice Flip Flops	49	1536	3%
Number of 4 input LUTs	80	1536	5%	Number of 4 input LUTs	152	1536	9%
Number of bonded IOBs	50	63	79%	Number of bonded IOBs	35	63	55%
Number of GCLKS	1	8	12%	Number of GCLKS	1	8	12%

Sampler old is the block diagram which uses only the adders whereas sampler new is the one which uses modified carry select adder.

III. Multirate Design Methodology

Design of the down sampler and upsampler is done with M = 3 and L= 3. The design procedure can be extended for an arbitrary M and L. The same design of upsampler and downsampler which consists of a modified carry select adder is used in tunable band pass filter as a multirate application. The noised input signal of a filter is denoised and obtained as filter output.

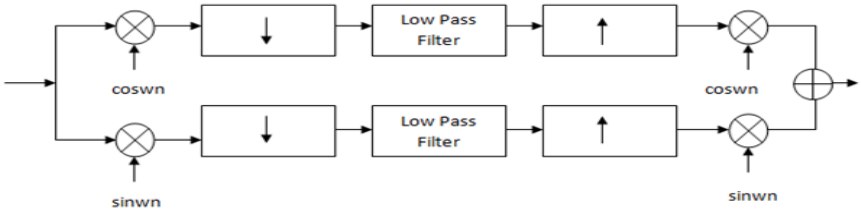

Fig. 8 Tunablebandpass filter block diagram

IV. Results

3.1 Simulation of Down Sampler

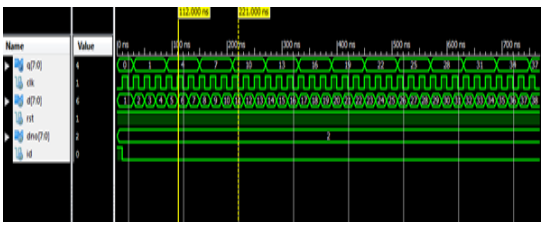

Fig. 9 Timing diagram of downsampler

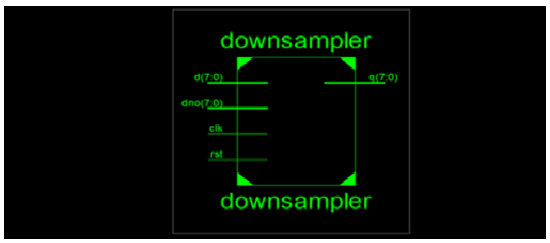

Fig. 10 RTL View

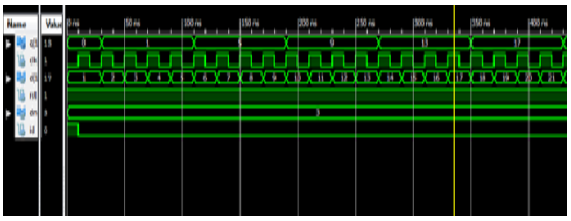

Fig. 11 Timing diagram of downsampler with modified carry select adder

3.2 Simulation of Up Sampler

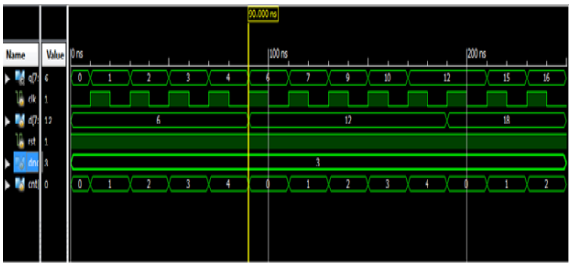

Fig. 12 Timing diagram of upsampler

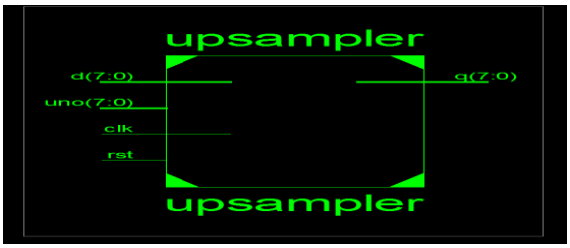

Fig. 13 RTL View

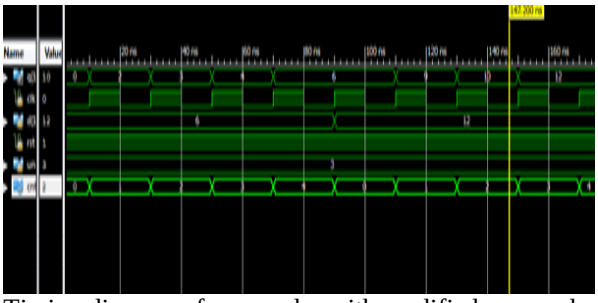

Fig. 14 Timing diagram of upsampler with modified carry select adder

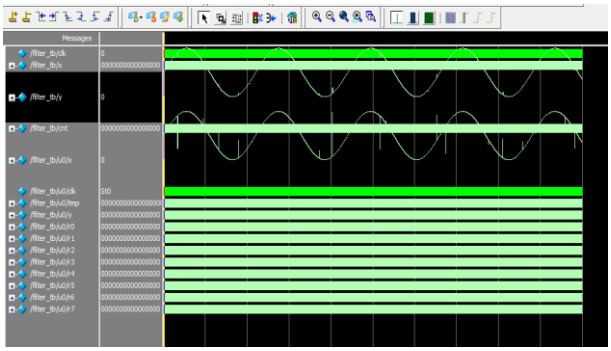

Fig. 15 Results before and after filtering in Tunable band pass filter

3.3 Comparison for area and power

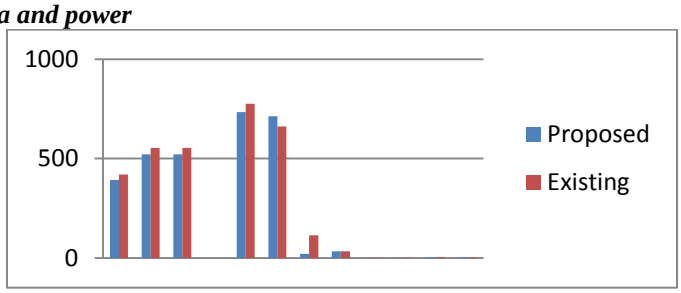

Fig. 16 Comparision between Tunable band pass filter used in application after and before using modified carry select adder in terms of area

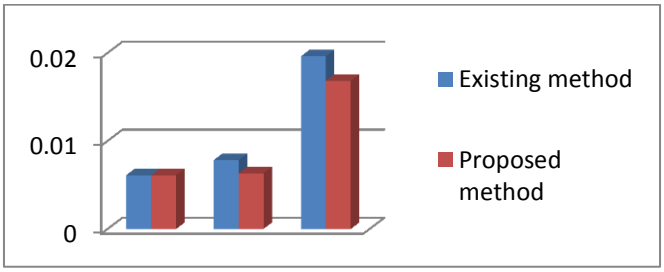

Fig. 17 Comparision of power

V. Conclusion

Multirate systems are commonly used for audio, video processing, communication systems and transform analysis.

The implementation ofdownsampler and upsampler with multirate signal processing approach is presented. The results are found satisfactory. Physical testing verified that implementation worked correctly for all factors. The proposed methodology which uses a modified carry select adder provides a systematic way to derive low power and area consumption.The same is used in the application of tunable band pass filter but using a modified carry select adder increases the delay.

VI. Future Scope

In future, efforts will be directed towards transistor level implementation of multirate modules to get full custom design with different circuit topology and optimization level to obtain very less area and power.

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