Analysis and Experimental Results of Interior DAC of SAR ADC using Cadence

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Abstract: *This paper focuses on analysis and experimental results of 6-bit charge-redistribution DAC and 6-bit charge-redistribution DAC using split array configuration. These DAC configurations are designed and simulated using GPDK 180nm CMOS technology. DAC is an important component within the SAR ADC. The charge redistribution DAC in a Split capacitor configuration has a total capacitance which is 87.5% smaller compared to a conventional design. Hence DAC gives the optimized architecture. Optimized design of DAC architecture ensures the accuracy of the components, which improves the performance of SAR ADC. The matching accuracy of integrated capacitors is excellent. The simulation results of both are compared. The delay required to get the output is 793.7E-15S and 793.6E-15S when all input bits are high for charge-redistribution DAC and split array DAC respectively. Dynamic range for these DACs is 35.98dB. The supply voltage is 1.8V.*
Keywords: *Analog- to- Digital converter, Digital- to- Analog converter, Charge redistribution, Successive Approximation, Split array.*

I. Introduction

Successive Approximation Register Analog-to-Digital Converter (SAR ADC) compares the input voltage and output voltage of an N-bit digital-to-analog converter (DAC) with only one comparator. The output voltage of DAC is used as a reference voltage; SAR ADC can get the final conversion result through a total of N times comparison. SAR ADC has moderate accuracy and moderate speed. It could achieve smaller chip area and low power consumption with CMOS technology. SAR ADC is widely used in industrial control, medical instrumentation, microprocessor-assisted analog-digital conversion interfaces and other fields. SAR ADC linearity is mainly limited by the linearity of built-in DAC and the structure of DAC. The match precision of devices are the decision factors for ADC's performance. Therefore, it is the key component to ensure the performance of SAR ADC that design a DAC with considerable accuracy for the overall system [1]. In recent work on SAR ADCs a new Digital-to-Analog Converter was introduced. This new converter is based on charge redistribution and it can easily be operated at very high sampling rates. Furthermore the matching accuracy of integrated capacitors is excellent. Converters up to 12-bit or even more resolution are possible without any adjustments. DACs that are used in ADCs are already adequate if they only show the right output value when the comparator action takes place [7]. The array capacitance influences the RC settling time of the DAC and therefore limits the entire converter speed. Reduction of capacitance and the die area of the DAC can be achieved by using split capacitor technique [3]

This paper describes analysis of 6-bit charge redistribution DAC and its implementation using split array technique. Section II discusses basics of charge–redistribution DAC. Section III discusses its implementation using Cadence. Section IV contains experimental results and Section V contains conclusions.

II. Basics Of Charge Redistribution And Split Array Dacs

1.1 Charge redistribution DAC

Fig.1 shows, a charge redistribution DAC is a parallel array of binary-weighted capacitors, 2^NC in total. After initially being discharged, the digital signal switches each capacitor to either V_{ref} or ground, causing the output voltage, V_{out}, to be a function of the voltage division between the capacitors [5,6].
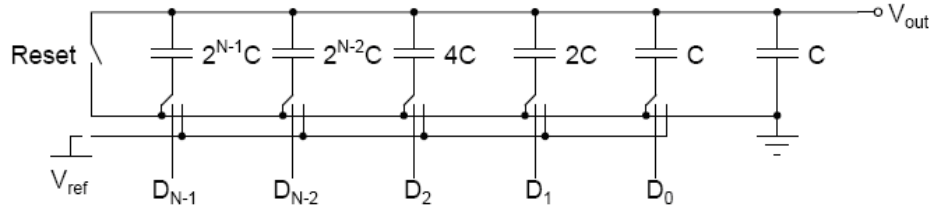

Fig. 1. A Charge-redistribution DAC

The capacitor array totals $2^N C$. Therefore, if the MSB is high and the remaining bits are low, then a voltage divider occurs between the MSB capacitor and the rest of the array. The analog output voltage, V_{out}, becomes:

$$V_{out} = V_{ref} \cdot \frac{2^{N-1}C}{\left(2^{N-1} + 2^{N-2} + 2^{N-3} + ... + 4 + 2 + 1 + 1\right)C} = V_{ref} \cdot \frac{2^{N-1}C}{2^N C} = \frac{V_{ref}}{2} \tag{1}$$

which confirms the fact that the MSB changes the output of a DAC by ½ V_{ref}. Fig. 2 shows the equivalent circuit under this condition.
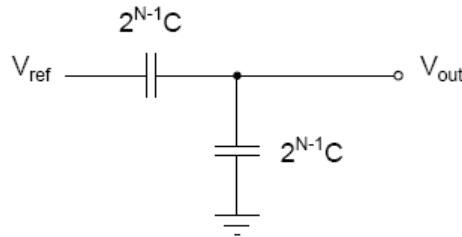

Fig. 2. Equivalent circuit with the MSB = 1, and all other bits set to zero

The ratio between V_{out} and V_{ref} due to each capacitor can be generalized to:

$$V_{out} = \frac{2^k C}{2^N C} . V_{ref} = 2^{k-N} . V_{ref} \tag{2}$$

Where it is assumed that the k-th bit, D_k, is one and all other bits are zero. Superposition can then be used to find the value of V_{out} for any input word by:

$$V_{out} = \sum_{k=0}^{N-1} D^k 2^{k-N} . V_{ref} \tag{3}$$

1.2 Split array DAC
   The charge-redistribution architecture is very popular because of its simplicity and relative good accuracy. Although a linear capacitor is required, high resolution in the 10- to 12-bit range can be achieved. However, as the resolution increases, the size of the MSB capacitor becomes a major concern. For example if the unit capacitor, *C*, were 0.5pF, and a 12-bit DAC were to be designed, the MSB capacitor would need to be:

$$C_{MSB} = 2^{N-1} . 0.5pF = 1024 \ pF \tag{4}$$

   One method of reducing the size of the capacitors is to use a split array. A 6-bit example of the array is shown in Fig. 3. This architecture is slightly different from the charge-redistribution DAC shown in Fig. 1 in that the output is taken off a different node and an additional attenuation capacitor is used to separate the array into a LSB array and a MSB array. Note that the LSB, D_0, now corresponds to the leftmost switch and that the MSB, D_5, corresponds to the rightmost switch [5,6].
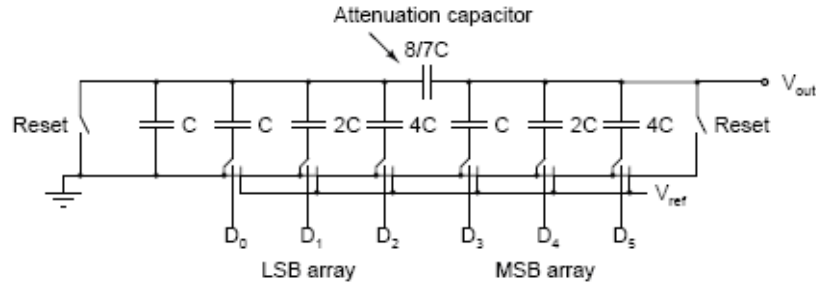
Fig. 3. A Charge-redistribution DAC using a split array

The value of the attenuation capacitor can be found by:

C_{att} = (Sum of the LSB array capacitors / sum of the MSB array capacitors) * C   (5)

Where the sum of the MSB array equals the sum of LSB capacitor array minus *C*. The value of the attenuation capacitor should be such that the series combination of the attenuation capacitor and the LSB array, assuming all bits are zero, equals *C*. To prove this a derivation is made, refer to formula (6). The output voltage is defined as the attenuation factor times the LSB bits plus the MSB bits times the reference voltage. The attenuation factor is a capacitive divider between the attenuation capacitor and the sum of the LSB capacitors. One can see that with some manipulation this is equal to formula (3).

$$V_{out} = \left(\frac{\dfrac{2^{N/2}}{2^{N/2}-1}}{\dfrac{2^{N/2}}{2^{N/2}-1}+2^{N/2}} \sum_{k=0}^{N/2-1} D_k 2^{k-N/2} + \sum_{k=N/2}^{N-1} D_k 2^{k-N} \right).V_{ref}$$

$$= \left(\frac{1}{2^{N/2}} \sum_{k=0}^{N/2-1} D_k 2^{k-N/2} + \sum_{k=N/2}^{N-1} D_k 2^{k-1} \right).V_{ref} \qquad (6)$$

$$= \left(\frac{2^{N/2}}{2^{N/2}} . \sum_{k=0}^{N/2-1} D_k 2^{k-N} + \sum_{k=N/2}^{N-1} D_k 2^{k-N} \right).V_{ref}$$

$$= \left(\sum_{k=0}^{N/2-1} D_k 2^{k-N} + \sum_{k=N/2}^{N-1} D_k 2^{k-N} \right).V_{ref}$$

$$= \sum_{k=0}^{N-1} D_k 2^{k-N} .V_{ref}$$

A drawback of the split array is that spreading in the attenuation capacitor affects all the capacitors after the attenuation capacitor. Therefore, care in the layout should be taken.

III.   Implementation Of Charge Redistribution And Split Array Dacs

The 6-bit charge-redistribution DAC architecture is shown in fig. 4. The unit capacitance C = 0.5pF is used. Total capacitance used in this DAC architecture is 32pF. The input pulses are applied to D_5,D_4,D_3,D_2,D_1,D_0 and their specifications are mentioned in Table I .
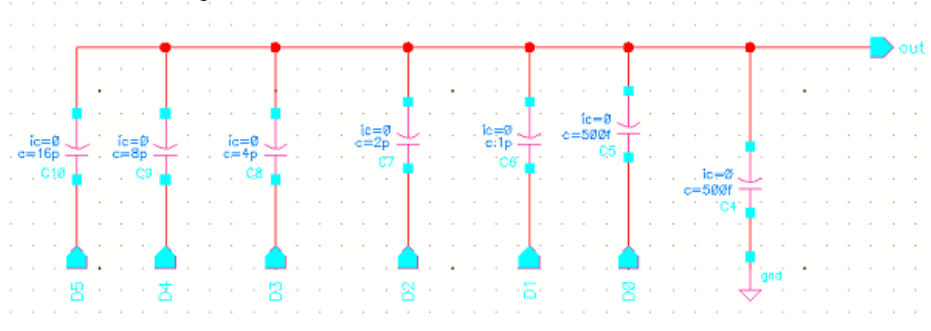

Fig. 4. 6 bit charge redistribution DAC schematic.

The 6-bit charge-redistribution DAC using a split array is shown in fig. 5. The unit capacitance C = 0.5pF is used and total capacitance of this circuit is 4pF. The input pulses are applied to D_5,D_4,D_3,D_2,D_1,D_0 and their specifications are mentioned in Table I . The symbol view of split array DAC is shown in fig. 6.
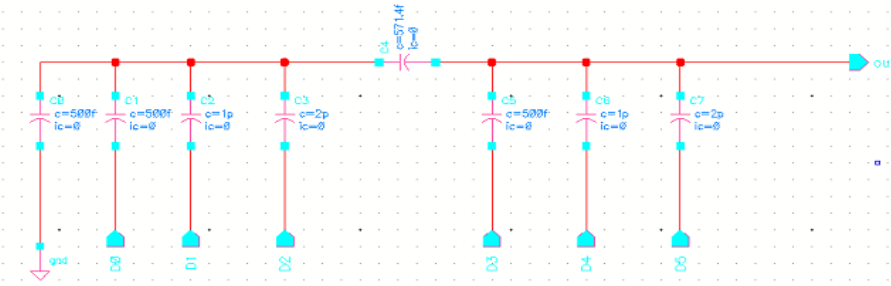
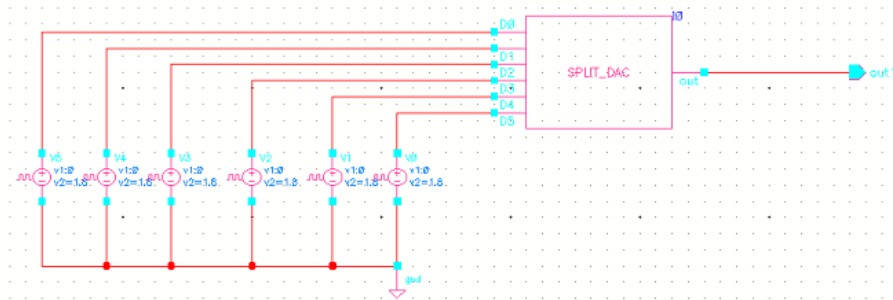Fig. 5. A 6 Bit charge-redistribution DAC using a Split array schematic.

Fig. 6. A symbol view of 6 Bit charge-redistribution DAC using a split array

IV. Experimental Results

The simulation results of 6-bit charge-redistribution DAC are shown in the fig. 7. For 6-bit charge-redistribution DAC using a split array, the results are shown in fig. 8. The Input pulses are shown in Table I for $D_5, D_4, D_3, D_2, D_1, D_0$ and results are shown in Table II for some input bit combinations. The delay calculated is 793.7 E-15S, and 793.6E-15S for charge-redistribution and using split array respectively, this is the time required to get output after applying inputs when all input bits are high.
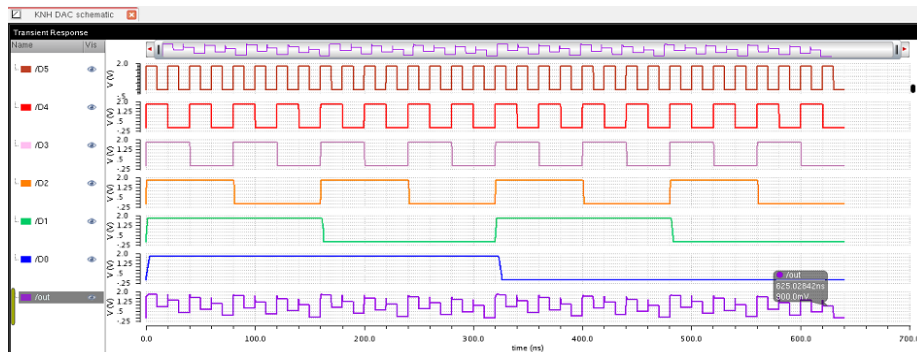

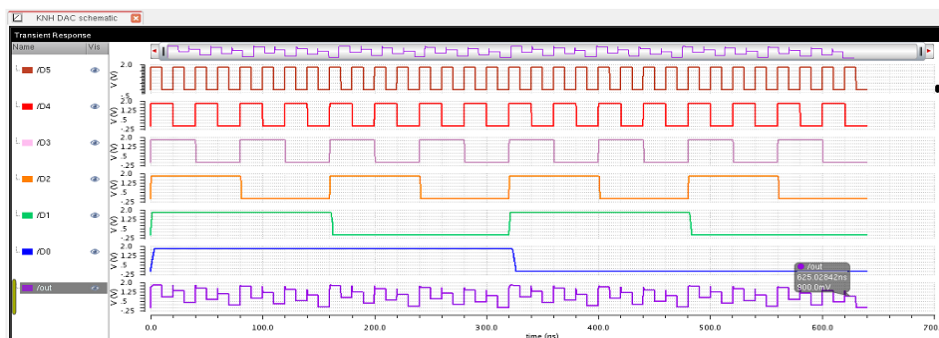Fig. 7. Simulation Results of 6 Bit charge-redistribution DAC

Fig. 8. Simulation results of 6 Bit charge-redistribution DAC using a Split array

TABLE I: INPUT PULSES

Inputs	Specifications
D_5 (MSB)	V1=0v, V2=1.8V, Ton = 10ns, T = 20ns
D_4	V1=0v, V2=1.8V, Ton = 20ns, T = 40ns
D_3	V1=0v, V2=1.8V, Ton = 40ns, T = 80ns
D_2	V1=0v, V2=1.8V, Ton = 80ns, T = 160ns
D_1	V1=0v, V2=1.8V, Ton = 160ns, T = 320ns
D_0 (LSB)	V1=0v, V2=1.8V, Ton = 320ns, T = 640ns

TABLE II: ANALOG OUTPUT VOLTAGES FOR SOME INPUT BIT COMBINATIONS

Input bits $D_5D_4D_3D_2D_1D_0$	Output of Split DAC	Output of Binary weighted DAC
000000	-159.33nV	-17.896V
100000	900.00mV	900.00mV
010000	450.00mV	450.00mV
110000	1.35V	1.35V
001000	225.00mV	225.00mV
111111	1.7719V	1.7719V

V.   Conclusion

The designed DACs are simulated using GPDK 180nm CMOS technology. The results of 6-bit charge-redistribution DAC and its implementation using split array technique are compared. The delay required to get the output for 6-bit charge-redistribution DAC is 793.7 E-15 S and for a split array is 793.6 E-15 S. Dynamic range for these architectures is 35.98dB. The total capacitance required for 6-bit charge-redistribution DAC is 32pF and for split array is 4pF for a unit capacitance of 0.5pF. The charge redistribution DAC in a Split capacitor configuration has a total capacitance which is 87.5% smaller compared to a conventional design. Hence split array DAC is optimized one.

Acknowledgements

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