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System Level Design of Timing and Frequency Control Circuit

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Abstract: *A multiband wireless system utilizes multiband frequencies in a single system for different wireless applications and the use of these systems is the most prominent feature of today's communication era. In spite of the complicated circuitry used to design these systems; these are widely used because of many important features and these systems are used with the help of timing and frequency control circuit which controls the frequency of the device according to the application. These circuits are used in mobile phones; laptops etc to provide them applications of different frequency range i.e. Bluetooth, WI-Fi, Zig-Bee and GPS etc. In this paper the timing and frequency control circuit is used in the form of PLL i.e. Phase Locked Loop. The PLL controls the frequency range of the circuit according to the application required and hence it can be used in multiband wireless systems. In this paper a timing and frequency control circuit is designed at system level, in which the center frequency is in GHz range and the reference frequency for the circuit is also in RF-range. By keeping the center frequency in GHz range, this PLL can be widely used in multiband wireless systems as it can easily adjust the frequencies required for particular applications. Each component is designed at system level using Verilog - A language in cadence with 1.8V power supply.*

Keywords: *Charge pump, Multiband wireless systems, PFD, PLL, VCO*

I. Introduction

Timing and frequency control circuit specifies the use of timing and frequency synthesis in any circuit, specially the circuits used in communication areas. The importance of timing and frequency control circuits in today's world is very high as these are used everywhere including our laptops and mobile devices for time and frequency synchronization. These circuits matches the timing and frequencies of input signal and feedback signal and hence tries to match the two frequencies to produce a signal which is in phase with the input signal and the best example of such type of circuit is Phase Locked Loop(PLL), which acts as our timing and frequency control circuit. A PLL i.e. a Phase-Locked Loop is a feedback system combining a voltage controlled oscillator and a phase comparator so connected that the oscillator frequency (or phase) accurately tracks that of an applied frequency- or phase-modulated signal. Phase-locked loops can be used, for example, to generate stable output frequency signals from a fixed low-frequency signal. In a phase locked loop, the error signal from the phase detector is the difference between the input signal and the feedback signal. Implementation of these signals in multichannel wireless systems is also a tedious task as a multichannel wireless system utilizes multiband frequencies in a single system for different applications of different frequencies, the timing and frequency circuit here plays a vital role in choosing the frequency which is suitable for a particular application among the bands of frequencies present in the system. So basically this paper deals with the implementation of phase locked loop, as timing and frequency circuit and this circuit will be used in multichannel wireless systems for multiband frequencies and the frequency synthesizer will choose the frequency according to the particular application. In this paper emphasis has been given for high frequencies input signals in GHz range and what effect it will have on our frequency synthesizer circuit as all the components are designed in GHz range which includes Phase Frequency Detector (PFD), Charge Pump (CP), Low pass Filter of second order, Voltage controlled Oscillator (VCO) and frequency divider.

1.1 Basic Overview

A timing and frequency control circuit is a control system that generates an output signal whose phase is related to the phase of an input reference signal. It compares the phase of the input signal with the phase of the signal derived from its output oscillator and adjusts the frequency of its oscillator to keep the phases matched and to obtain the lock condition [3]. The frequency is matched with the feedback signal which is obtained by frequency divider circuit. All the components used in timing and frequency control circuit is described in detail with its system level design in next section.

II. Phase Frequency Detector/Charge Pump

The PFD detects the difference in phase and frequency between the reference clock and the feedback clock inputs and generates an "up" or "down" signals based on whether the feedback frequency is lagging or leading the reference frequency. If an up signal is received by charge pump then current is drawn into the loop filter and if a down signal is received then current is drawn from the loop filter. The function of phase frequency detector is to correct the excess phase between the two inputs and to lock the frequency by varying the VCO voltage and frequency [5]. The phase frequency detector/ charge pump circuit used in this paper mainly consist of two parts; the first part is a phase frequency detector consisting of two d-flip flops, one for up signal and other for down signal, when reference signal is leading then down signal goes high; and when the feedback signal is leading which is the signal received by frequency divider then up signal goes high. The second part consists of a charge pump which is responsible for delivering a current proportional to the phase/frequency difference [8]. The circuit diagram on which system level design of PFD/CP is implemented is shown below:

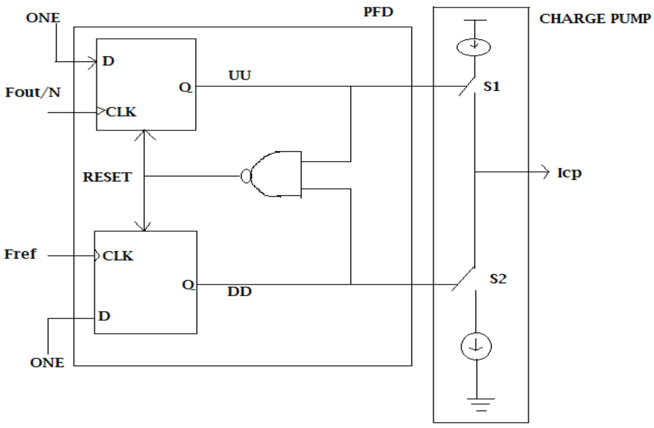

Figure1: Phase Frequency detector with charge pump

2.1 Verilog-A code for PFD/CP

```
`include "disciplines.vams"
`include "constants.vams"
 module pfd_cp1 (out, ref, fb);
 output out; electrical out;
 input ref; voltage ref; Input fb; voltage fb;
parameter  real iout=100u;
parameter  real vh=+1;
parameter  real vl=-1;
parameter  real vth=(vh+vl)/2;
parameter  integer dir=1 from [-1:1] exclude 0;
parameter  real tt=1p from (0:inf);
parameter  real td=0n from [0:inf);
integer state;
analog begin
@(initial_step)
state=0;
@(cross(V(ref)-vth, dir))
if (state > -1)
 state = state - 1;
@(cross(V(fb)-vth, dir))
if (state < 1)
state = state + 1;
I(out) <+ transition(iout*(V(fb)-V(ref)), td, tt);
end
endmodule
```

2.2 System Level simulation result of PFD/CP

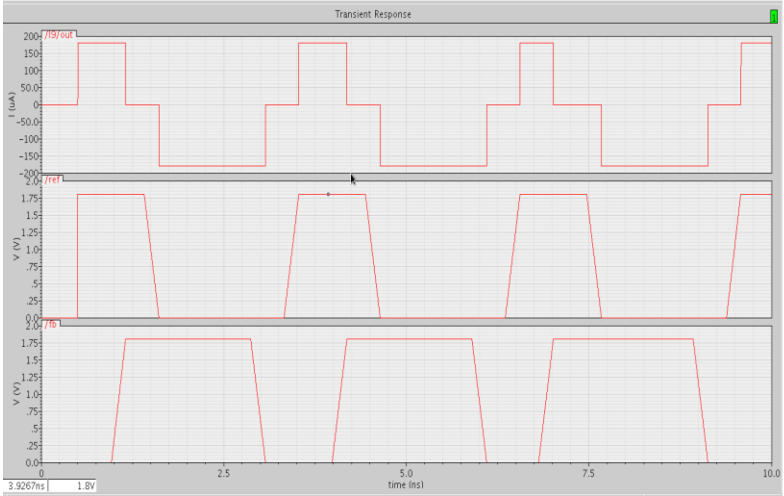

Figure 2: Simulation result of PFD/CP

The simulation result of PFD/CP shows the difference between the phase of reference signal and the feedback signal. This circuit gives current as the output and positive side represents that reference signal appears first and then feedback signal. If both the signals are at high level then the output moves to reset position.

III. Low Pass Filter

The low pass filter passes the current from charge pump to the C1 capacitor to set average VCO frequency. The resistor used in the low pass filter provides instant phase correction without affecting the average frequency [1]. The second capacitor is used to smooth large IR ripples on Vctl. In this paper second order low pass filter is used and system level designing of second order low pass filter is done in cadence platform using Verilog-A. This loop filter is the major component which is responsible for timing and frequency control circuit to get locked as settling of low pass filter determines the locking of this control circuit.

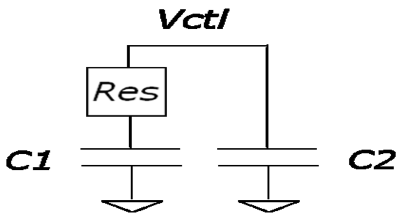

Figure 3: Second order low pass filter

3.1 Verilog A code for Low pass filter

```
 include "constants.vams"
`include "disciplines.vams"
`define PI 3.14
 module LPF1(vin,vout);
 input vin;
 output vout;
 electrical vin,vout;
 parameter real LPF_BW_GHz= 1000 from (0:inf];
 real r1;real r2;real c1;real c2;real wc;
 analog begin
 @(initial_step("tran","ac","dc"))
 begin
 r1=1K;
 r2=1K;
wc=2*`PI*LPF_BW_GHz;
c1=1/(wc*r1);
c2=1/(wc*r2);
```

```
end
V(vout,vin)<+ I(vout,vin)*r1;
V(vout,vin)<+ I(vout,vin)*r2;
I(vout)<+ ddt(V(vout)*c1);
I(vout)<+ ddt(V(vout)*c2);
end
endmodule
```

3.2 System level simulation result of Low pass filter

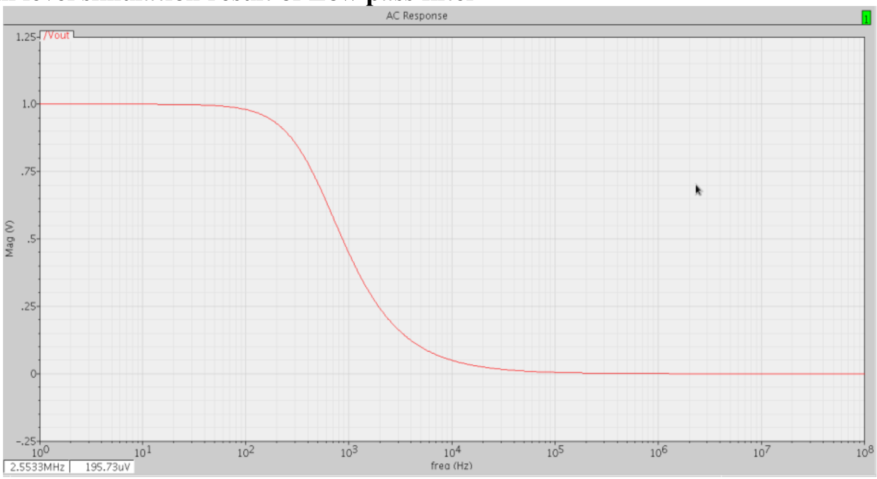

Figure 4: Simulation result of low pass filter

The cut-off frequency obtained from the graph is 50 Hz.

IV. Voltage Controlled Oscillator

The oscillator which is a single output circuit is divided into three main parts; Active circuit, resonating circuit and feedback path. The active circuit is the main tank circuit used in VCO, which can be of NMOS,PMOS or CMOS type depending on the applications [6]. The circuit which is widely used in active circuit is NMOS configuration because the circuit is simple as less number of elements are required to form it and it is best suitable for low voltage VCO [10].

The resonating circuit used in VCO for timing and frequency control circuit comprises of integrated varactors and inductors [11]. These are variable inductors and capacitors which can change its value according to the frequency change and also they are used for RF applications [9]. In this paper a LC type VCO is used to handle GHz range frequencies and system level designing of VCO is done using its transfer function and gain with center frequency in the range of 2 GHz and implemented in cadence using Verilog-A.

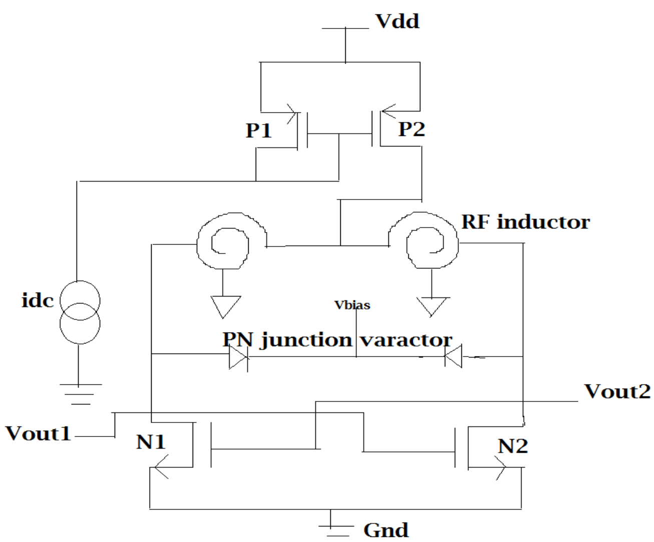

Figure 5: LC type Voltage Controlled Oscillator

4.1 Verilog-A code for VCO

```
`include "disciplines.vams"
`include "constants.vams"
`define PI 3.14
module vco1 (vin,vout);
input vin;
output vout;
electrical vin,vout;
parameter real amp=1;
parameter real center_freq=0.9G;
parameter real vco_gain=1G;
parameter integer steps_per_period=32;
real phase;
real inst_freq;
analog begin
inst_freq=center_freq+vco_gain*V(vin);
$bound_step(1.0/(steps_per_period*inst_freq));
phase=idtmod(inst_freq,0,1);
V(vout)<+ amp*sin(2*`PI*phase);
end
endmodule
```

4.2 System level simulation result of VCO

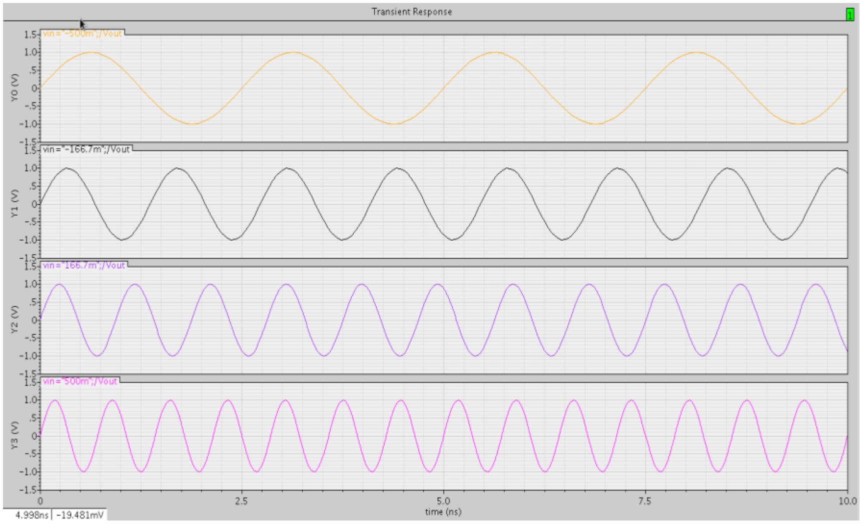

Figure 6: Simulation result of VCO

The output of the VCO shows that the output is dependent on input signal. The above simulation shows that with different input voltages the frequency of VCO is also changing.

V. Frequency Divider

Frequency dividers are made up of logic gates and flip flops.They can be divided into synchronous and asynchronous types [2] . In synchronous each flip flop is triggered by the input signal of the divider, but in case of asynchronous dividers the input signal of the divider feeds the first flip flop, which triggers the second one and so on. Since the synchronous divider achieves a faster transition than the asynchronous divider; frequency divider used in this paper is of asynchronous type which is designed using JK flip flops [4]. The frequency divider using JK flip flop consist of three stages where the output of first stage is give to second and second stage input and output is given to nand gate; whose output is fed to the final block. Each block of JK flip flop itself acts like a divide by 2 circuit. In this type of divider each stage changes at the clock edges. Asynchronous type of 3 stage divider is shown below:

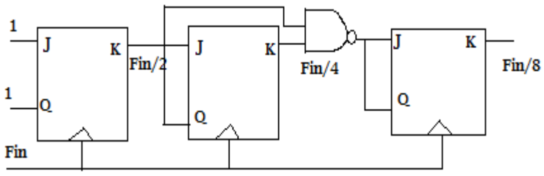

Figure 7: Asynchronous type of frequency divider

5.1 Verilog-A code for frequency divider

```
        `include "discipline.h"
module V_jk_ff(q, clk, j, k);
        input clk,j,k;
 output q;
 voltage q, clk,j,k;
        parameter real  tdelay   = 0n from [0:inf),
                        ttransit = 0n from [0:inf),
                        vout_high =1.8,
                       vout_low  = 0 from (-inf:1),
                       vth       = 0.9;
integer x;
analog
begin
        @(initial_step) x = 0;
 @(cross(V(clk) - vth, +1))
        begin
         if (V(j) > vth)
        case (V(k) > vth)
         1 : x = !x;
        0 : x = 1;
        endcase
        else
          if (V(k) > vth) x = 0;
         end
 V(q)   <+ transition( vout_high*x  + vout_low*!x, tdelay, ttransit );
 end
endmodule
```

5.2 System level simulation result of Frequency divider

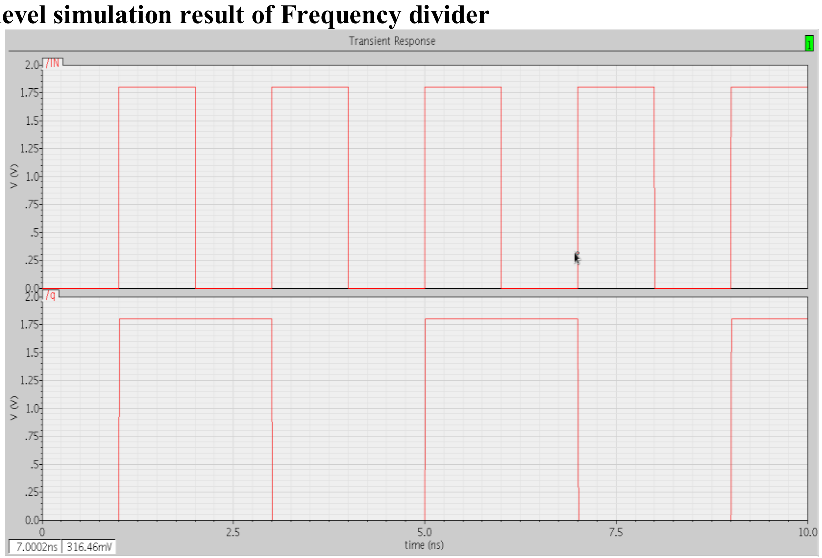

Figure 8: Simulation result of frequency divider

The simulation result of frequency divider shows that it divides the frequency by 2. If the input signal is of frequency 500 MHz then the output signal is of frequency range 250 MHz and here JK flip flop is used as frequency divider by 2.

VI. Transfer Function Of Each Block

A transfer function is a mathematical representation, in terms of spatial or temporal frequency, of the relation between the input and output of a linear time invariant system with zero initial conditions and zero point equilibrium. The transfer function of each block is as follows [7]:

- Transfer function of PFD is:
  $V_{inVCO} = 1+j\omega R_2C/1+j\omega(R_1+R_2)C * V_{PDtri} = K_f. V_{PDtri}$........................ (1)
  Where $V_{PDtri} = Vdd/4\pi$ (volts/radian).. (2)
- Transfer function of Charge Pump is:

$V_{inVCO} = I_{PDI}*1+j\omega RC_1/j\omega(C1+C2) * [1+j\omega RC_1C_2/C_1+C_2]= K_f. I_{PDI}$..(3)

- Transfer function of Low Pass Filter is:

$F_{LPF}(s) = sR_1C_1+1/s (sC_1C_2R_1+C_1+C_2)$……………………………… (4)

- Transfer function of VCO is:

$P_o(s)/V_o(s)= V_o/s$………………………………………………………(5)
where $P_o(t)= K_oV_o(t)dt$ and.…………………………………………. (6)
$V_o(t)= V \cos(\omega_ot+ K_o/\omega_m* V_m \sin \omega_mt)$………………………………. (7)

VII. Timing And Frequency Control Circuit Using Verilog-A

The timing and frequency control circuit using Verilog-A is designed using all the components of this circuit; designed in Verilog-A, which is explained in previous sections along with simulation results. The block diagram of timing and frequency control circuit designed using Verilog-A is as shown below:

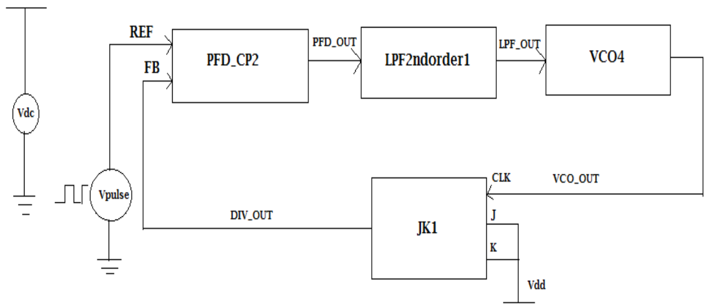

Figure 9: Block diagram of timing and frequency control circuit

The functioning of all the blocks is as same mentioned above. The PFD_CP2 block detects the difference between the reference signal and feedback signal and passes the output to low pass filter which filters out all the high frequency signals and passes the low frequency signals to VCO input which produce oscillations according to the input and provide the output to feedback path which consist of a JK flip flop which acts as divide by 2 circuit and divides the VCO output by 2 and then this signal is again fed back to PFD for phase and frequency comparison [6]. This process continues until the phase is locked and VCO produce a constant frequency signal. The schematic of this circuit in cadence is as shown below:

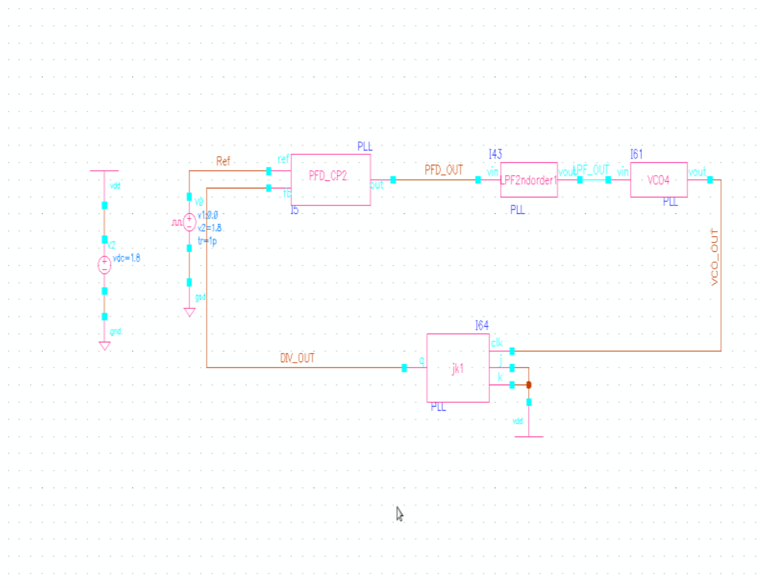

Figure 10: Schematic view of timing and frequency control circuit using Verilog-A

7.1 System level simulation result of timing and frequency control circuit

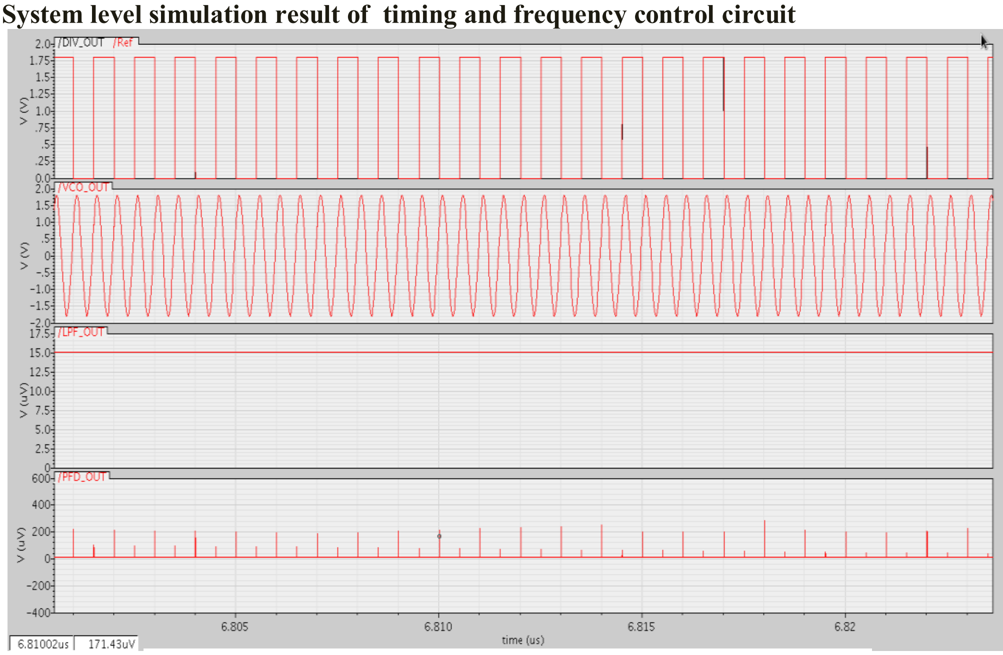

Figure 11: Simulation result of timing and frequency control circuit

The above simulation results show the phase when the reference frequency is matched with the feedback frequency and the circuit is in lock condition. The lock obtained in this case is approximately at 6.8ns; when the low pass filter settles down completely; VCO is producing the same frequency which is our centre frequency (2GHz) and the difference between the reference frequency and feedback frequency is also zero.

VIII. Conclusion

The timing and frequency control circuits are widely used in the multiband wireless systems as in these systems many applications run simultaneously under various frequency bands, the best example of multiband wireless systems are mobile phones, which are widely used today and it shows the best use of frequency synthesizer circuits as different applications with different frequency bands can run simultaneously at the same time for example Bluetooth, Zig-Bee, GPS etc. these all applications are of different frequencies but can run on a same system because of timing and frequency control circuit or frequency synthesizer. Since the design of the timing and frequency control circuit is concentrated on GHz range, the centre frequency was 2GHz as the frequency can be adjusted according to the particular application from low to high. All the components i.e.

Phase frequency Detector (PFD), Charge Pump (CP), Voltage controlled oscillator (VCO) and programmable frequency divider are designed for GHz range applications varying from the center frequency of 2GHz to 30GHz.

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