

Digital Technique for Analog Built-in Self-Test

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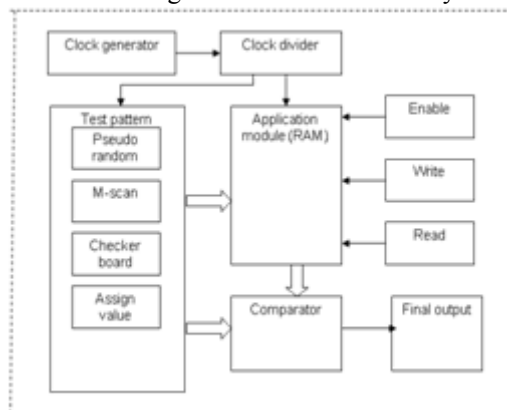
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Abstract: A device core logic testing of analog signals with minimal area overhead for measuring on chip voltages in digital circuits can be adopted by built-in-self-test in a distributed architecture. Here for measuring this analog voltage, the subsampled signal pair is fed to delay measurement to measure the skew between this pair. The routing of analog signals over long paths can be minimized by using clock gating. A clock is routed serially to the nodes of analog test voltage with consists of delay cells, flipflops. However the test voltage to a scheme between pair of signals raise to the signal pair at node.

Index terms: built-in self-test (BIST), current starved, over-sampling ratio, quantization, subsampling.

I. Introduction

In analog circuits BIAS VARIATION is a common problem and is getting worse as the technology scales. In here the variation of process is increasing, and reduces the power supply. Increased popularity of mixed signal IC designs in the deep submicron process, to precisely measure analog voltages for testing & debugging process. When measuring on-chip voltages such situations arise in BIST applications, while measuring voltages at the terminals of sleep transistors for power monitor applications and in measuring low bandwidth signals in sensor systems. These analog voltages could be potentially located all over the chip. For displaying analog signal waveforms using the technique of subsampling. For viewing waveforms in laboratory this method is well suited. For automated testing it cannot be used directly.



In the proposed architecture, the dc voltages of the test nodes are all tied together to a common bus and digitized centrally through a 12bit analog to digital converter(ADC). By converting an ac signal to dc signal through an envelope detector circuit. Techniques of analog routing, where in voltages and/or currents to be measured in some internal circuitry are literally “scanned” out to test pins, here analog circuits are used to route analog voltages/currents, which can themselves lead to signal distortion during propagation. However in the case of time-based architecture, time resolution has improved since the transition time of digital signals has reduced with technology scaling.

The all digital nature of time-based approaches offers itself for scaling and stringent area & power specifications. For time-based architectures, designing ADCs based on this methodology. The two main parts of such solutions are : “transducer” to converts voltages to time pulses or delays, and a scheme to measure time/delays. This technique was extended and a 10bit ADC working at low supply voltage of 0.6v was demonstrated, where as conventional ADC architectures can go up to only 9bit of resolution for a comparator noise of standard deviation of half least bit(LSB).

For gaining popularity, voltage controlled oscillator (VCO) is the another digital approach. In this approach, voltage to be the quantized controls the frequency of the VCO. However to reduce the area overhead, the number of stages in the VCO needs to be small, which increases its operating frequency and hence its power. Another proposal of ADC is a ring oscillator, in which a differential transistor pair drives two identical ring oscillators as a matched load. The voltage difference is digitized by the difference between the counters that capture the frequencies of two oscillators.

In our proposal approach, a small part of the measuring unit, called the sampling head (SpH), is placed at the measurement node it self, avoiding the routing of analog signals over long paths. The sampling head consists of pair of delay cells & a pair of flipflops, which certain control circuitry. Here the sampling head acts as a transducer which converts the analog voltage in to the skew between pair of subsampled signals. The clock pair is centrally processed in an all-digital manner to ectarct this skew.

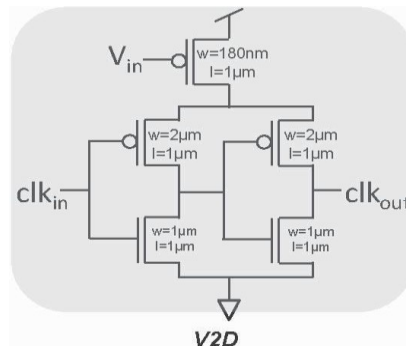
II. Proposed Solution

As coming to the proposed solution, In the proposed system a Built in self test is performed using a sample module which is nothing but a random access memory is designed. The BIST RAM is considered under test and difference advanced test cases are given to test the circuit. The performance is measure in such a way the power consumption reduction.shown in fig. here the sampling heads are placed at each test node, in such away that In order to minimize the routing of analog signals over long paths. I here the each sampling head consists of pair of identical delay cells(V2D) and a pair of flipfpos (DFF). And at the same time here a clock is routed serially to all the sampling heads, which is fed to both delay cells in the sampling heads. The delay of one element of the pair is controlled by the analog voltage V_{Ai} , and at the same time other reference voltage V_{ref} . To measure a certain test node,, the corresponding subsampled signal pair has t o be fed to the delay measurement unit(DMU) with an appropriate select signal to the multiplexer.

As we seen in fig. both the sampling clock (samp clk) and input clock are “picked up” from a single point for each sampling head. hence the cross talk and coupling noise that may effect the clocks do not distribute to additional noise in the sampling head circuitry, and at the same time the output subsampled signal pair of the sampling head are low frequency signals and the skew between them is already amplified by the sub sampling process. This technique of subsampling provides bandwidth/resolution tradeoff, i.e, it needs more time for requiring measurements coarser resolutions can be done faster where as finer resolution measurements.

Module Description

There are some bist implementation techniques there are bist pattern generation, pseudo-random pattern generation, march test SRAM BIST, & parity checker. In bist pattern generation ROM is a method to store a good test-pattern set in a ROM on the chip. Linear feedback shift register is a another method in bist pattern generator to generate pseudo-random tests. Nadeau – dostie proposed a MARCH TEST BIST method to handle



BIST of n’bit word RAMs, out of here we are using four digital techniques, namely as test pattern generator(TPG),control unit (CU),test pattern recorder (TPR), integration module (IM). They provide a serial access design by adding multiplexers to the inputs of write drivers. We see in block diagram application ram is nothing but memory, it having encrypt, clock are the inputs and decrypt, enable are the outputs and at the same time read and write operations are done. if enable is on both read/write operations are done, with out encrypt both read/write operations are not done. Paeudo random means of repetition of frame sizes. Why we are using this means, normally an IC having several components, suppose there is having an fault means we cannot describe that fault easily in software and at the same time hardware also. so that only we described BIST technique.

MODULE 1: Design of Test Pattern Generator (TPG)

Description:

This is the first technique, in which that read accessible memory which is nothing but RAM is placed centre of the block diagram. The test pattern generation is the basic module for Analog built-in self-test (BIST). In the proposed system a Built in self test is performed using a sample module which is nothing but a random access memory (RAM) is designed. The BIST RAM is considered under test and difference advanced test cases are given to test the circuit. We are using the test pattern generator for applying the proper test cases to the BIST RAM. In here the inputs are given by the clock directly to the ram module, it access that inputs if there is any error, it modifies it and then compile that inputs and then after no errors it simulates automatically, for every operation there is both read and write operation, and then simulate the system and then fix design.

Module 2: Design of control unit

Description:

This is the control unit and this is second test technique under this method. This module is implemented for controlling the overall operations in the RAM built-in self-test, this means that several inputs are passing through the system, for every read operation there are some inputs and at the same time for every write operation there are some inputs, we have to send them in correct manner. For obtaining good efficiency, control unit occupies the place in reading the clocks. The control unit makes the control over the writing, reading, addressing and comparison etc. in the built-in self-test. Moreover the control unit will take the decision about the process in the BIST. In this way improves the efficiency.

Module 3: Design of Test Pattern Recorder (TPR)

Description:

This is the test pattern recorder and this is the third test technique in this method. After checking the both read inputs and write inputs, it send that inputs to ram block. In the RAM built-in self-test, the input data to be stored in the RAM memory locations. The comparator in the BIST (built-in self-test) system take the data from the RAM module and also directly from the input with the help of BIST controller. After the comparison we get the output with respect to the inputs of comparator and test the BIST RAM under the different advanced test cases. The performance is measure in such a way the power consumption reduction, Area efficiency is achieved.

Module 4: Design and analysis of Integration module

Description:

This is the integration module and this is the final test technique in this method. Here we are using FPGA, why we are using fpga means there are so many ports like input clk, data in, read out, output clk, in compiling time we don't have specific idea where the error occurs, so that we are using fpga, at any time we are any doubt, send that inputs means both write inputs and write outputs to fpga ports, there we can easily identify the where the fault will occur. We are integrating all the sub modules and output signals are routed into the required ports as per the FPGA device.

III. Design Considerations

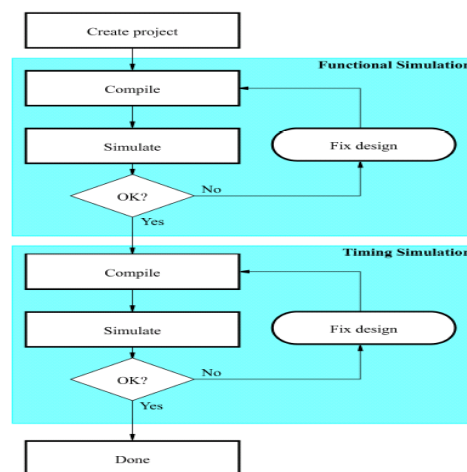
Bist includes reduced test generation effort at all levels. There is a test generation problem in which that it is difficult to carry a stimulus involving hundreds of chip inputs through many layers of circuitry to the chip-under-test. There are some bist implementation techniques there are bist pattern generation, pseudo-random pattern generation, march test SRAM BIST, & parity checker. In bist pattern generation ROM is a method to store a good test-pattern set in a ROM on the chip. Linear feedback shift register is a another method in bist pattern generator to generate pseudo-random tests. Nadeau – dostie proposed a MARCH TEST BIST method to handle BIST of n-bit word RAMs. They provide a serial access design by adding multiplexers to the inputs of write drivers. We see in block diagram application ram is nothing but memory, it having encrypt, clock are the inputs and decrypt, enable are the outputs and at the same time read and write operations are done. if enable is on both read/write operations are done, with out encrypt both read/write operations are not done. Pseudo random means of repetition of frame sizes. Why we are using this means, normally an IC having several components, suppose there is having an fault means we cannot describe that fault easily in software and at the same time hardware also. so that only we described BIST technique.

Model Sim Simulator

Back Ground Details

Designers of digital systems are inevitably faced with the task of testing their designs. Each design can be composed of many components, each of which has to be tested in isolation and then integrated into a design when it operates correctly. To verify that a design operates correctly we use simulation, which is a process of testing the design by applying inputs to a circuit and observing its behavior. The output of a simulation is a set of waveforms that show how a circuit behaves based on a given sequence of inputs. The general flow of a simulation is shown in below Figure. There are two main types of simulation: functional and timing simulation. The functional simulation tests the logical operation of a circuit without accounting for delays in the circuit. Signals are propagated through the circuit using logic and wiring delays of zero. This simulation is fast and useful for checking the fundamental correctness of the designed circuit. The second step of the simulation process is the timing simulation. It is a more complex type of simulation, where logic components and wires take some time to respond to input stimuli. In addition to testing the logical operation of the circuit, it shows the timing of signals in the circuit. This type of simulation is more realistic than the functional simulation; however, it takes longer to perform.

It is the model sim simulator, first of all we have to create a project and then add the project, we have to give a specific name, in that name we have to add modules, here we are using ram module, bist module, integration module. in firstly open model sim simulator and then click file option in that file option we have to open project. After open an project create a project in that space we have to give a specific name and then click ok, then after it shows a add files in that project in that we have to browse a three modules which is nothing but ram, bist, integration. And then after complete all the three modules if it shows any error verifies it and then after start simulation.



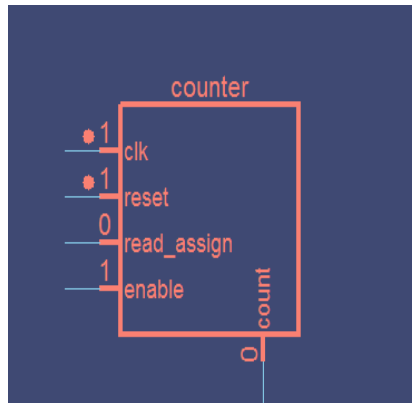
According to design considerations delay cell circuitry sizing of the capacitance between the analog voltage and the input clock is about 2fF. with a decoupling capacitor of 4fF, the kick back will be less than 0.6mV. for a smaller kickback it increases the decoupling capacitor, or cascading has to be implemented. in the cascade, the transistor of gain is 20, and then the decoupling capacitor can be small as 0.1pF.

Every cell of delay is sensitive to supply voltage, in supply voltage the variations occurs and directly impacts the voltage measurement. For a distributed profile across the chip, power supply is located. The measurement of bias voltages is heavily dependent on V_{cal} for the calibration and interpolation. The noisy currents of the voltage-to-delay converter contribute to jitter on clocks. If N delay cells are used in cascade to generate the delay difference, assuming the jitter added by each to be independent of one another, the jitter grows as N^2 , while the total delay cells grows as N . this leads to bandwidth limitation and increased kickback to the analog test node.

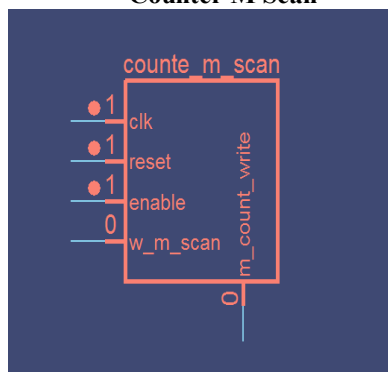
For a given measurement the resolution of measurement of delay difference that can be obtained is, say, 6σ (where σ is the standard deviation of measured delay values). Then coming to desired voltage resolution, the required voltage-to-delay ratio is calculated. Based on the total delay required, one can choose the number of delay cells/stages needed.

For example in design consideration, suppose that resolution of 10ps can be achieved in a given measurement time and that the voltage resolution desired is 1mV. Then the voltage-to-delay converter has to give a differential delay of 10ps/mV. Suppose a single delay cell is designed to provide this delay. On the other hand, if 0.1-mV resolution is desired with the same set up and measurement time.

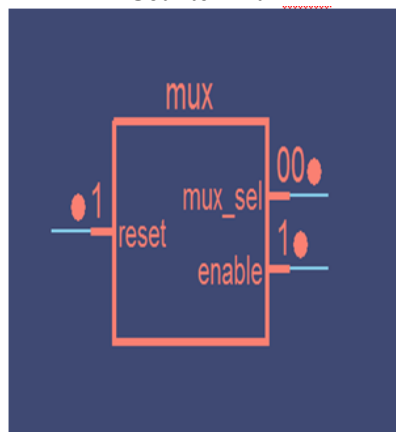
III. Simulation Result Counter



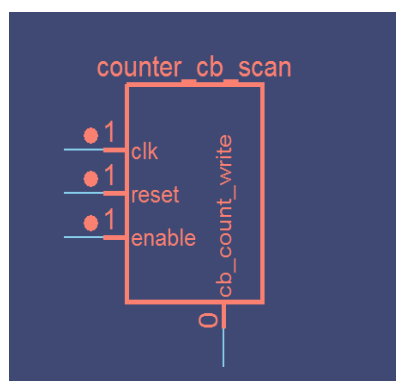
Counter M Scan



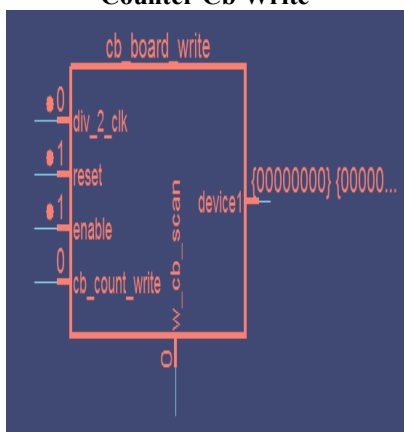
Counter Mux



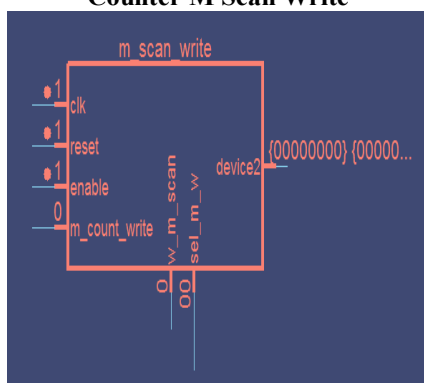
Counter Cb Scan



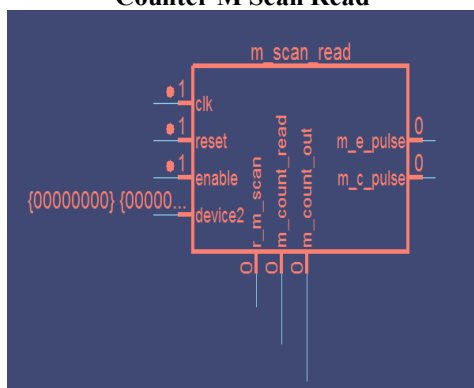
Counter Cb Write



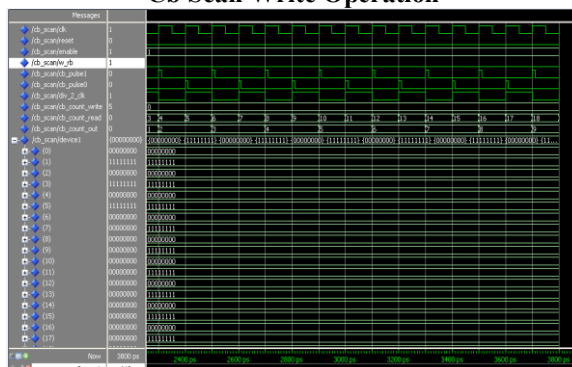
Counter M Scan Write



Counter M Scan Read



Cb Scan Write Operation



reduces the time frequency also. Instead a clock signal a sampling clock of slightly different frequency needs to be routed serially to each sampling head, and a pair of low-frequency subsampled signals need to be routed to the central DMU. We have implemented a sampling head in UMC 130-nm process node and implemented the DMU on FPGA. An effective 5.29b of resolution was demonstrated for low bandwidth signals too, where sample – and – hold circuitry is avoided.

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