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FPGA Implementation of an Efficient VLSI Architecture for Lift Based 5/3 DWT

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Abstract: *The wavelet transform has emerged as advanced technology in the field of VLSI implementation for image compression. Wavelet based coding provides improvements in picture quality at higher compression ratios. In this paper, we propose an efficient VLSI architecture for lifting based 5/3 DWT using FPGA. The lifting scheme 5/3 algorithm is used for implementing 1D-DWT architecture. The 2D-DWT lifting based architecture is designed using 1D-DWT lifting architectures. The proposed architecture uses less hardware interns of dedicated multipliers compared to existing architectures. The proposed architecture is implemented on Virtex-IV FPGA and it is observed that the parameters such as LUT's and delays are efficient.*
Keywords: *Discrete Wavelet Transform (DWT), Lifting Schemes, CDF-5/3, 1D-DWT, 2D-DWT etc.*

I. Introduction

The discrete wavelet transform (DWT) has become one of the most used techniques for signal analysis and image processing applications. The discrete wavelet transform (DWT) performs a multi-resolution signal analysis which has adjustable locality in both time and frequency domains [1]. Due to it is well time–frequency characteristics, one of the most significant uses for (DWT) has been for image compression as in the (JPEG 2000). .The available DWT architecture can be divided broadly into two schemes named as convolution scheme and lifting scheme. Normally convolution scheme is used to implement DWT filters. But this scheme uses huge number of multipliers which is very difficult to implement and take a large amount of resources in hardware. To eliminate those problems lifting schemes is used. This scheme uses the basic convolution equations in such way that the numbers of multipliers are drastically reduced. Due to this reason lifting scheme is widely used to build chip than convolution scheme.

Many lifting based architecture have been proposed for efficient hardware implementation of both 1D and 2D-DWT architectures. Here we briefly discuss a few of them. Mallet [1] proposed modified algorithm for lifting computation where the critical path delay for the lifting equations is 5Tm + 8Ta, where Tm and Ta denote the multiplier and adder delay respectively. The primary reason behind this large delay is stacking of multipliers from the inputs to outputs. To inhibit the effect, the mechanism of flipping has been introduced in which scales the delay down to 3Tm + 4Ta. As a fruitful result, the processing speed increases significantly when the flipped equations are mapped into hardware. Durgasowjanya et al., [2] proposed fixed point 1-D DWT using Lifting Scheme, which operate at uses only 3% of total slice register of Virtex-II FPGA. Nagabushanam M and Ramachandran S. [3] proposed lifting based 1D/2D/3D DWT-IDWT architecture, which uses only 5% of total slice register of Virtex-IV FPGA. K. Andra et al., [4] to generalizes the lifting based architecture, which consists of two row processors, two column processors and two memory modules. But the memory control logic of the architecture is complex

II. Discrete Wavelet Transform

The best way to describe discrete wavelet transform is through a series of cascaded filters. We first consider the FIR based discrete transform. The input image X is fed into a low-pass filter h´ and a high-pass filter g´ separately. The output of the two filters are then sub sampled, resulting low-pass sub band y_L and high-pass sub band y_H. The original signal can be reconstructed by synthesis filters h and g which take the up sampled y_L and y_H as inputs. To perform the forward DWT the standard uses a 1-D sub band decomposition of a 1-D set of samples into low-pass samples and high-pass samples. Low pass samples represent a down sampled low-resolution version of the original set. High-pass samples represent a down sampled residual version of the original set, needed for the perfect reconstruction of the original set.

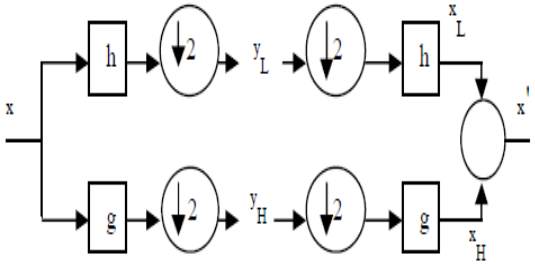

Fig.1: DWT analysis and synthesis system

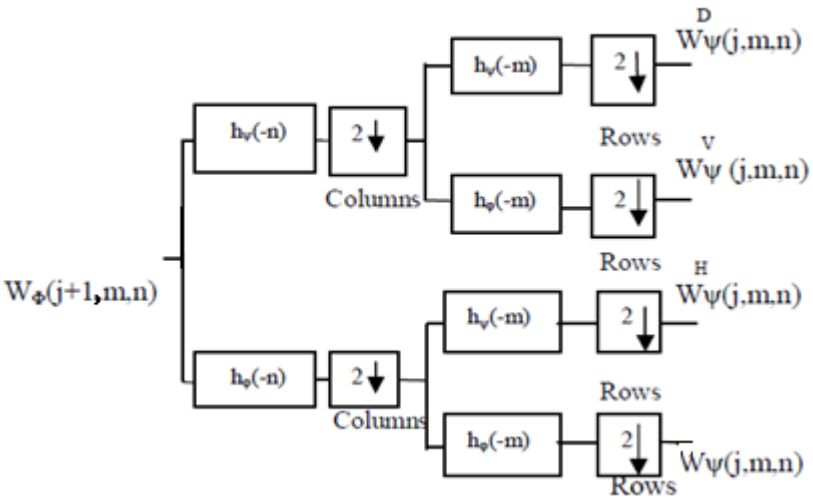

Fig. 2: The 2-D DWT analysis filter bank

III. Mathematical Formulation of DWT

The basic lifting schemes equations for CDF-5/3 [4] are given in equation (1) and (2)

$$y[2n+1] = x[2n+1] - \left[\frac{x[2n]+x[2n+2]}{2}\right] \quad (1)$$

$$y[2n] = x[2n] + [y[2n-1] + y[2n+1]] \quad (2)$$

The above two equations are simplified to get high pass and low pass filter coefficients [4] is given in Table 1.

Table 1: Filter Coefficients of 5/3 DWT

i	LPF Coefficients	LPF Coefficients
0	3/4	1/2
±1	1/4	-1/4
±2	-1/8	0

IV. Proposed Architecture

The proposed 5/3 DWT is separable i.e. we can divide total 2D-DWT architecture into two separate 1D-DWT block as row processor and column processor. The proposed 1D and 2D-DWT is described below.

1.1. 1D-DWT

The basic block diagram of proposed 1D-DWT is shown in Fig. 3. The total 1D-DWT block is built by six shifters, one multiplier, two add/shift unit, one FIFO and one clock divider. The clock divider mainly used to make decimation block. The latency of 1D-DWT block is 4-clock cycle. To indicate that the device is ready an extra signal rst_out is taken as output port. Here we use one counter which counts up to four and when it reaches four then it maintain constant four values. When this counter reaches four then rst_out signal will be high which indicate next block is that 1D-DWT block is ready to give output.

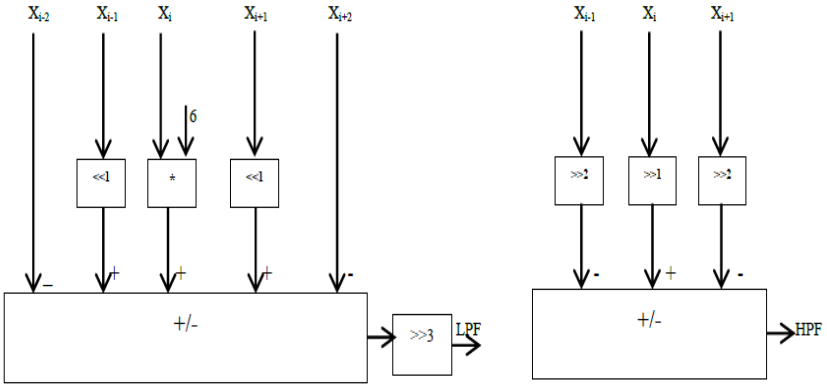

Fig. 3: Proposed 1D-DWT Architecture

1.2. 2D-DWT

The basic block diagram of 2D-DWT is shown in Fig. 4. This module is consists of three 1D-DWT and one dwt_memory block. The 1D-DWT block DWT0 provides one level compression for input image which means it convert 256x256 image into either 128x256 or 256x128 image depending on input reading method of image data. This compressed image pixel data is stored into dwt_memory. This memory block is used to make transpose of the input imge pixels which are compressed. This transpose image is given to DWT1 and DWT2 block to produce LL, LH, HL and HH bands.

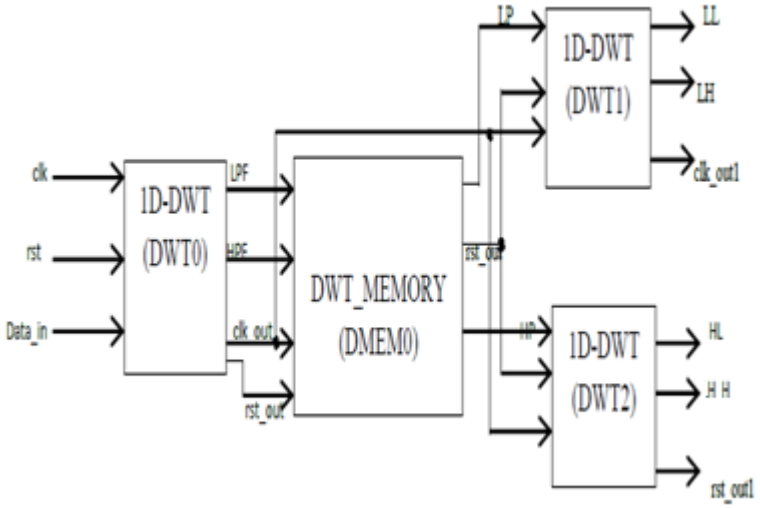

Fig. 4: Proposed 2D-DWT Architecture

II. Hardware Image Output

2.1. 1D-DWT

The output image of 1D-DWT is shown in Fig. 5 which has a size of 128x256 of two bands (named as L and H bands).

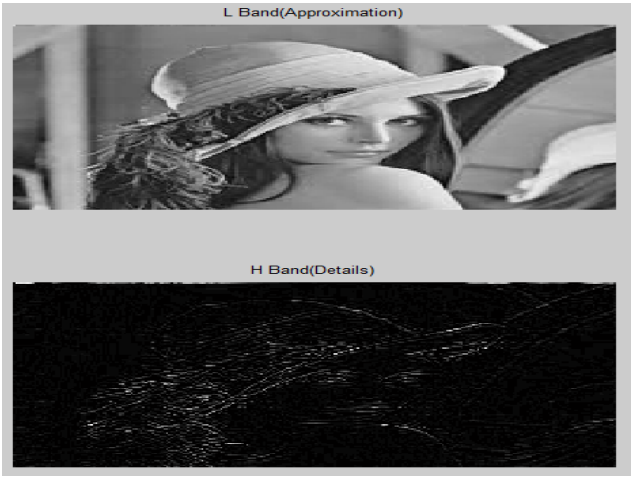

Fig. 5: Image Output of 1D-DWT Block

2.2. 2D-DWT

The output image of 2D-DWT is shown in Fig. 5 which has a size of 128x128 of fourbands (named as LL, LH, HL and HH bands).

Fig. 6: Image Output of 2D-DWT Block

III. RTL Schematic

3.1. 1D-DWT

The extended RTL schematic of 1D-DWT is shown in Fig. 7. Here first input is given to FIFO and then the output of FIFO is connected to the input of cdf_1d block. Extra D-FlipFlop is used for delay synchronization.

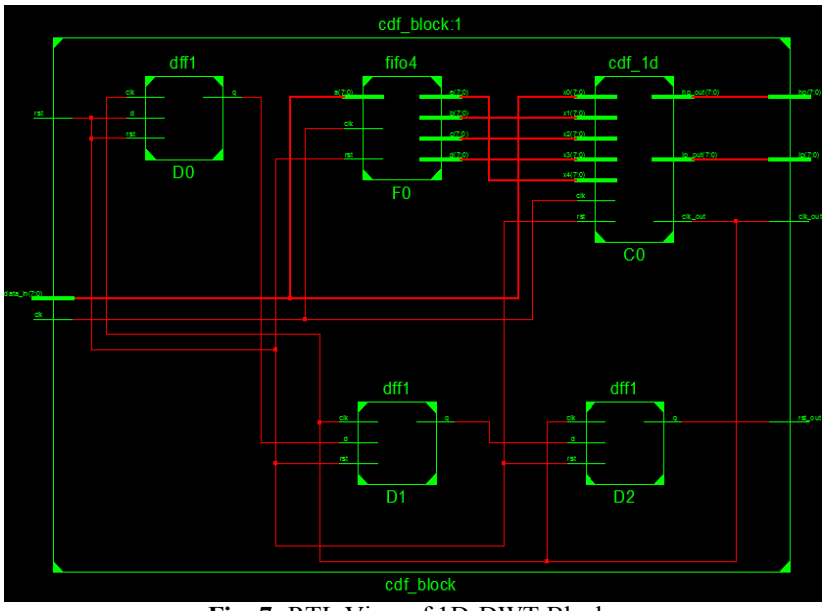

Fig. 7: RTL View of 1D-DWT Block

3.2. 2D-DWT

The extended RTL schematic for 2D-DWT is shown in Fig. 8. Here DWT0 block is used to compresses input image in 1D and dwt_memory is used to take transpose of the compressed image by DWT0. DWT1 and DWT2 are used to perform 1D compression on transposeimage. As a result we get four bands of 2D-DWT.

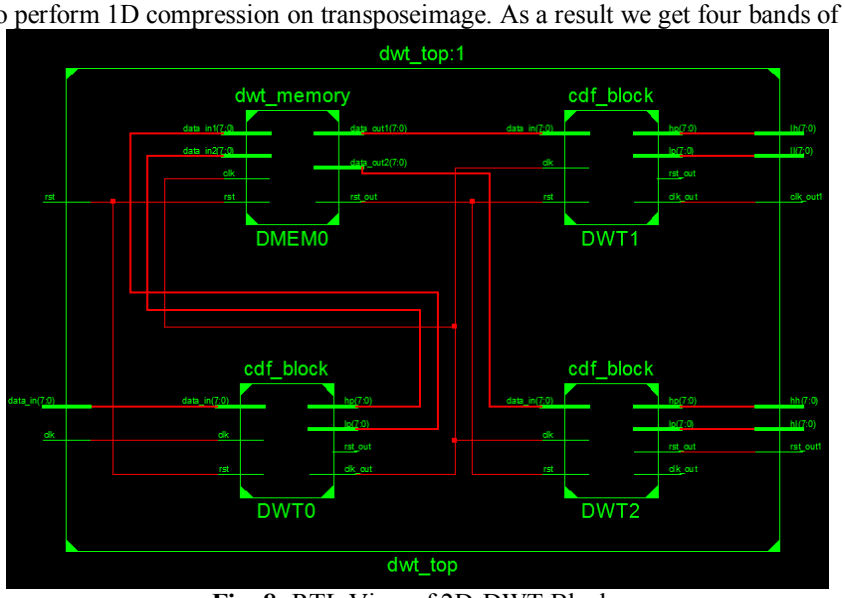

Fig. 8: RTL View of 2D-DWT Block

IV. Comparison Between Existing and Proposed DWT Architecture

4.1. 1D-DWT

The comparison of various 1D-DWT architecture is given in Table 2. The clock rate of proposed architecture is much higher than existing [5,6].

Table 2: Comparisonsof Various 1D-DWT Architecture

Parameters	Husain et al., [5]	Sowmya et al., [6]	Proposed
No. of Slice Registers	373	823	53
No. of Flip Flops	----	634	85
No. of Multipliers	0	2	1
Frequency (MHz)	64	133.786	317

4.2. 2D-DWT

The comparison of various 2D-DWT architectures is given in Table 3 and 4. The clock rate of proposed architecture is higher than existing [6]. The Clock rate of 2D-DWT is very much less than individual 1D-DWT because large amount of memory is used to make transpose of whole image after first level 1D-DWT.

Table 3: Comparison of Various 2D-DWT Architecture

Parameters	Naseer and Mustafa [7]	Proposed
No. of Slices	1299	422
No. of Flip Flops	767	235
Frequency (MHz)	62.797	181.283

The comparisons of various numbers of multipliers, adders and shifters are given in Table 4. In proposed structure numbers of multipliers and adders are less but numbers of shifters are more. Since shifters are made by interchanging wire numbers, so it does not create any hardware.

Table 4: Comparison of Components Used in2D-DWT Architectures

Structure	Multiplier	Shifter	Adder
Andra et al., [4]	4	0	8
Wu et al., [8]	16	0	16
Barua et al., [9]	4	0	8
Liao et al., [10]	4	0	8
Proposed	3	18	6

V. Conclusion

In this paper, we propose an efficient VLSI architecture for lifting based 5/3 DWT using FPGA. The 1D-DWT lift architecture has been designed efficiently by reducing the multipliers. The proposed 1D-DWT is used to design efficient 2D lift based 5/3 DWT. The 2D lift 5/3 is further implemented on Virtex-IV board to test the parameters such as LUT's, slices and delays. It is observed that the proposed architecture is better compared to existing traditional architecture.

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