Low Power and High Performance VLSI Interconnects By Schmitt Trigger Technique In Nanoscale Regime

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Abstract: *In this thesis, we address the interconnect problem in the deep sub-micron (DSM) regime. In VLSI interconnects to restore the input signal affected by the parasitic buffers are placed in between interconnects. But buffers has a certain switching time that contribute the overall signal delay and crosstalk delay. The designs of sized logic and repeater insertion for improved delay, power and placement are implemented by using both Schmitt trigger and buffer insertion. In this work replacement of sized logic with buffers with Schmitt trigger based on sizing is proposed for the signal restoration and to reduce delay. Because of adjustable threshold voltage V_{th} of Schmitt trigger the delay and power can be reduced in interconnects when compared to buffers. HSPICE simulations are carried out for the different PTM based on sized logic shows that Schmitt trigger with sized logic gives 12.45 % less delay when compared to buffer sized logic and also average power reduced to 5.09 % in case of Schmitt trigger when compared to sized logic of buffer.*
Keywords: *Delay, DSM, Interconnects, power , Repeater, Schmitt trigger, sized logic.*

I. Introduction

It is known fact that in modern IC's, interconnect delay has turn out to be the primary performance issue contributing an increasingly important portion to the total cycle delay. While the RC delay of a un-buffered interconnect grows quadratic ally with wire length, buffers have been traditionally used to linearize the dependency of delay on interconnect length. In an optimal buffer insertion the interconnect delay of any given stage are approximately equally divided between the buffer and the wire. But this balance gets disturbed to the wire delay degradation due to process of scaling which leads to an increase in the proportion of the wire delay in a buffered interconnect whose geometries are optically shrunk (without any redesign) to the next technology node. Thus buffer insertion has become a serious step in deep sub-micron design of modern integrated circuits. The insertion of buffers has certain advantages but also leads to increased area and power dissipation thus affecting the overall system performance.

In this work, Schmitt trigger is used as an alternate to buffer insertion. Schmitt trigger is widely used element in electronic circuits which has a special property of responding to slowly changing input waveforms with a fast transition at the output. It also exhibit hysteresis indicating that it has different switching thresholds for positive and negative going input signals.

The driving force behind the rapid growth of the VLSI technology has been the constant reduction of the feature size of VLSI devices. The feature size decrease from about 2mm in 1985 to 0.35- 0.5mm today (1996). Such continual miniaturization of VLSI devices has strong impact on the VLSI technology in several ways. First, the device density increases swiftly – the total number of transistors on a single VLSI chip has increased from less than 500,000 in 1985 to over 10 million. Secondly, the interconnect delay becomes much more important. According to the scaling rules, when the interconnects and devices are scaled down in all three dimensions with a factor of S, then intrinsic gate delay will be reduced by a factor of S, the delay produced in local interconnects (such as connections between adjacent gates) remains the same but the delay of global interconnects increases by a factor of $S2$. As a result, the interconnect delay have become a dominating factor in determining system performance. In many systems designs 50% to 70% of clock cycle are consumed by interconnect delays. This percentage will continue to increase as the feature size decreases further. Not only do interconnects become more important, they also become much more difficult to model and optimize in the deep submicron technology, as the distributed nature of the interconnect has to be considered. For conventional technology with the feature size of 1mm or above the interconnect resistance in most cases is negligible compared to the driver resistance. In this case, the interconnect delay is determined by the driver resistance

times the total interconnect and loading capacitance. In the deep submicron design technology, however, the interconnect resistance is comparable to the driver resistance in many long signal nets. Therefore, interconnect has to be modeled as a distributed RC or RLC circuit. Techniques such as optimal wire sizing, buffer placement, and simultaneous driver, buffer, and wire sizing have become necessary and important.

II.   Repeater/Buffer Insertion Process

The main objective of a uniform repeater insertion system is to minimize the time for a signal is to propagate through a long interconnect. Uniform repeater insertion technique divided the interconnect into equal sections and employ equal size of repeaters to drive each section as shown in Fig.1

In some practical case, the optimum location of the repeaters cannot be achieved due to physical space constraint. Also changing the repeater size can compensate for a change in the ideal physical placement. Bakoglu and Meindl developed an expression for the optimum number and sizes of repeaters to achieve the minimum signal propagation delay in an RC interconnect. Adler and Friedman characterized a timing model for a CMOS inverter driving an RC load. They used this model to enhance the accuracy of the repeater insertion process in RC interconnects. Interconnect width is mainly considered as a design parameter by Alpert .He showed that in RC lines repeater insertion outperforms wire sizing.

The delay can be affected by the line inductance particularly low-resistance materials with fast switching time. Ismail and Friedman extended previous research in repeater insertion by considering the line inductance. They showed that on-chip inductance can decrease the delay and power of the repeater insertion process as compared to an RC line model.
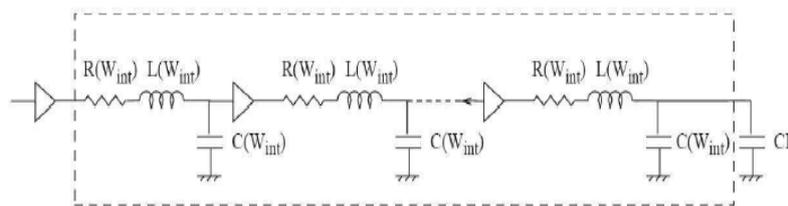

**Fig.1.Uniform repeater insertion driving a distributed RC interconnect**

A.   NON ULE SIZING OF REPEATERS

The ULE optimization technique presented in the previous sections targeted delay minimization. Several additional design objectives are considered in this section based on ULE model. The proposed methodologies extend the use of ULE to delay minimization by buffers and repeaters as well as power optimization.

The proposed ULE technique decreases the delay of a logic path composed of a number of sized stages connected in between of wires. A further decrease in delay can be achieved by changing the number of stages by inserting extra repeaters. This approach is similar to adding inverters to a logic path in LE to obtain a best possible number of stages as in repeater insertion. In many existing repeater insertion methodologies, the inverter can be placed anywhere along the wire. However practically, the wire segments are fixed along the path after placement and routing. The first optimization heuristic incorporated into ULE is based on repeater insertion within long wire segments along the path (see Fig. 2). In this case, the wires are divided by repeaters into shorter segments prior to the ULE sizing. For example, the number of repeaters can be determined from

$$Di = \tau . di = \tau . (gi . hi + Pi).$$

After repeater insertion, ULE optimization is performed to determine the optimal size of the individual logic gates and repeaters.
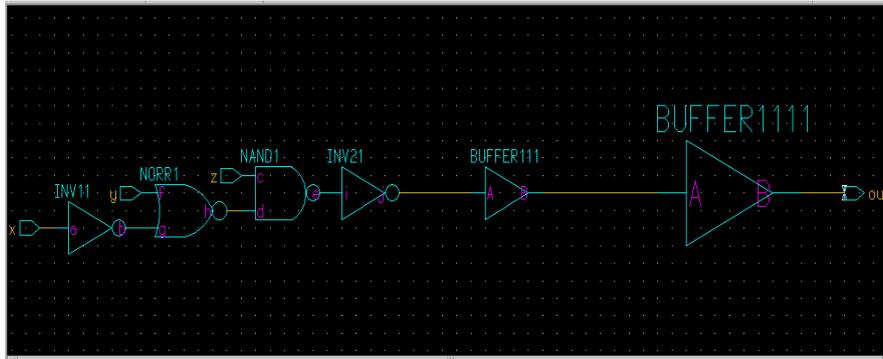
Fig.2 Repeaters can be inserted along wires while cascaded buffers are added and sized to maintain small logic gates.

Another optimization step can be performed in addition to repeater insertion is the optimal size of those logic gates that drive long interconnect can be large expending excessive area and power. This effect is mainly significant in multiple input logic gates where all of the transistors are scaled to obtain the optimum size if one of the inputs is along the critical path. Non-uniform buffers are inserted to drive the long wire segments as shown in Fig. 2 to solve this problem. The optimal number of inverters in each cascaded buffer is determined from the LE model since the wire impedance between the cascaded inverters is negligible. Sizing the entire path is determined from the ULE. Note that the resulting size of the repeaters after ULE optimization can be different than the equal size as described in [3]. As exemplified in previous sections, the ULE method converges to the equal sizing factor in the case of long wires but produces different results when shorter wire segments are considered (such as in repeaters insertion) and when sizing is influenced by neighboring gates. Thus, after repeater insertion, the ULE optimization process produces optimal sizing resulting in a shorter delay as compared to equal sizing in repeater insertion system.
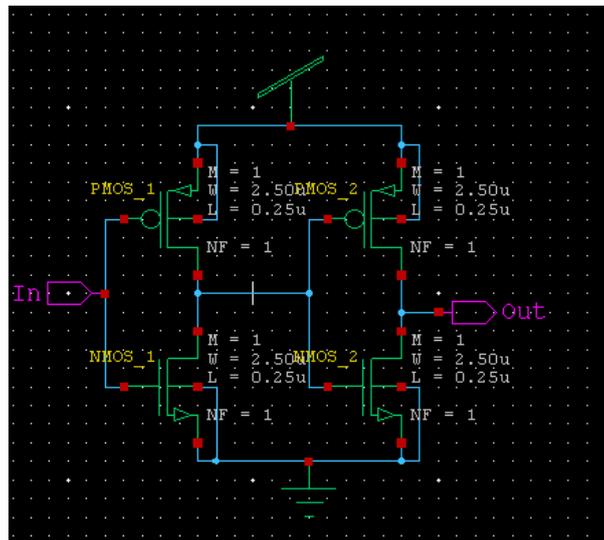
Fig3. CMOS buffer circuit

III. Proposed Work

In this four transistor Schmitt trigger is used as an alternate to buffer insertion in buses. The main motivation of this approach is that a buffer responds to an input signal only after it exceeds higher than half of given voltage i.e Vdd/2 but Schmitt trigger can be designed to have a threshold voltage less than Vdd/2 and thus can be made to respond faster and by this the delay can be reduced in cost of area.

Let us consider an input signal by a fast rising edge given to the input of the circuit. Ideally, the signal at the end of the circuit should be in the same shape but the delay produced by the interconnect due to parasitic capacitances leads to far-end signal being obtained only after certain time has been elapsed. This value can be high i.e a few nanoseconds depending on the values of resistance and parasitic capacitance. While a buffer is repeatedly used to restore the original signal and its output is obtained only after the input voltage signal crosses Vdd/2. But the Schmitt trigger can be designed to have a lower threshold voltage so that it can respond faster

than a buffer. It compares the response of a buffer and a Schmitt trigger to a slowly varying input. The buffer is designed with 2 CMOS inverters placed back to back (figure 3). Buffer is designed with minimal lambda parameters for different technologies by keeping Wp = 2Wn to ensure equal rise and fall time of the signal. Schmitt trigger used in this approach has 4 MOS transistors which are comparable is size with the transistors used in buffer.
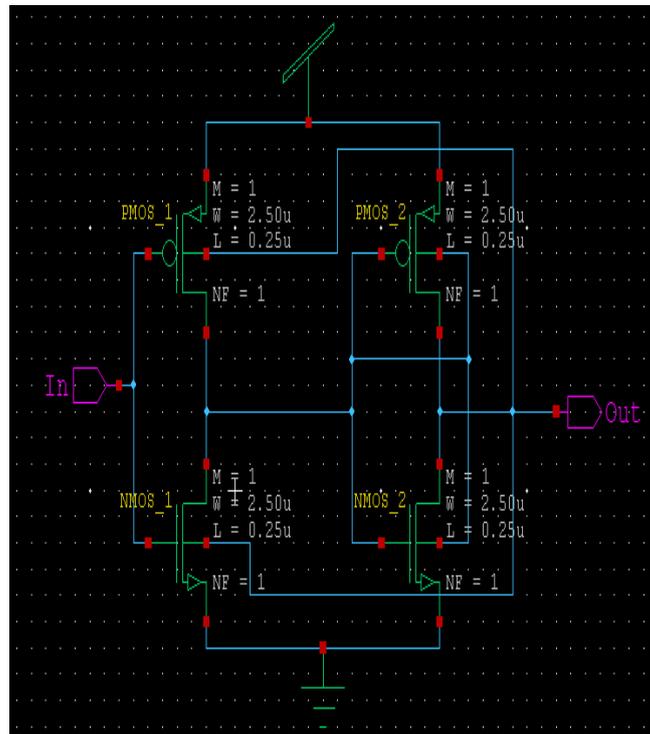

Fig4. CMOS Schmitt trigger circuit using 4 MOS transistors.

All these factors are not in support of buffer insertion for interconnect modeling. Thus a major Breakthrough is needed to handle interconnects. Hence keeping in mind of all the problems being faced and to be coming with buffer insertion, in this thesis, an alternate to buffer is proposed and tried analyzing the results. In the new approach buffer is replaced by Schmitt trigger and analyzed all the above mentioned factor.
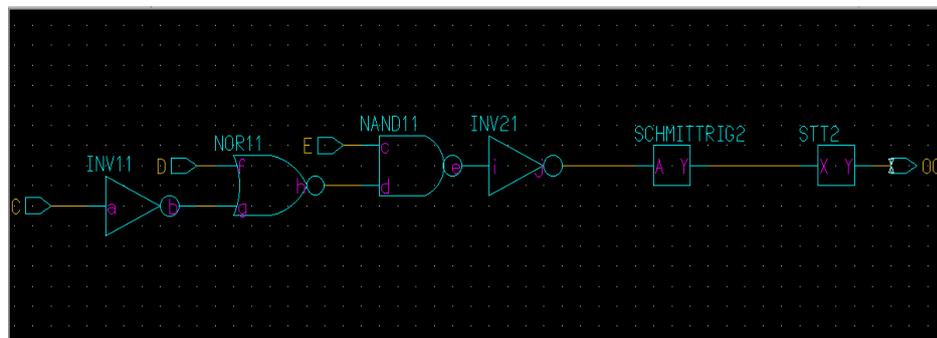

Fig5. Sized logic with Schmitt trigger circuit

A. DELAY ANALYSIS:
The main advantage of using Schmitt trigger in place of buffer is that we can control threshold voltage limits. Let us consider an input signal with a very slow rise time given to the input end of the interconnect. Ideally the signal obtained at the output should be in the same shape but the interconnect delay/RC delay (the delay produced by parasitic) will play a very important role in deep submicron technologies so the output signal gets delayed due to the parasitic capacitance and inductance and reaches to high voltage after a certain amount of time. This delay may be high i.e. in few nanoseconds when the values of resistance and parasitic capacitance are high. By this we get a delayed as well as a deformed output waveform. To rectify this deformed waveform we insert buffer at the output end of the interconnect. Now until the delayed signal reaches higher than Vdd/2

the output of the buffer will remain low i.e. at zero volts and whenever it reaches to a value less than Vdd/2 it will directly go to high within the switching time of a buffer as shown in figure1. So efficiently we saved half of the RC product in terms of delay.

In this we considered the interconnect as a linear structure ignoring the tree structure and also all interconnects are treated as RC models. Firstly the critical repeater length for each technology is calculated. Here repeater length is the minimum distance beyond which inserting an optimal-sized buffer makes the interconnect delay smaller than the corresponding unrepeated wire.

IV.   Simulation Results And Comparisions

The existing and proposed methods are performed on four different process parameters Viz. 180nm, 90nm, 65nm and 45nm using H-spice simulator at 27⁰c. The supply voltages to be considered for the four process parameters (technologies) along with the threshold voltages for NMOS and PMOS in the respective technologies are as shown in Table 4.1.

TABLE 4.1 Supply Voltages and Threshold Voltage values

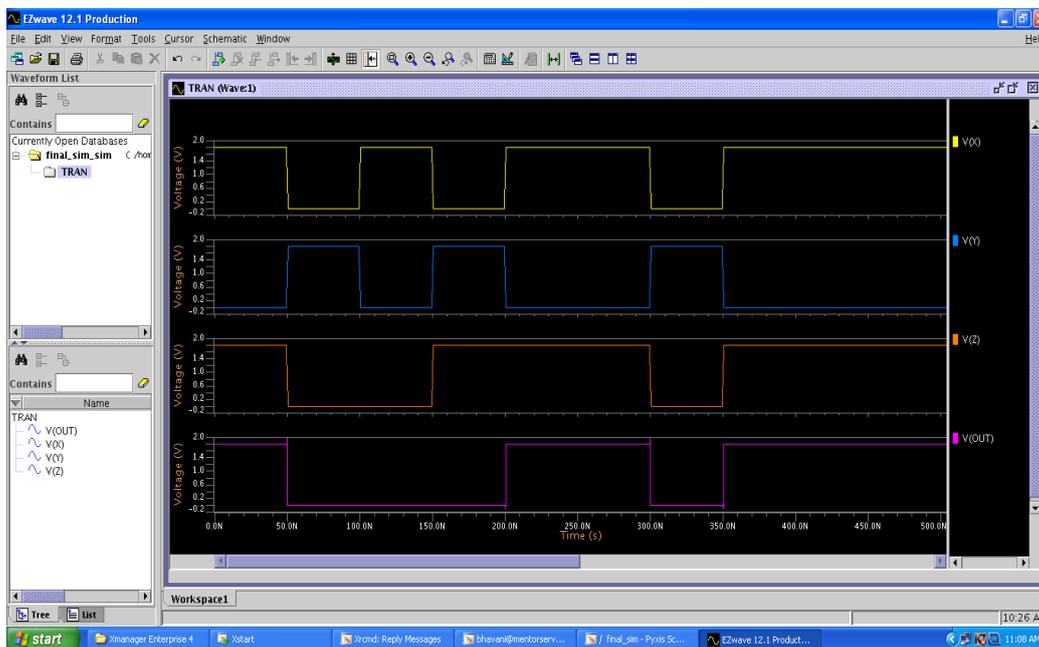| Technology	180nm	90nm	65nm	45nm
Supply Voltage	1.8V	1.2V	1.1V	1V
NMOS V_T (V)	0.3999	0.2607	0.22	0.1711
PMOS V_T (V)	-0.42	-0.303	-0.22	-0.1156

**Fig6. Simulation waveforms Schmitt trigger technique in logical sizing**

A) MINIMUM SIZED LOGIC REPEATER INSERTION, CASCADED SIZED LOGIC WITH UNIFORM REPEATER INSERTION AND SIZED LOGIC WITH NON-UNIFORM REPEATER INSERTION

The four criteria are applied to a different CMOS technology (i.e 45nm, 65nm, 90nm, 180nm) to determine the optimum solution for different line lengths. All the above three methods delay and power are compared with different technologies. The optimum solution for each criterion is listed in Table 4.2, 4.3, 4.4 a clock signal with a 2ns transition.
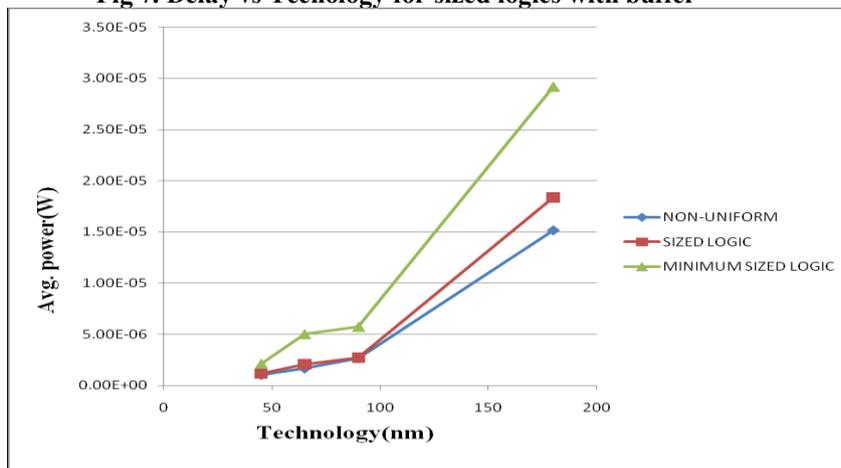
1. DELAY

Table4.2. Delay comparison with different method

TECHNOLOGY (nm)	DELAY(Ps)		
	MINIMUM SIZED LOGIC	SIZED LOGIC	NON-UNIFORM REPEATER
180	126.75	114.95	116.85
90	147	117.45	120.75
65	168.05	128.94	149.6
45	233.4	203.50	229.93
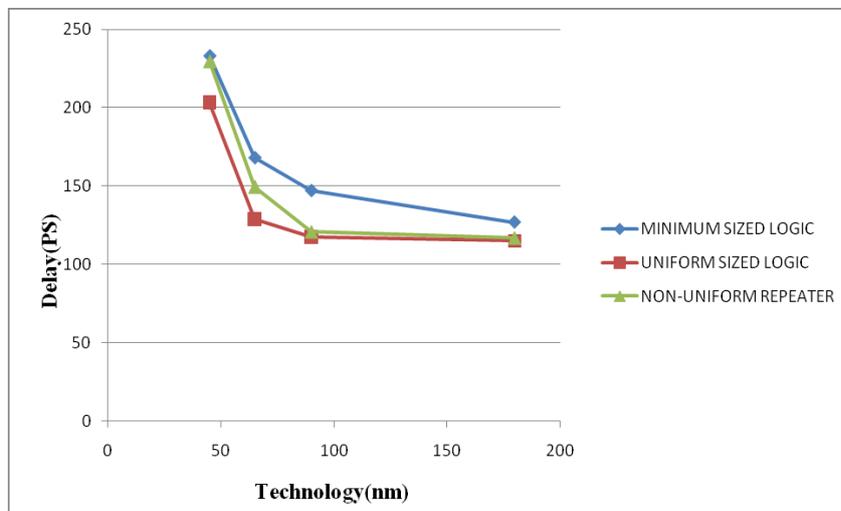
Fig 7. Delay vs Tecnology for sized logics with buffer

Fig 8. Avg power vs Technology for sized logics with buffer

2. AVERAGE POWER

Table 4.3 Delay comparison with different methods

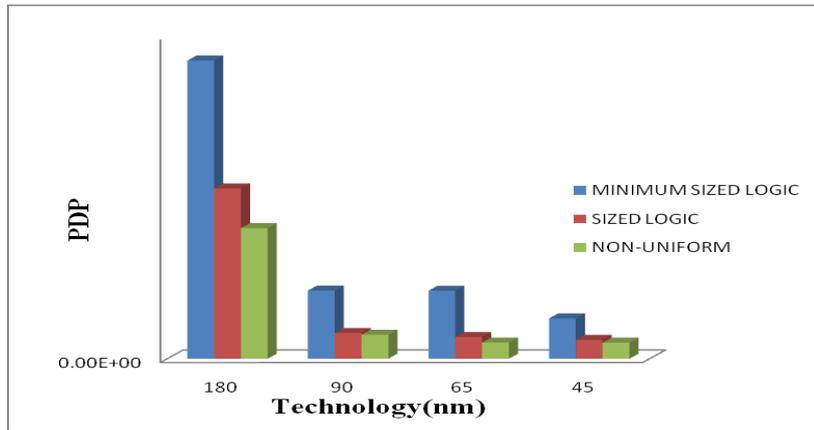| TECHNOLOGY (nm)	AVERAGE POWER(W)		
	MINIMUM SIZED LOGIC	SIZED LOGIC	NON-UNIFORM REPEATER
180	2.9185E-05	1.8376E-05	1.5164E-05
90	5.7553E-06	2.7198E-06	2.6849E-06
65	5.022E-06	2.0900E-06	1.6804E-06
45	2.1431E-06	1.1458E-06	1.0515E-06

Fig9. Power delay product vs Tecnology for sized logics with buffer

3. POWER DELAY PRODUCT

Table 4.4 PDP with different methods

TECHNOLOGY (nm)	PDP		
	MINIMUM SIZED LOGIC	SIZED LOGIC	NON-UNIFORM REPEATER
180	3.699E-15	2.1123E-15	1.7719E-15
90	8.46E-16	3.1944E-16	3.2688E-16
65	8.439E-16	2.694E-16	2.5138E-16
45	5.001E-16	2.331E-16	2.4177E-16

B) COMPARISON OF SIZED LOGIC WITH NON-UNIFORM REPEATER INSERTION AND SIZED LOGIC WITH SCHMITT TRIGGER INSERTION TECHNIQUE

    The four criteria are applied to a different CMOS technology (i.e 45nm, 65nm, 90nm, 180nm) to determine the optimum solution for different line lengths. Comparison of non-uniform repeater insertion and Schmitt trigger insertion technique. The optimum solution for each criterion is listed in Table 4.5 a clock signal with a 2ns transition.

1. DELAY

Table 4.5 Delay comparison between sized logics with buffer and Schmitt trigger

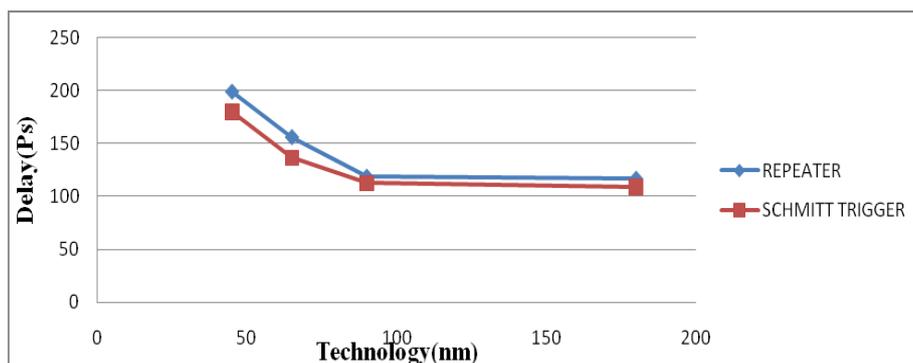| TECHNOLOGY(nm)	DELAY(Ps)		PERCENTAGE DECREASE IN DELAY (%)
	REPEATER	SCHMITT TRIGGER	
180	116.65	108.79	6.738
90	118.6	112.55	5.1011
65	155.8	136.4	12.45
45	198.55	179.55	9.5693

Fig 10. Delay vs Technology for sized logics with buffer and Schmitt trigger

2. AVERAGE POWER

Table 4.6 Average power comparison between sized logics with buffer and Schmitt trigger

TECHNOLOGY (nm)	AVERAGE POWER(W)		PERCENTAGE DECREASE IN AVERAGE POWER %
	REPEATER	SCHMITT TRIGGER	
180	2.1127E-05	2.0854E-05	1.292 %
90	4.0455E-06	4.0102E-06	0.872 %
65	2.5667E-06	2.4883E-06	3.054 %
45	1.2828E-06	1.2175E-06	5.090 %

Buffer consumes 5.09% more power per   cycle than the proposed Schmitt trigger technique.

V.   Conclusions

The delay introduced in interconnect is more when compared to the gate delay in DSM. In this we used the sized logic with buffer and Schmitt trigger. The proposed Schmitt trigger (depending on Sized logic) is used in place of buffers in between the interconnects for further reduction of delay and power. A four MOS transistor Schmitt trigger is implemented for this analysis. The simulation results shows that proposed technique exhibit less Delay and power when compared to the existing techniques. It is also proved here that the proposed technique works even at nanometer designs.

- Programmable dual threshold property of Schmitt trigger allows the designer to control lower thresholds for fast signal switching time.
- Lower thresholds are advantageous at the time of switching too, as it would not allow all the transistors to be in active or saturation mode.
- Noise immunity of Schmitt trigger is more than buffer because of larger band gap.

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